Integrated Circuit Systems, Inc.

ICS87004
1:4, DIFFERENTIAL-TO-LVCMOS/LVTTL ZERO DELAY CLOCK GENERATOR

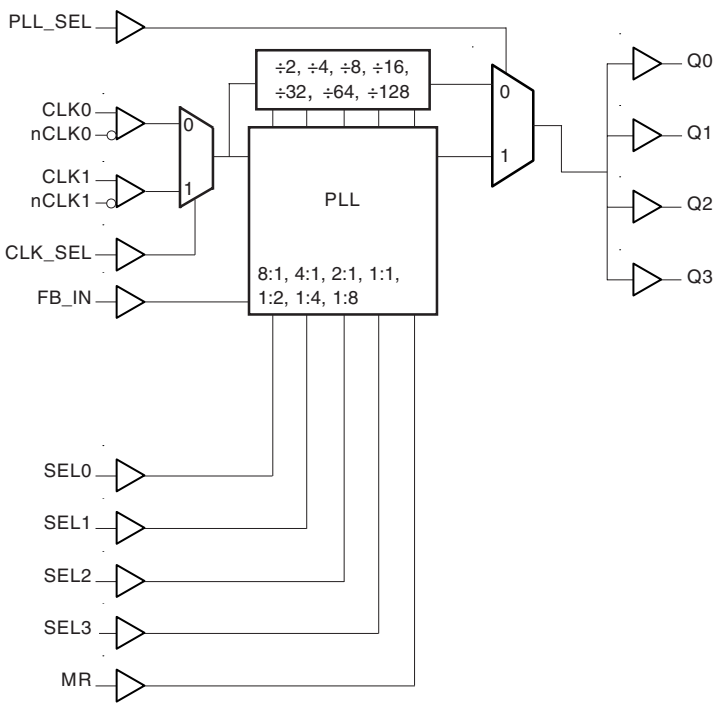
GENERAL DESCRIPTION

The ICS87004 is a highly versatile 1:4 Differential-to-LVCMOS/LVTTL Clock Generator and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS87004 has two selectable clock inputs. The CLK0, nCLK0 and CLK1, nCLK1 pairs can accept most standard differential input levels. Internal bias on the nCLK0 and nCLK1 inputs allows the CLK0 and CLK1 inputs to accept LVCMOS/LVTTL. The ICS87004 has a fully integrated PLL and can be configured as zero delay buffer, multiplier or divider and has an input and output frequency range of 15.625MHz to 250MHz. The reference divider, feedback divider and output divider are each programmable, thereby allowing for the following output-to-input frequency ratios: 8:1, 4:1, 2:1, 1:1, 1:2, 1:4, 1:8. The external feedback allows the device to achieve "zero delay" between the input clock and the output clocks. The PLL_SEL pin can be used to bypass the PLL for system test and debug purposes. In bypass mode, the reference clock is routed around the PLL and into the internal output dividers.

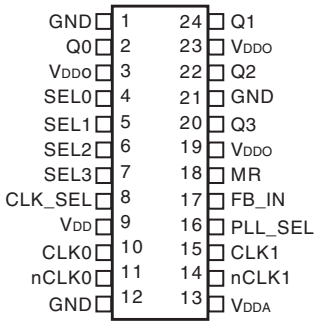
FEATURES

- 4 LVCMOS/LVTTL outputs, 7Ω typical output impedance
- Selectable CLK0, nCLK0 or CLK1, nCLK1 clock inputs
- CLKx, nCLKx pairs can accept the following differential input levels: LVPECL, LVDS, LVHSTL, HCSL, SSTL
- Internal bias on nCLK0 and nCLK1 to support LVCMOS/LVTTL levels on CLK0 and CLK1 inputs
- Output frequency range: 15.625MHz to 250MHz
- Input frequency range: 15.625MHz to 250MHz
- VCO range: 250MHz to 500MHz
- External feedback for "zero delay" clock regeneration with configurable frequencies
- Programmable dividers allow for the following output-to-input frequency ratios: 8:1, 4:1, 2:1, 1:1, 1:2, 1:4, 1:8
- Fully integrated PLL
- Cycle-to-cycle jitter: 45ps (maximum)
- Output skew: 45ps (maximum)
- Static phase offset: 50 ± 125ps (3.3V ± 5%)
- Full 3.3V or 2.5V operating supply
- 5V tolerant inputs
- Lead-Free package available
- Industrial temperature information available upon request

BLOCK DIAGRAM



PIN ASSIGNMENT



24-Lead TSSOP

4.40mm x 7.8mm x 0.92mm

G Package

Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 12, 21	GND	Power		Power supply ground.
2, 20, 22, 24	Q0, Q3, Q2, Q1	Output		Clock outputs. 7Ω typical output impedance. LVCMOS/LVTTL interface levels.
3, 19, 23	V_{DDO}	Power		Output supply pins.
4, 5, 6, 7	SEL0, SEL1, SEL2, SEL3	Input	Pulldown	Determines output divider values in Table 3. LVCMOS/LVTTL interface levels.
8	CLK_SEL	Input	Pulldown	Clock select input. When HIGH, selects differential CLK1, nCLK1. When LOW, selects differential CLK0, nCLK0. LVCMOS/LVTTL interface levels.
9	V_{DD}	Power		Core supply pin.
10	CLK0	Input	Pulldown	Non-inverting differential clock input.
11	nCLK0	Input	Pullup/ Pulldown	Inverting differential clock input. V_{DD}/2 default when left floating.
13	V_{DDA}	Power		Analog supply pin.
14	nCLK1	Input	Pullup/ Pulldown	Inverting differential clock input. V_{DD}/2 default when left floating.
15	CLK1	Input	Pulldown	Non-inverting differential clock input.
16	PLL_SEL	Input	Pullup	Selects between the PLL and reference clock as input to the dividers. When LOW, selects the reference clock (PLL Bypass). When HIGH, selects PLL (PLL Enabled). LVCMOS/LVTTL interface levels.
17	FB_IN	Input	Pulldown	LVCMOS/LVTTL feedback input to phase detector for regenerating clocks with "zero delay". Connect to one of the outputs. LVCMOS/LVTTL interface levels.
18	MR	Input	Pulldown	Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the outputs to go low. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		KΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		KΩ
C_{PD}	Power Dissipation Capacitance (per output)	V_{DD}, V_{DDA}, V_{DDO} = 3.465V			23	pF
		V_{DD}, V_{DDA}, V_{DDO} = 2.625V			17	pF
R_{OUT}	Output Impedance		5	7	12	Ω

TABLE 3A. PLL ENABLE FUNCTION TABLE

Inputs					Outputs PLL_SEL = 1 PLL Enable Mode
SEL3	SEL2	SEL1	SEL0	Reference Frequency Range (MHz)	Q0:Q3
0	0	0	0	125 - 250	÷ 1
0	0	0	1	62.5 - 125	÷ 1
0	0	1	0	31.25 - 62.5	÷ 1
0	0	1	1	15.625 -31.25	÷ 1
0	1	0	0	125 - 250	÷ 2
0	1	0	1	62.5 - 125	÷ 2
0	1	1	0	31.25 - 62.5	÷ 2
0	1	1	1	125 - 250	÷ 4
1	0	0	0	62.5 - 125	÷ 4
1	0	0	1	125 - 250	÷ 8
1	0	1	0	62.5 - 125	x 2
1	0	1	1	31.25 - 62.5	x 2
1	1	0	0	15.625 - 31.25	x 2
1	1	0	1	31.25 - 62.5	x 4
1	1	1	0	15.625 - 31.25	x 4
1	1	1	1	15.625 - 31.25	x 8

TABLE 3B. PLL BYPASS FUNCTION TABLE

Inputs				Outputs PLL_SEL = 0 PLL Bypass Mode
SEL3	SEL2	SEL1	SEL0	Q0:Q3
0	0	0	0	÷ 8
0	0	0	1	÷ 8
0	0	1	0	÷ 8
0	0	1	1	÷ 16
0	1	0	0	÷ 16
0	1	0	1	÷ 16
0	1	1	0	÷ 32
0	1	1	1	÷ 32
1	0	0	0	÷ 64
1	0	0	1	÷ 128
1	0	1	0	÷ 4
1	0	1	1	÷ 4
1	1	0	0	÷ 8
1	1	0	1	÷ 2
1	1	1	0	÷ 4
1	1	1	1	÷ 2

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, V_O	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA}	70°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO}$ = 3.3V±5%, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				100	mA
I_{DDA}	Analog Supply Current				16	mA
I_{DDO}	Output Supply Current				6	mA

TABLE 4B. LVCMOS / LVTTL DC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO}$ = 3.3V±5% OR 2.5V±5%, TA = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	PLL_SEL, CLK_SEL, SEL0, SEL1, SEL2, SEL3, FB_IN, MR		2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	PLL_SEL, CLK_SEL, SEL0, SEL1, SEL2, SEL3, FB_IN, MR		-0.3		0.8	V
I_{IH}	Input High Current	CLK_SEL, MR, FB_IN, SEL0, SEL1, SEL2, SEL3	$V_{DD} = V_{IN}$ = 3.465V, $V_{DD} = V_{IN}$ = 2.625V			150	µA
		PLL_SEL	$V_{DD} = V_{IN}$ = 3.465V, $V_{DD} = V_{IN}$ = 2.625V			5	µA
I_{IL}	Input Low Current	CLK_SEL, MR, FB_IN, SEL0, SEL1, SEL2, SEL3	V_{DD} = 3.465V, V_{IN} = 0V, V_{DD} = 2.625V, V_{IN} = 0V	-5			µA
		PLL_SEL	V_{DD} = 3.465V, V_{IN} = 0V, V_{DD} = 2.625V, V_{IN} = 0V	-150			µA
V_{OH}	Output High Voltage; NOTE 1		V_{DDO} = 3.465V	2.6			V
			V_{DDO} = 2.625V	1.8			V
V_{OL}	Output Low Voltage; NOTE 1		V_{DDO} = 3.465V or 2.625V			0.5	V

NOTE 1: Outputs terminated with 50Ω to V_{DDO}/2. In the Parameter Measurement Information Section, see *Output Load Test Circuit Diagrams.*

TABLE 4C. DIFFERENTIAL DC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO}$ = 3.3V±5% OR 2.5V±5%, TA = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK0, CLK1	$V_{DD} = V_{IN}$ = 3.465V, $V_{DD} = V_{IN}$ = 2.625V			150	µA
		nCLK0, nCLK1	$V_{DD} = V_{IN}$ = 3.465V, $V_{DD} = V_{IN}$ = 2.625V			150	µA
I_{IL}	Input Low Current	CLK0, CLK1	V_{DD} = 3.465V, V_{IN} = 0V, V_{DD} = 2.625V, V_{IN} = 0V	-5			µA
		nCLK0, nCLK1	V_{DD} = 3.465V, V_{IN} = 0V, V_{DD} = 2.625V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Input Voltage			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			GND + 0.5		V_{DD} - 0.85	V

NOTE 1: Common mode voltage is defined as V_{IH}.
NOTE 2: For single ended applications, the maximum input voltage for CLK0, nCLK0 and CLK1, nCLK1 is V_{DD} + 0.3V.

TABLE 4D. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO}$ = 2.5V±5%, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		2.375	2.5	2.625	V
V_{DDA}	Analog Supply Voltage		2.375	2.5	2.625	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current				96	mA
I_{DDA}	Analog Supply Current				15	mA
I_{DDO}	Output Supply Current				6	mA

TABLE 5A. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO}$ = 3.3V±5%, TA = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency			15.625		250	MHz
t_{PD}	Propagation Delay, NOTE 1	CLK0, nCLK0 CLK1, nCLK1	PLL_SEL = 0V f ≤ 250MHz, Qx ÷ 2	5		6	ns
t(Ø)	Static Phase Offset; NOTE 2, 4	CLK0, nCLK0 CLK1, nCLK1	PLL_SEL = 3.3V f_{REF} ≤ 167MHz, Qx ÷ 1	-75	50	175	ps
*t*sk(o)	Output Skew; NOTE 3, 4	CLK0, nCLK0 CLK1, nCLK1	PLL_SEL = 0V		40	50	ps
*t*jit(cc)	Cycle-to-Cycle Jitter; NOTE 4		f_{OUT} > 40MHz		30	45	ps
t_L	PLL Lock Time					1	ms
t_R / t_F	Output Rise/Fall Time		20% to 80%	400		800	ps
odc	Output Duty Cycle			40	50	60	%

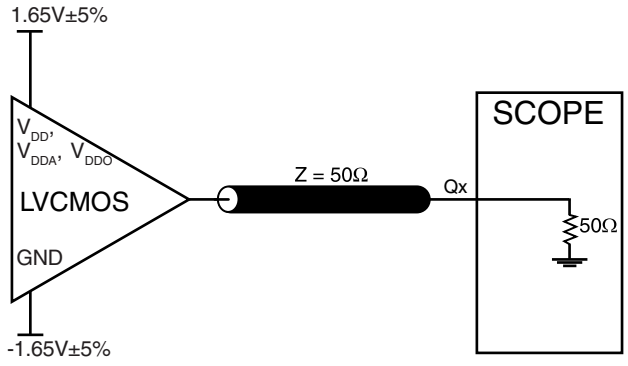
NOTE 1: Measured from the differential input crossing point to the output at V_{DDO}/2.
NOTE 2: Defined as the time difference between the input reference clock and the average feedback input signal when the PLL is locked and the input reference frequency is stable.
NOTE 3: Defined as skew between outputs at the same supply voltages and with equal load conditions. Measured at V_{DDO}/2.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 5B. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO}$ = 2.5V±5%, TA = 0°C TO 70°C

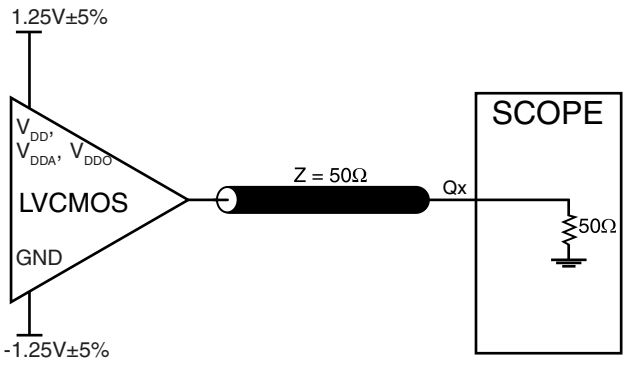
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency			15.625		250	MHz
t_{PD}	Propagation Delay, NOTE 1	CLK0, nCLK0 CLK1, nCLK1	PLL_SEL = 0V f ≤ 250MHz, Qx ÷ 2	5.3		6.7	ns
t(Ø)	Static Phase Offset; NOTE 2, 4	CLK0, nCLK0 CLK1, nCLK1	PLL_SEL = 2.5V f_{REF} ≤ 167MHz, Qx ÷ 1	-175	-25	125	ps
*t*sk(o)	Output Skew; NOTE 3, 4	CLK0, nCLK0 CLK1, nCLK1	PLL_SEL = 0V		40	45	ps
*t*jit(cc)	Cycle-to-Cycle Jitter; NOTE 4		f_{OUT} > 40MHz		35	45	ps
t_L	PLL Lock Time					1	ms
t_R / t_F	Output Rise/Fall Time		20% to 80%	400		700	ps
odc	Output Duty Cycle			44	50	56	%

NOTE 1: Measured from the differential input crossing point to the output at V_{DDO}/2.
NOTE 2: Defined as the time difference between the input reference clock and the average feedback input signal when the PLL is locked and the input reference frequency is stable.
NOTE 3: Defined as skew between outputs at the same supply voltages and with equal load conditions. Measured at V_{DDO}/2.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

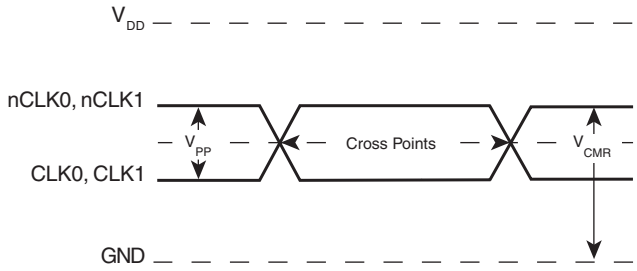
PARAMETER MEASUREMENT INFORMATION



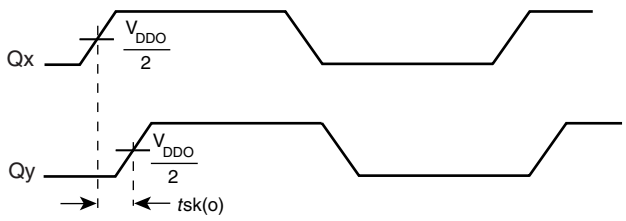
3.3V OUTPUT LOAD AC TEST CIRCUIT



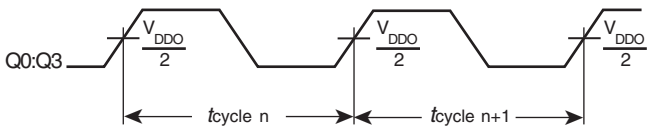
2.5V OUTPUT LOAD AC TEST CIRCUIT



DIFFERENTIAL INPUT LEVEL



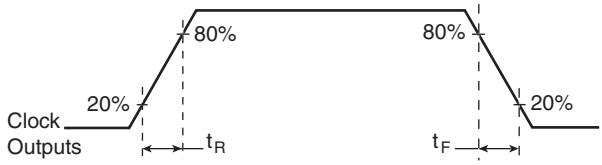
OUTPUT SKEW



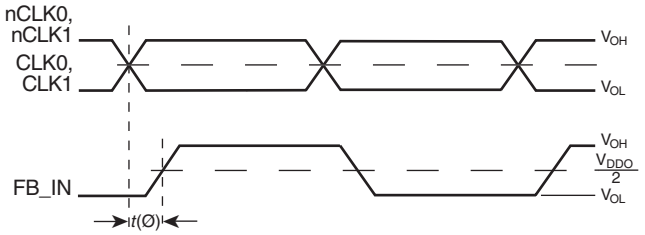
$t_{jit(cc)} = t_{cycle\ n} - t_{cycle\ n+1}$

1000 Cycles

CYCLE-TO-CYCLE JITTER

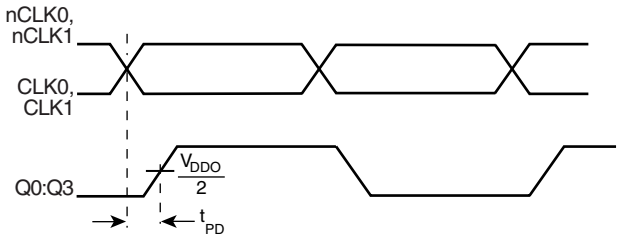


OUTPUT RISE/FALL TIME

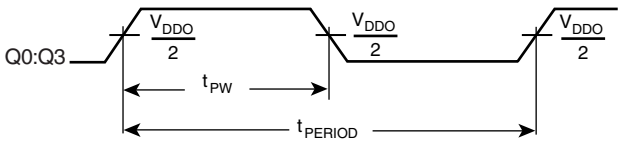


$t(Ø)_{mean}$ = Static Phase Offset
(where $t(Ø)$ is any random sample, and $t(Ø)_{mean}$ is the average of the sampled cycles measured on controlled edges)

STATIC PHASE OFFSET



PROPAGATION DELAY



$$odc = \frac{t_{PW}}{t_{PERIOD}}$$

OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS87004 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD}, V_{DDA}, and V_{DDO} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a 10µF and a .01µF bypass capacitor should be connected to each V_{DDA}.

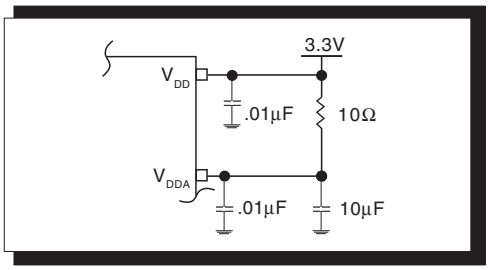


FIGURE 1. POWER SUPPLY FILTERING

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 2 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{DD}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

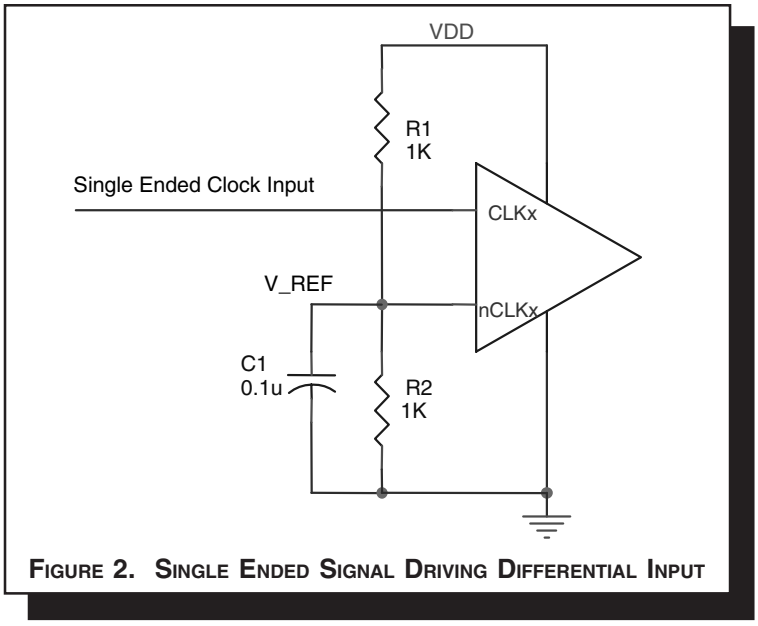


FIGURE 2. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

DIFFERENTIAL CLOCK INPUT INTERFACE

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. Figures 3A to 3D show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in *Figure 3A,* the input termination applies for ICS HiPerClockS LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

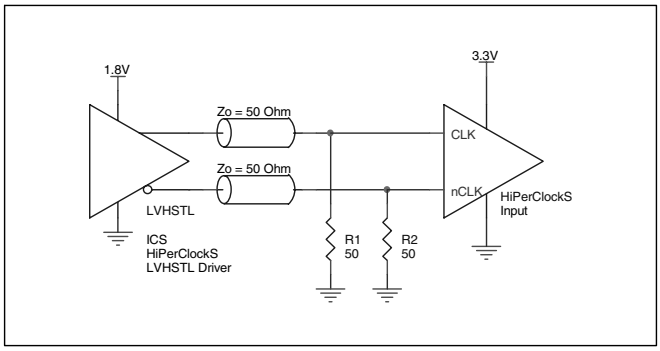


FIGURE 3A. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY ICS HIPERCLOCKS LVHSTL DRIVER

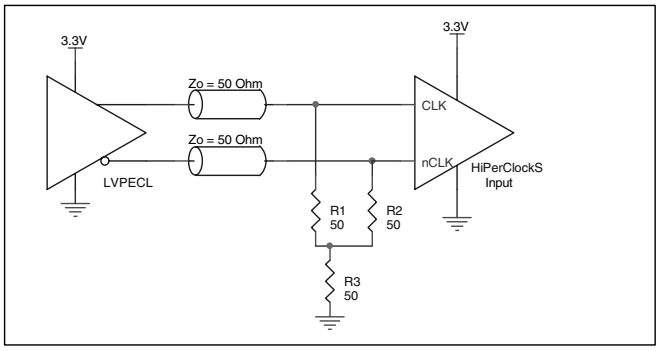


FIGURE 3B. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER

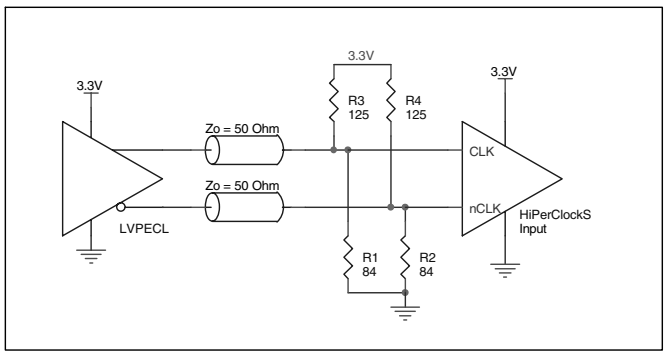


FIGURE 3C. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER

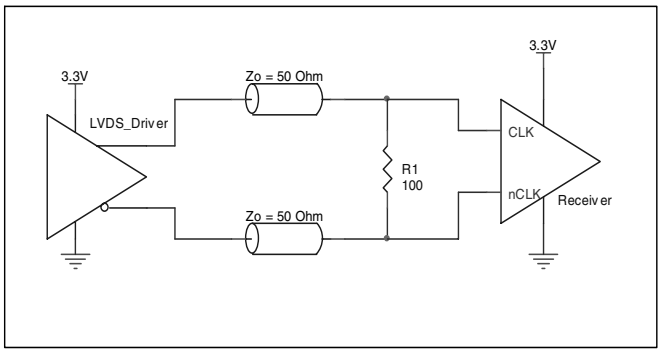


FIGURE 3D. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY 3.3V LVDS DRIVER

RELIABILITY INFORMATION

TABLE 6. θ_{JA} VS. AIR FLOW TABLE FOR 24 LEAD TSSOP

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Multi-Layer PCB, JEDEC Standard Test Boards	70°C/W	63°C/W	60°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS87004 is: 2578

PACKAGE OUTLINE - G SUFFIX FOR 24 LEAD TSSOP

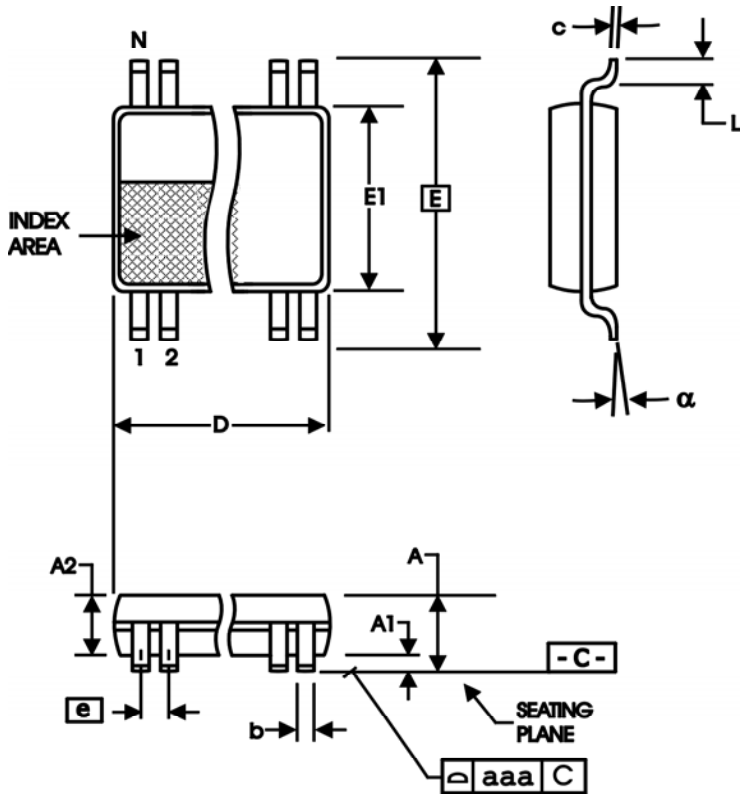


TABLE 7. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	24	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	7.70	7.90
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 8. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS87004AG	ICS87004AG	24 Lead TSSOP	60 per tube	0°C to 70°C
ICS87004AGT	ICS87004AG	24 Lead TSSOP on Tape and Reel	2500	0°C to 70°C
ICS87004AG	ICS87004AG	24 Lead "Lead Free" TSSOP	60 per tube	0°C to 70°C
ICS87004AGT	ICS87004AG	24 Lead "Lead Free" TSSOP on Tape and Reel	2500	0°C to 70°C

REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
A	T8	13	Ordering Information table - added "Lead-Free" part number.	6/16/04