PRELIMINARY

Integrated Circuit Systems, Inc.

ICS874004
PCI EXPRESS™ JITTER ATTENUATOR

GENERAL DESCRIPTION

ICS HiPerClockS™

The ICS874004 is a high performance Differential-to HCSL Jitter Attenuator designed for use in PCI Express™ systems. In some PCI Express™ systems, such as those found in desktop PCs, the PCI Express™ clocks are generated from a low bandwidth, highphase noise PLL frequency synthesizer. In these systems, a jitter attenuator may be required to attenuate high frequency random and deterministic jitter components from the PLL synthesizer and from the system board. The ICS874004 has 3 PLL bandwidth modes: 200KHz, 400KHz, and 800KHz. 200KHz mode will provide maximum jitter attenuation, but with higher PLL tracking skew and spread spectrum modulation from the motherboard synthesizer may be attenuated. 400KHz provides an intermediate bandwidth that can easily track triangular spread profiles, while providing good jitter attenuation. 800KHz bandwidth provides the best tracking skew and will pass most spread profiles, but the jitter attenuation will not be as good as the lower bandwidth modes. Because some 2.5 Gb serdes have x20 multipliers while others have than x25 multipliers, the 874004 can be set for 1:1 mode or 5/4 multiplication mode (i.e. 100MHz input/125MHz output) using the F_SEL pin.

The ICS874004 uses ICS 3rd Generation FemtoClock™ PLL technology to achieve the lowest possible phase noise. The device is packaged in a 24 Lead TSSOP package, making it ideal for use in space constrained applications such as PCI Express™ add-in cards.

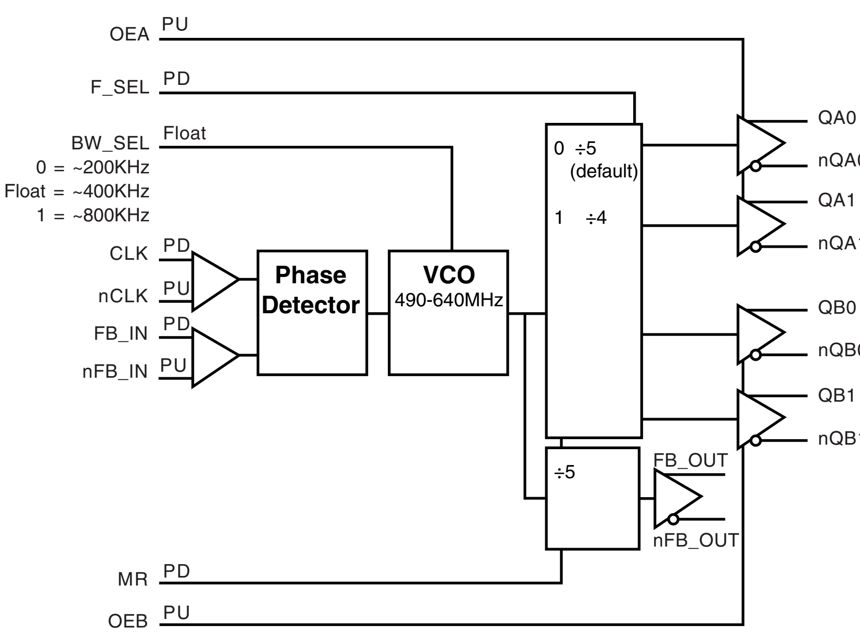
Features

- (4) Differential LVDS output pairs
- (1) Differential clock input
- CLK and nCLK supports the following input types: LVPECL, LVDS, LVHSTL, SSTL, HCSL
- Output frequency range: 98MHz - 160MHz
- Input frequency range: 98MHz - 128MHz
- VCO range: 490MHz - 640MHz
- Cycle-to-cycle jitter: 50ps (maximum) design target
- 3.3V operating supply
- 3 bandwidth modes allow the system designer to make jitter attenuation/tracking skew design trade-offs
- 0°C to 70°C ambient operating temperature

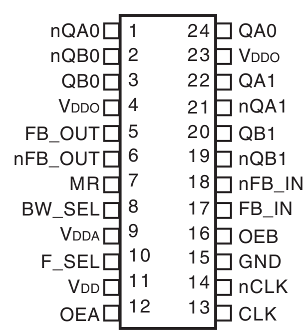
PLL BANDWIDTH

BW_SEL
0 = PLL Bandwidth: ~200KHz
Float = PLL Bandwidth: ~400KHz (Default)
1 = PLL Bandwidth: ~800KHz

BLOCK DIAGRAM



PIN ASSIGNMENT



ICS874004
24-Lead TSSOP
4.40mm x 7.8mm x 0.92mm package body
G Package
Top View

The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 24	nQA0, QA0	Output		Differential output pair. LVDS interface levels.
2, 3	nQB0, QB0	Output		Differential output pair. LVDS interface levels.
4, 23	V_{DDO}	Power		Output supply pins.
5	FB_OUT	Output		Non-inverting differential feedback output.
6	nFB_OUT	Output		Inverting differential feedback output.
7	MR	Input	Pulldown	Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs (nQx) to go low and the inverted outputs (Qx) to go high. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels.
8	BW_SEL	Input	Pullup/ Pulldown	Selects PLL Band Width input. LVCMOS/LVTTL interface levels.
9	V_{DDA}	Power		Analog supply pin.
10	F_SEL	Input	Pulldown	Frequency select pin. LVCMOS/LVTTL interface levels.
11	V_{DD}	Power		Core supply pin.
12	OEA	Input	Pullup	Output enable pin for QA pins. When HIGH, the QAx/nQAx outputs are active. When LOW, the QAx/nQAx outputs are in a high impedance state. LVCMOS/LVTTL interface levels.
13	CLK	Input	Pulldown	Non-inverting differential clock input.
14	nCLK	Input	Pullup	Inverting differential clock input.
15	GND	Power		Power supply ground.
16	OEB	Input	Pullup	Output enable pin for QB pins. When HIGH, the QBx/nQBx outputs are active. When LOW, the QBx/nQBx outputs are in a high impedance state. LVCMOS/LVTTL interface levels.
17	FB_IN	Input	Pulldown	Non-inverting differential feedback input.
18	nFB_IN	Input	Pullup	Inverting differential feedback input.
19, 20	nQB1, QB1	Output		Differential output pair. LVDS interface levels.
21, 22	nQA1, QA1	Output		Differential output pair. LVDS interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		KΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		KΩ

TABLE 3A. OUTPUT ENABLE FUNCTION TABLE

Inputs		Outputs		
OEA	OEB	QAx/nQAx	QBx/nQBx	FB_OUT/nFB_OUT
0	0	HiZ	HiZ	Enabled
1	1	Enabled	Enabled	Enabled

TABLE 3B. PLL BANDWIDTH/PLL BYPASS CONTROL

Inputs	PLL Bandwidth
BW_SEL	
0	~200KHz
1	~800KHz
Float	~400KHz

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, V_O	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA}	70°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO}$ = 3.3V±5%, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current			60		mA
I_{DDA}	Analog Supply Current			8		mA
I_{DDO}	Output Supply Current			82		mA

TABLE 4B. LVCMOS/LVTTL DC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO}$ = 3.3V±5%, TA = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	F_SEL, MR, OEA, OEB		2		V_{DD} + 0.3	V
		BW_SEL		V_{DD} - 0.3		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	F_SEL, MR, OEA, OEB		-0.3		0.8	V
		BW_SEL		-0.3		0.3	V
I_{IH}	Input High Current	BW_SEL, OEA, OEB	$V_{DD} = V_{IN}$ = 3.465V			5	µA
		F_SEL, MR	$V_{DD} = V_{IN}$ = 3.465V			150	µA
I_{IL}	Input Low Current	BW_SEL, OEA, OEB	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
		F_SEL, MR	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA

TABLE 4C. DIFFERENTIAL DC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO}$ = 3.3V±5%, TA = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK, FB_IN	$V_{DD} = V_{IN}$ = 3.465V			150	µA
		nCLK, nFB_IN	$V_{DD} = V_{IN}$ = 3.465V	5			µA
I_{IL}	Input Low Current	CLK, FB_IN	$V_{DD} = V_{IN}$ = 3.465V			150	µA
		nCLK, nFB_IN	$V_{DD} = V_{IN}$ = 3.465V	-150			µA
V_{PP}	Peak-to-Peak Input Voltage			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			GND + 0.5		V_{DD} - 0.85	V

NOTE 1: Common mode voltage is defined as V_{IH}.
NOTE 2: For single ended applications, the maximum input voltage for CLK, nCLK and FB_IN, nFB_IN is V_{DD} + 0.3V.

TABLE 4D. LVDS DC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$, $T_A = 0°C$ TO $70°C$

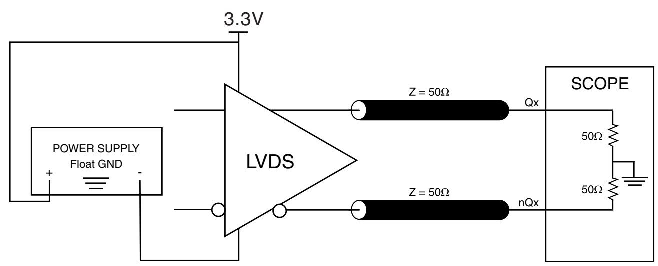
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage			350		mV
ΔV_{OD}	V_{OD} Magnitude Change			50		mV
V_{OS}	Offset Voltage			1.35		V
ΔV_{OS}	V_{OS} Magnitude Change			50		mV

TABLE 5. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$, $T_A = 0°C$ TO $70°C$

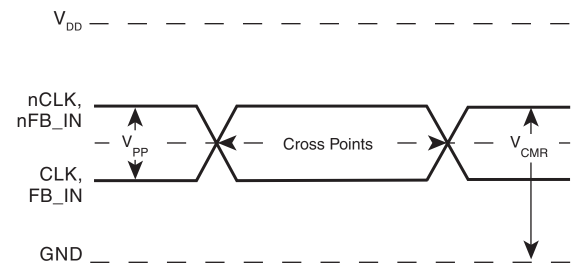
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency		98		160	MHz
*t*jit(cc)	Cycle-to-Cycle Jitter, NOTE 1			13		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%		330		ps
odc	Output Duty Cycle			50		%

NOTE 1: This parameter is defined in accordance with JEDEC Standard 65.

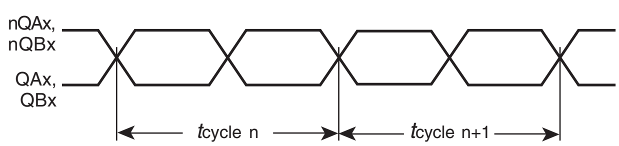
PARAMETER MEASUREMENT INFORMATION



3.3V LVDS OUTPUT LOAD AC TEST CIRCUIT



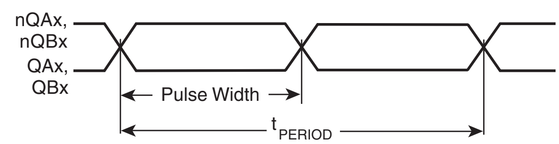
DIFFERENTIAL INPUT LEVEL



$$t_{jit(cc)} = t_{cycle\ n} - t_{cycle\ n+1}$$

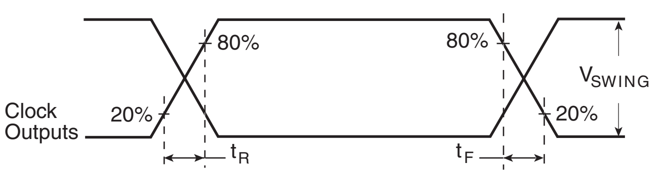
1000 Cycles

CYCLE-TO-CYCLE JITTER

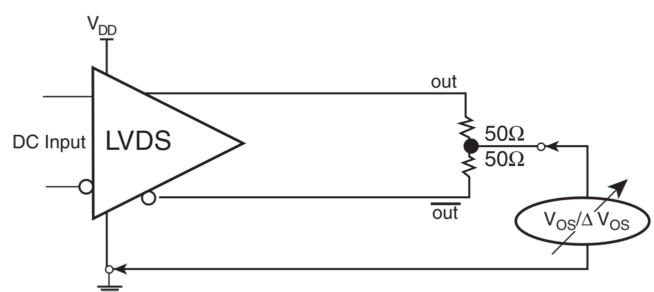


$$odc = \frac{t_{PW}}{t_{PERIOD}}$$

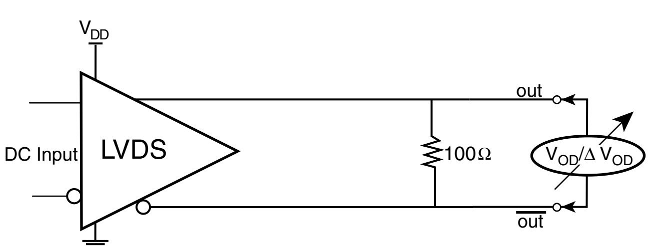
OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



OUTPUT RISE/FALL TIME



OFFSET VOLTAGE SETUP



DIFFERENTIAL OUTPUT VOLTAGE SETUP

APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS874004 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD}, V_{DDA}, and V_{DDO} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a 10µF and a .01µF bypass capacitor should be connected to each V_{DDA} pin.

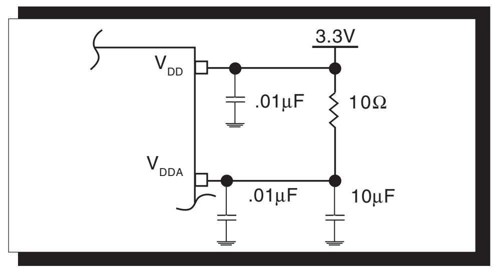


FIGURE 1. POWER SUPPLY FILTERING

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 2 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = $V_{DD}/2$ is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

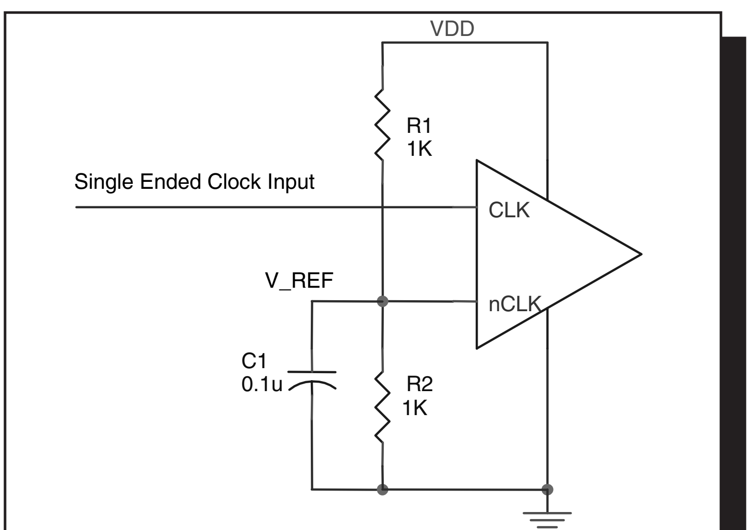


FIGURE 2. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

DIFFERENTIAL CLOCK INPUT INTERFACE

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. Figures 3A to 3D show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in *Figure 3A,* the input termination applies for ICS HiPerClockS LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

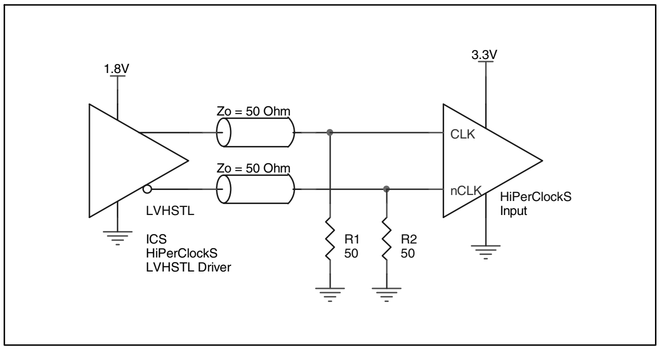


FIGURE 3A. HIPERCLOCKS CLK/nCLK INPUT DRIVEN BY ICS HIPERCLOCKS LVHSTL DRIVER

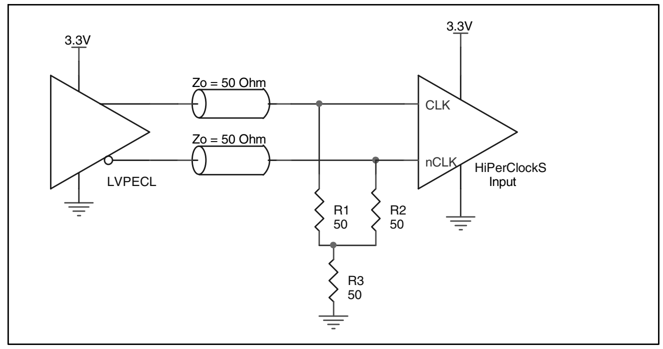


FIGURE 3B. HIPERCLOCKS CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER

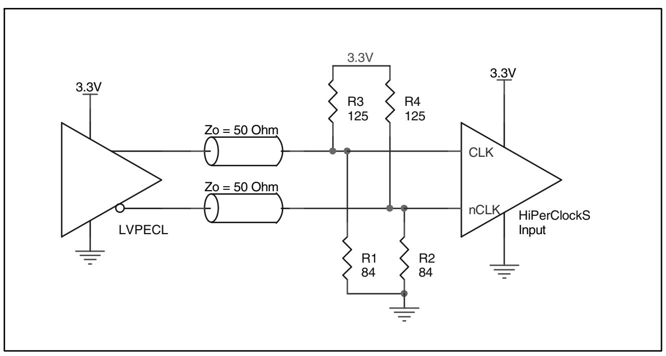


FIGURE 3C. HIPERCLOCKS CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER

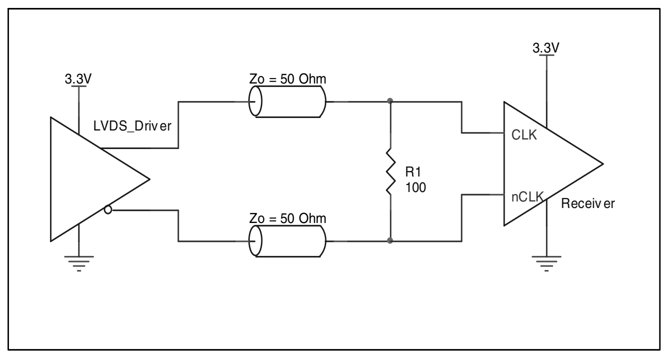


FIGURE 3D. HIPERCLOCKS CLK/nCLK INPUT DRIVEN BY 3.3V LVDS DRIVER

LVDS DRIVER TERMINATION

A general LVDS interface is shown in *Figure 4.* In a 100Ω differential transmission line environment, LVDS drivers require a matched load termination of 100Ω across near the receiver input. For a multiple LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the un-used outputs.

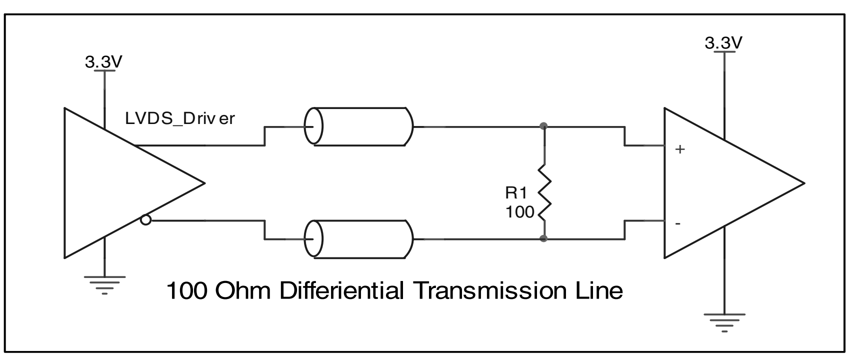


FIGURE 4. TYPICAL LVDS DRIVER TERMINATION

RELIABILITY INFORMATION

TABLE 6. θ_{JA} VS. AIR FLOW TABLE FOR 24 LEAD TSSOP

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Multi-Layer PCB, JEDEC Standard Test Boards	70°C/W	65°C/W	62°C/W

TRANSISTOR COUNT

The transistor count for ICS874004 is: 1216

PACKAGE OUTLINE - G SUFFIX FOR 24 LEAD TSSOP

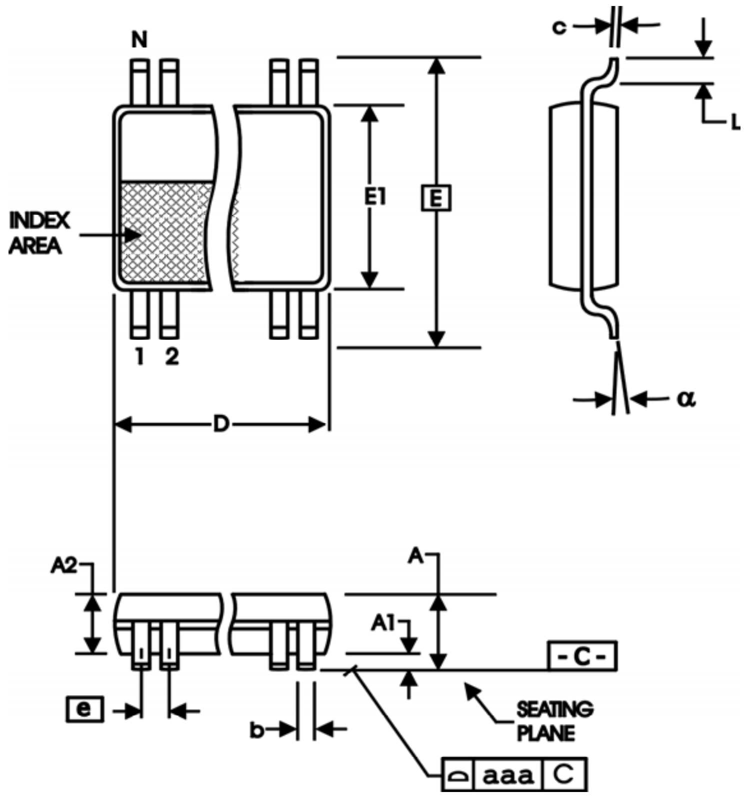


TABLE 7. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	24	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	7.70	7.90
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 8. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS874004AG	ICS874004AG	24 Lead TSSOP	tube	0°C to 70°C
ICS874004AGT	ICS874004AG	24 Lead TSSOP	2500 tape & reel	0°C to 70°C