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4AM11

Silicon N-Channel/P-Channel Power MOS FET Array

HITACHI

Application

High speed power switching

Features

- Low on-resistance
  N-channel: $R_{DS(on)}$ 0.17 , V_{GS} = 10 V, I_D = 2.5 A
  P-channel: $R_{DS(on)}$ 0.2 , V_{GS} = –10 V, I_D = –2.5 A
- Capable of 4 V gate drive
- Low drive current
- High speed switching
- High density mounting
- Suitable for H-bridged motor driver

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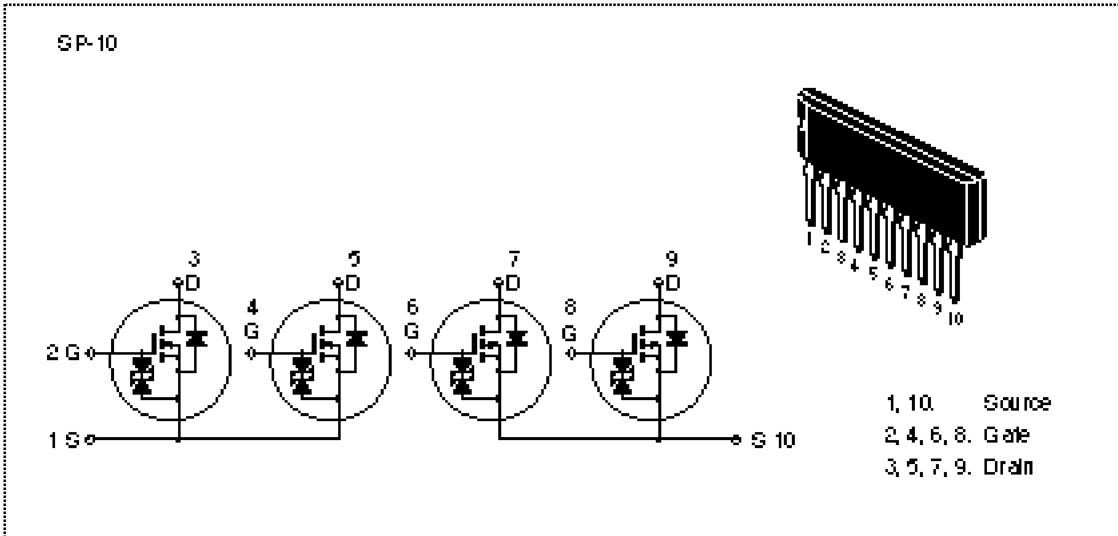
Outline



Absolute Maximum Ratings (Ta = 25°C) (1 Unit)

Item	Symbol	Rating		Unit
		Nch	Pch	
Drain to source voltage	V_{DSS}	60	–60	V
Gate to source voltage	V_{GSS}	±20	±20	V
Drain current	I_D	5	–5	A
Drain peak current	$I_{D(pulse)}$*1	20	–20	A
Body to drain diode reverse drain current	I_{DR}	5	–5	A
Channel dissipation	Pch (Tc = 25°C)*2	28		W
Channel dissipation	Pch*2	4		W
Channel temperature	Tch	150		°C
Storage temperature	Tstg	–55 to +150		°C

Notes: 1. PW 10 μs, duty cycle 1%
2. 4 Devices operation

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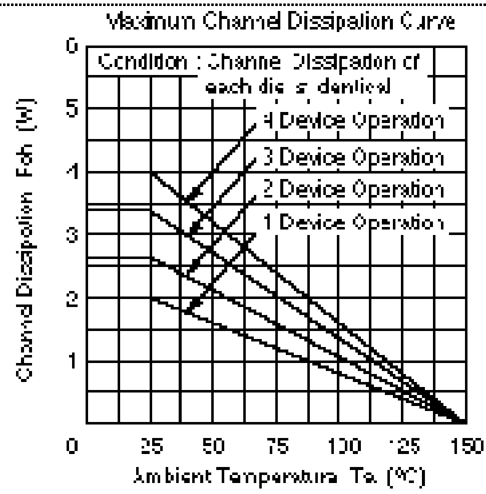
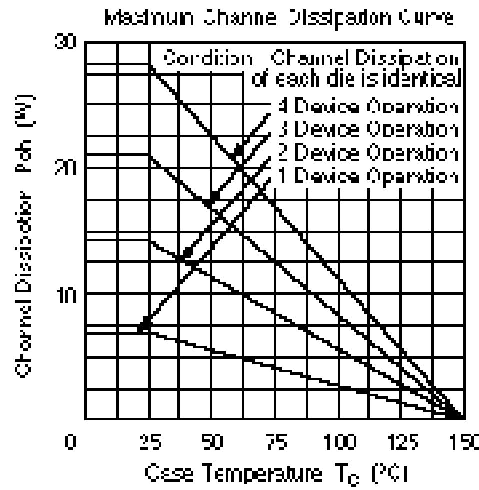
Electrical Characteristics (Ta = 25°C) (1 Unit)

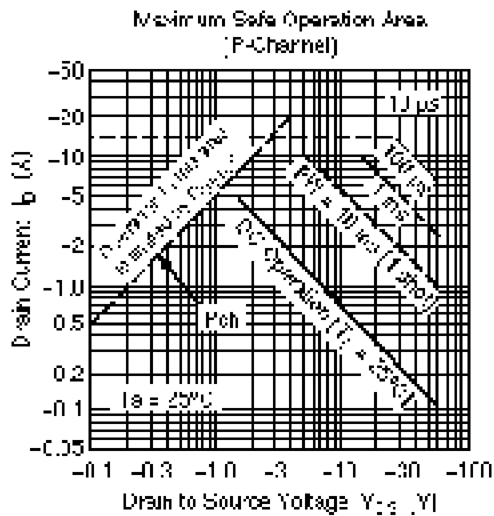
Item	Symbol	N channel Min	N channel Typ	N channel Max	P channel Min	P channel Typ	P channel Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	–60	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	±20	—	—	V	I_G = ±100 μA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	—	—	±10	μA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	—	—	–250	μA	V_{DS} = 50 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.0	–1.0	—	–2.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.13	0.17	—	0.15	0.2		I_D = 2.5 A, V_{GS} = 10 V*1
		—	0.18	0.24	—	0.20	0.27		I_D = 2.5 A, V_{GS} = 4 V*1
Forward transfer admittance	$\|y_{fs}\|$	2.7	4.5	—	2.7	5.0	—	S	I_D = 2.5 A, V_{DS} = 10 V*1
Input capacitance	Ciss	—	400	—	—	900	—	pF	V_{DS} = 10 V, V_{GS} = 0, f = 1 MHz
Output capacitance	Coss	—	220	—	—	460	—	pF	
Reverse transfer capacitance	Crss	—	60	—	—	130	—	pF	
Turn-on delay time	$t_{d(on)}$	—	5	—	—	8	—	ns	I_D = 2.5 A, V_{GS} = 10 V, R_L = 12
Rise time	t_r	—	30	—	—	35	—	ns	
Turn-off delay time	$t_{d(off)}$	—	170	—	—	180	—	ns	
Fall time	t_f	—	75	—	—	85	—	ns	
Body to drain diode forward voltage	V_{DF}	—	1.0	—	—	–1.0	—	V	I_F = 5 A, V_{GS} = 0
Body to drain diode reverse recovery time	t_{rr}	—	100	—	—	170	—	μs	I_F = 5 A, V_{GS} = 0, dIF/dt = 50 A/μs

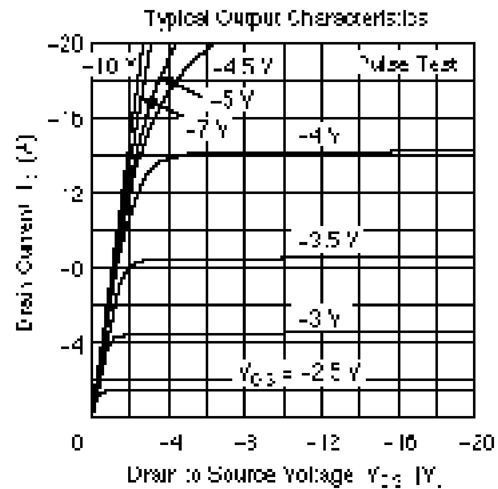
Note: 1. Pulse Test

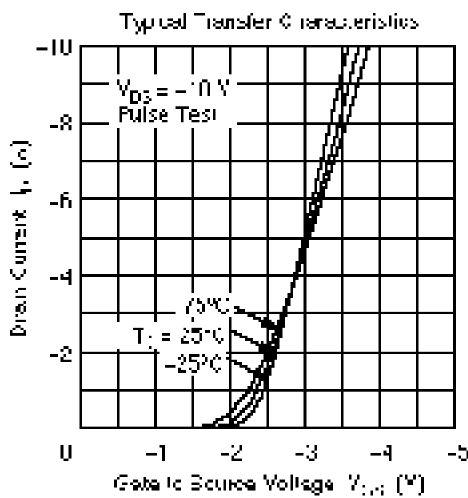
Polarity of test conditions for P channel device is reversed.

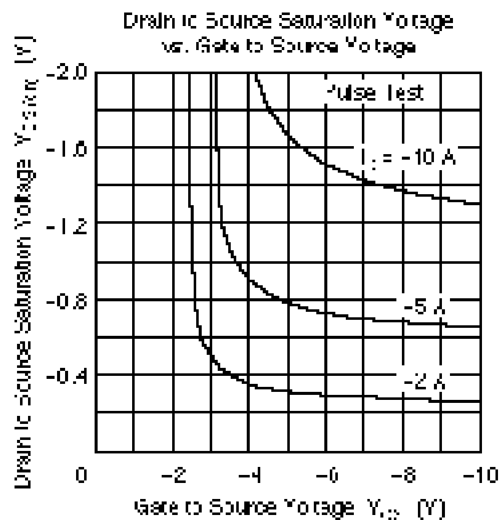

Maximum Channel Dissipation Curve
4 Device Operation
3 Device Operation
2 Device Operation
1 Device Operation
Channel Dissipation Pch (W)
0
1
2
3
4
5
6
25
50
75
100
125
150
Ambient Temperature Ta (°C)

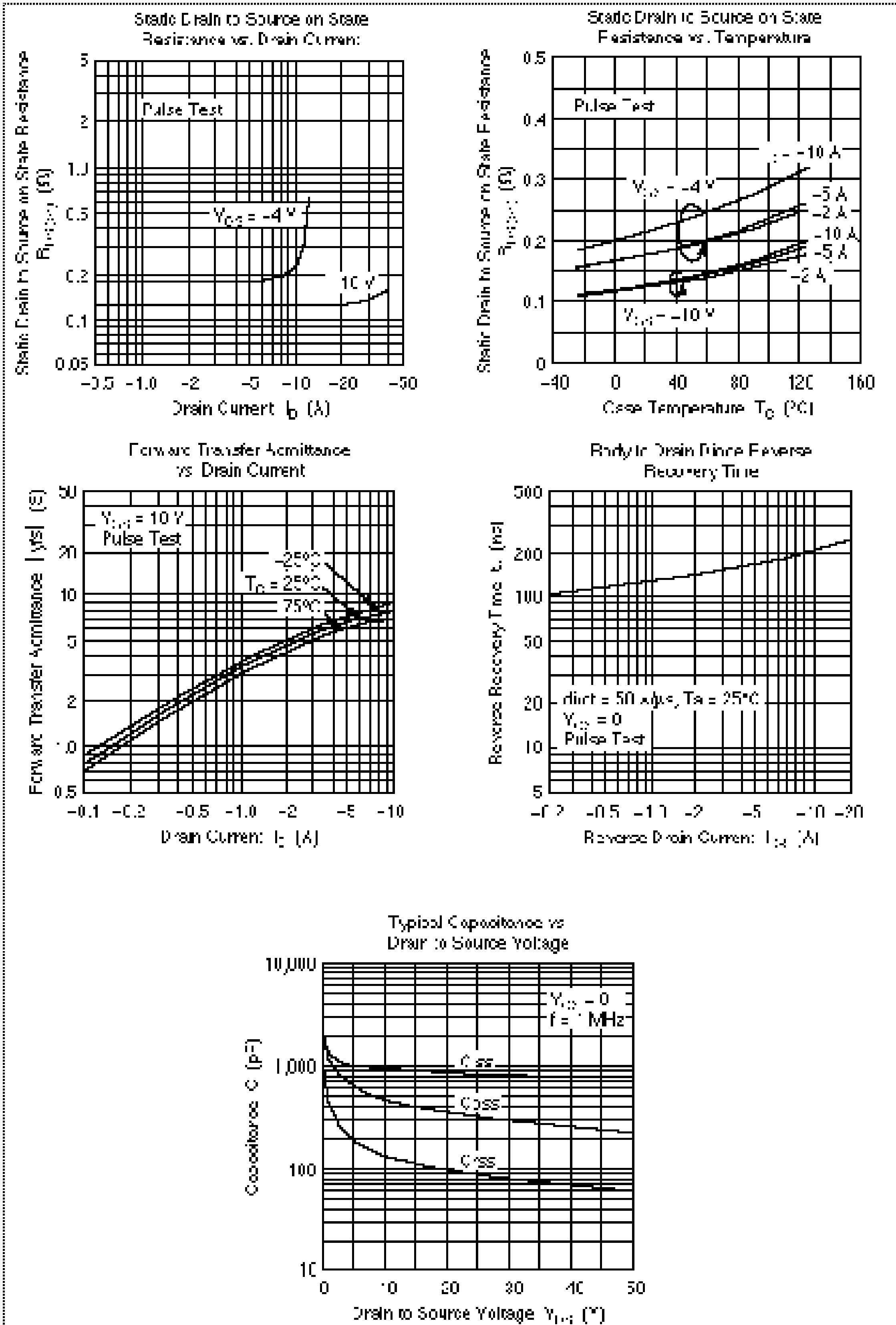

Maximum Channel Dissipation Curve
Condition : Channel Dissipation
of each die is identical
4 Device Operation
3 Device Operation
2 Device Operation
1 Device Operation
Channel Dissipation Pch (W)
30
20
10
0
25
50
75
100
125
150
Case Temperature Tc (°C)

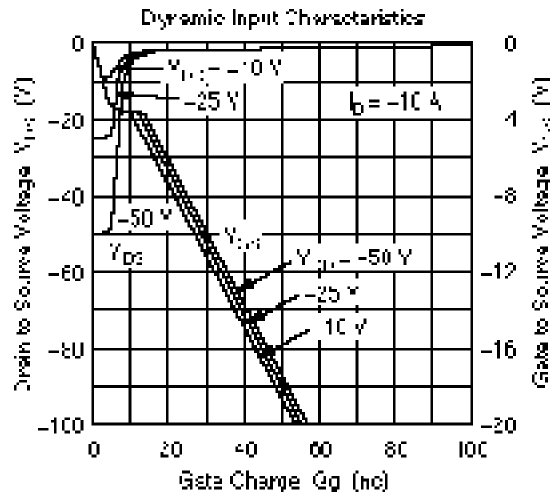

Maximum Safe Operation Area
(P-Channel)
10 µs
100 µs
Pch
Ta = 25°C
Drain Current ID (A)
−50
−20
−10
−5
−2
−1.0
0.5
0.2
−0.1
−0.05
−0.1
−0.3
−1.0
−3
−10
−30
−100
Drain to Source Voltage VDS (V)

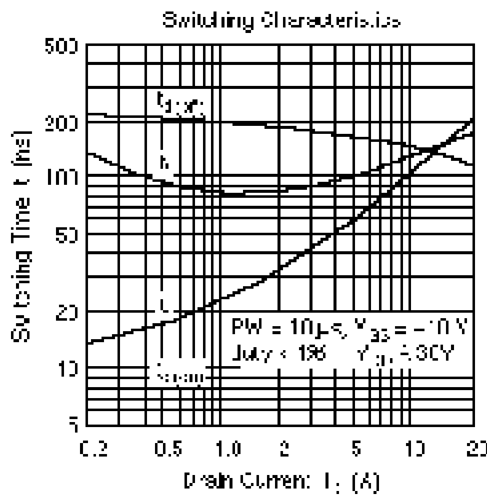

Typical Output Characteristics
−10 V
−4.5 V
Pulse Test
−5 V
−7 V
−4 V
−3.5 V
−3 V
VGS = −2.5 V
Drain Current ID (A)
−20
−16
−12
−8
−4
0
−4
−8
−12
−16
−20
Drain to Source Voltage VDS (V)

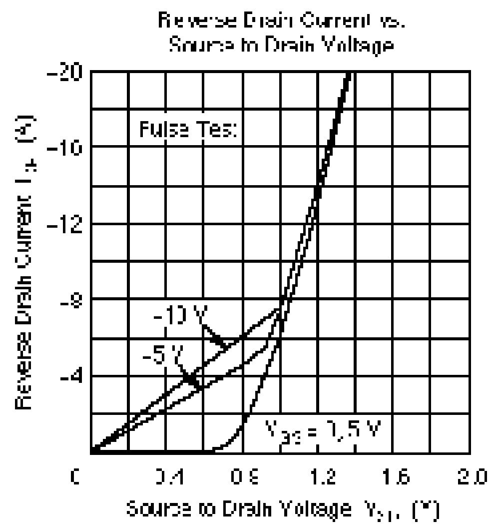

Typical Transfer Characteristics
VDS = −10 V
Pulse Test
75°C
Tc = 25°C
−25°C
Drain Current ID (A)
−10
−8
−6
−4
−2
0
−1
−2
−3
−4
−5
Gate to Source Voltage VGS (V)

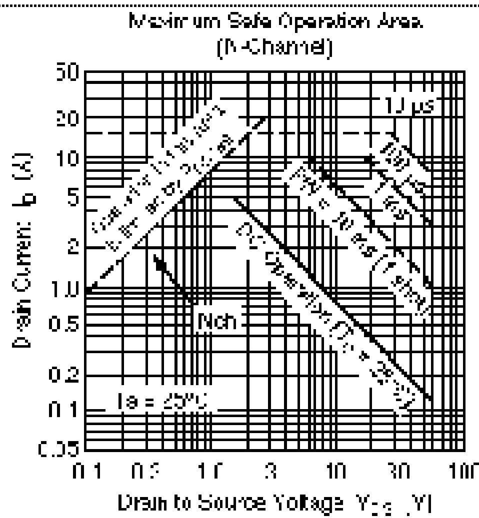

Drain to Source Saturation Voltage
vs. Gate to Source Voltage
Pulse Test
ID = −10 A
−5 A
−2 A
Drain to Source Saturation Voltage VDS(on) (V)
−2.0
−1.6
−1.2
−0.8
−0.4
0
−2
−4
−6
−8
−10
Gate to Source Voltage VGS (V)

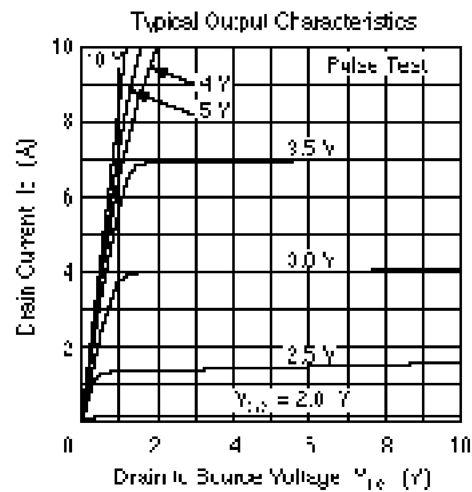

Static Drain to Source on State Resistance vs. Drain Current
Pulse Test
Static Drain to Source on State Resistance $R_{DS(on)}$ (Ω)
Drain Current I_D (A)
Static Drain to Source on State Resistance vs. Temperature
Pulse Test
Case Temperature T_C (°C)
Forward Transfer Admittance vs. Drain Current
Pulse Test
Forward Transfer Admittance |yfs| (S)
Drain Current I_D (A)
Body to Drain Diode Reverse Recovery Time
Reverse Recovery Time t_{rr} (ns)
Pulse Test
Reverse Drain Current I_{DR} (A)
Typical Capacitance vs Drain to Source Voltage
f = 1 MHz
Ciss
Coss
Crss
Capacitance C (pF)
Drain to Source Voltage V_{DS} (V)

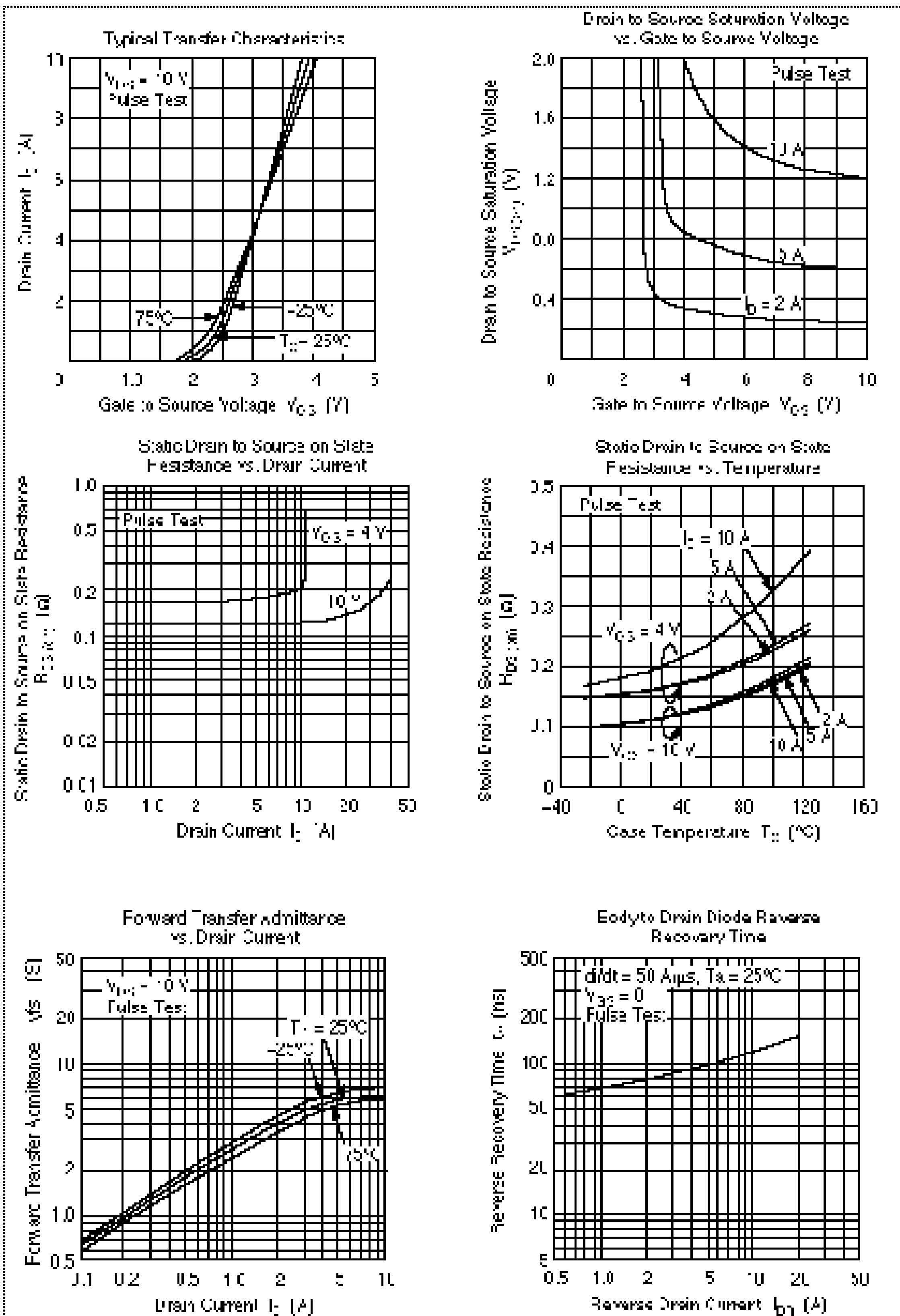

Dynamic Input Characteristics
Drain to Source Voltage V_{DS} (V)
Gate to Source Voltage V_{GS} (V)
Gate Charge Qg (nc)
$I_D = -10$ A
V_{DS}
V_{GS}

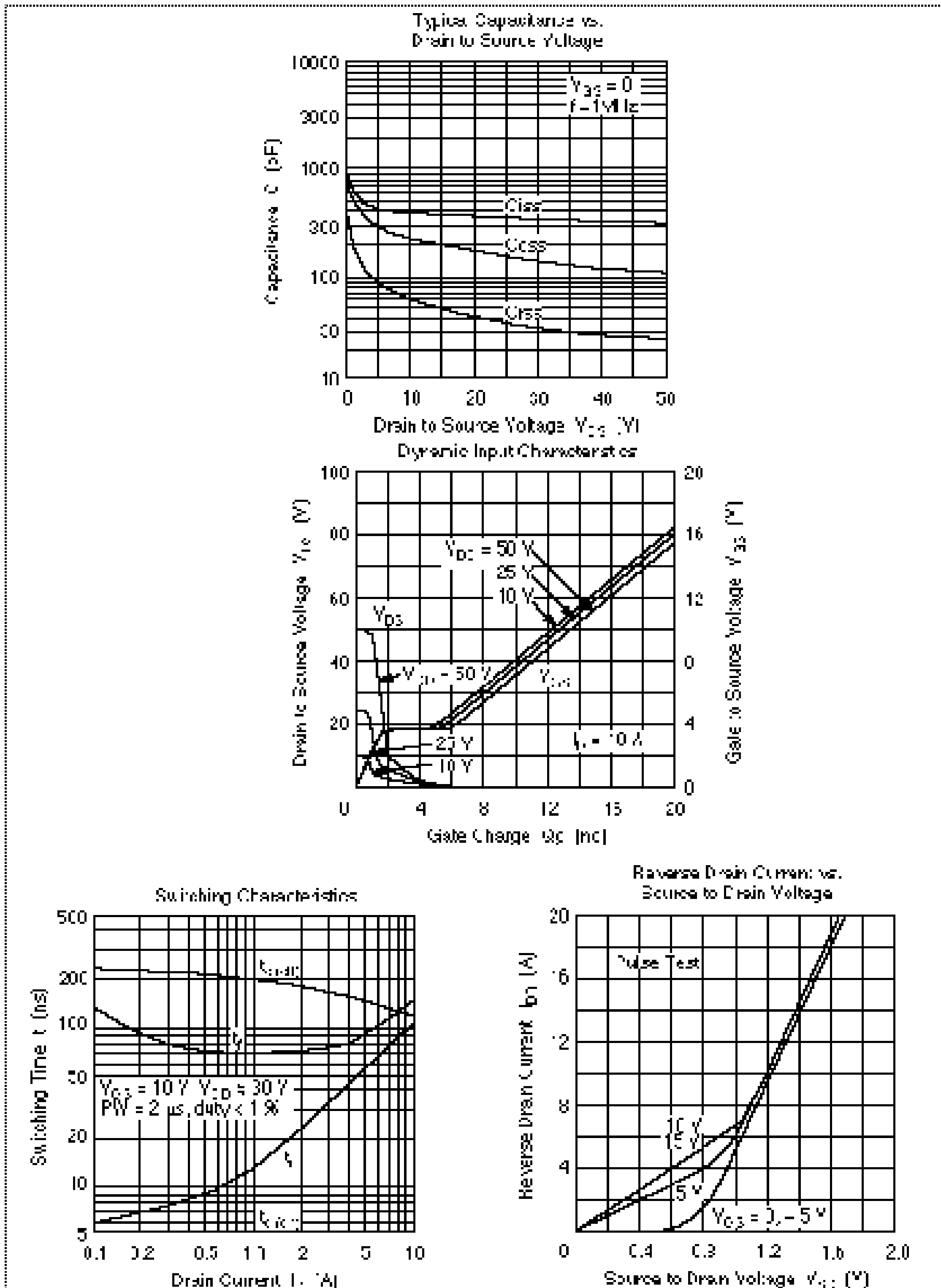

Switching Characteristics
Switching Time t (ns)
Drain Current I_D (A)
PW = 10 μs, $V_{GS} = -10$ V
duty ≤ 1%


Reverse Drain Current vs. Source to Drain Voltage
Reverse Drain Current I_{DR} (A)
Source to Drain Voltage V_{SD} (V)
Pulse Test


Maximum Safe Operation Area (N-Channel)
Drain Current I_D (A)
Drain to Source Voltage V_{DS} (V)
Nch
Ta = 25°C


Typical Output Characteristics
Drain Current I_D (A)
Drain to Source Voltage V_{DS} (V)
Pulse Test
3.5 V
3.0 V
2.5 V
$V_{GS} = 2.0$ V


Typical Transfer Characteristics
Gate to Source Voltage V_{GS} (V)
Drain Current I_D (A)
Pulse Test
75°C
−25°C
Drain to Source Saturation Voltage vs. Gate to Source Voltage
Pulse Test
Gate to Source Voltage V_{GS} (V)
Static Drain to Source on State Resistance vs. Drain Current
Pulse Test
Drain Current I_D (A)
Static Drain to Source on State Resistance vs. Temperature
Pulse Test
Case Temperature
Forward Transfer Admittance vs. Drain Current
Pulse Test
Drain Current I_D (A)
Bodyto Drain Diode Reverse Recovery Time
di/dt = 50 A/μs, Ta = 25°C
Pulse Test
Reverse Drain Current


Typical Capacitance vs. Drain to Source Voltage
Capacitance C (pF)
Drain to Source Voltage V_{DS} (V)
V_{GS} = 0
f = 1 MHz
Ciss
Coss
Crss
Dynamic Input Characteristics
Drain to Source Voltage V_{DS} (V)
Gate to Source Voltage V_{GS} (V)
Gate Charge Qg (nc)
V_{DD} = 50 V
25 V
10 V
V_{DS}
V_{GS}
I_D = 10 A
Switching Characteristics
Switching Time t (ns)
Drain Current I_D (A)
V_{GS} = 10 V, V_{DD} ≒ 30 V
PW = 2 µs, duty < 1 %
$t_{d(off)}$
t_f
t_r
$t_{d(on)}$
Reverse Drain Current vs. Source to Drain Voltage
Reverse Drain Current I_{DR} (A)
Source to Drain Voltage V_{SD} (V)
Pulse Test
10 V
15 V
5 V
V_{GS} = 0, –5 V

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