



Integrated Device Technology, Inc.

### 3.3V CMOS 16-BIT BUFFER/LINE DRIVER

IDT74FCT163244/A/C

#### FEATURES:

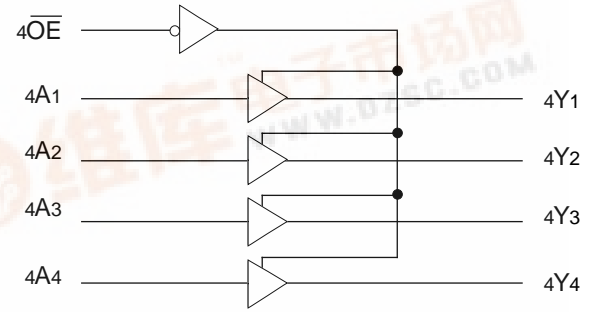
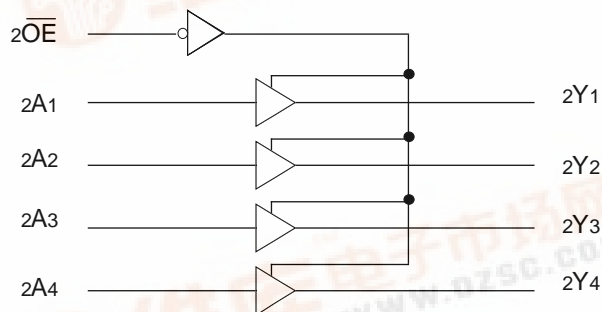
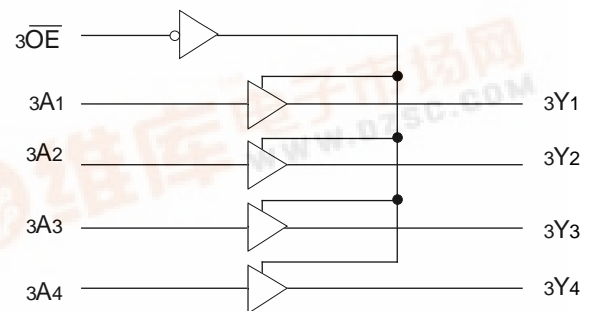
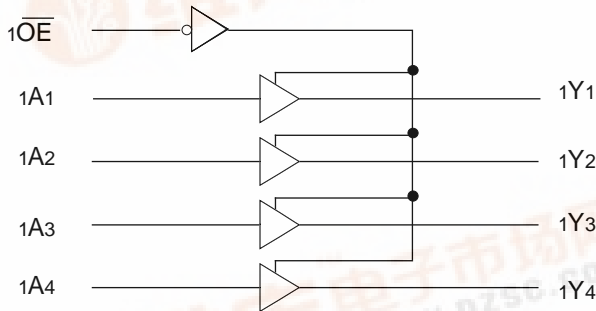
- 0.5 MICRON CMOS Technology
- **Typical tsk(o) (Output Skew) < 250ps**
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- Packages include 25 mil pitch SSOP, 19.6 mil pitch TSSOP and 15.7 mil pitch TVSOP
- Extended commercial range of -40°C to +85°C
- Vcc = 3.3V ±0.3V, Normal Range or Vcc = 2.7 to 3.6V, Extended Range
- CMOS power levels (0.4μW typ. static)
- Rail-to-Rail output swing for increased noise margin
- Low Ground Bounce (0.3V typ.)
- Inputs (except I/O) can be driven by 3.3V or 5V components

#### DESCRIPTION:

The FCT163244/A/C 16-bit buffer/line drivers are built using advanced dual metal CMOS technology. These high-speed, low-power devices offer bus/backplane interface capability with improved packing density. These devices have a flow-through organization for simplifying board layout. The three-state controls operate these devices in a Quad-Nibble, Dual-Byte or single 16-bit word mode. All inputs are designed with hysteresis for improved noise margin.

The inputs of the FCT163244/A/C can be driven from either 3.3V or 5V devices. This feature allows the use of these devices as translators in a mixed 3.3V/5V supply system. Thus, the FCT163244/A/C can be used as buffers to connect 5V components to a 3.3V bus.

#### FUNCTIONAL BLOCK DIAGRAM

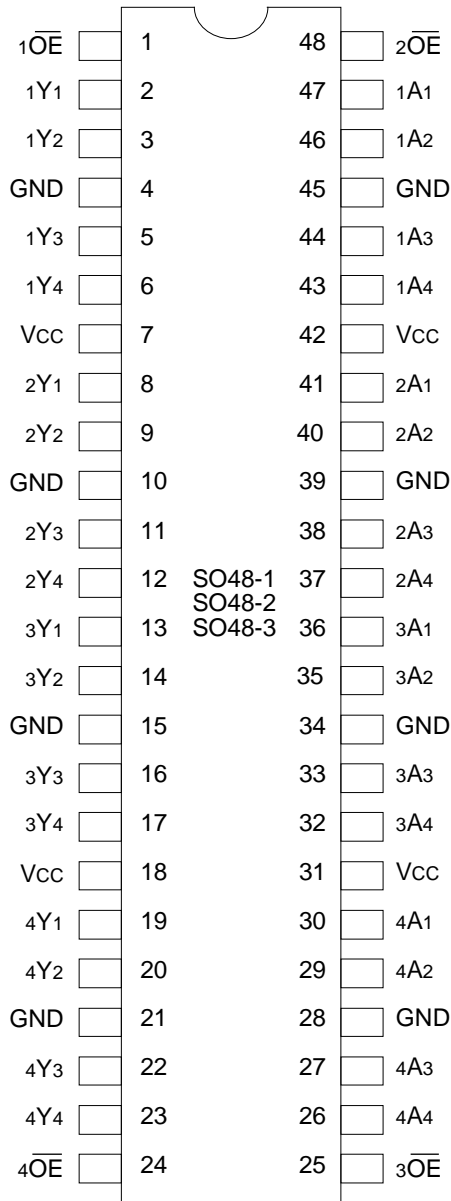


2532 drw 01

2532 drw 02



## PIN CONFIGURATIONS



SSOP/  
TSSOP/TVSOP  
TOP VIEW

2532 drw 03

## PIN DESCRIPTION

Pin Names	Description
$\overline{xOE}$	3-State Output Enable Inputs (Active LOW)
$xAx$	Data Inputs
$xYx$	3-State Outputs

2532 tbl 01

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Description	Max.	Unit
$V_{TERM}^{(2)}$	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
$V_{TERM}^{(3)}$	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
$V_{TERM}^{(4)}$	Terminal Voltage with Respect to GND	-0.5 to $V_{CC} + 0.5$	V
TSTG	Storage Temperature	-65 to +150	°C
IOUT	DC Output Current	-60 to +60	mA

### NOTES:

2532 lmk 03

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- Vcc terminals.
- Input terminals.
- Output and I/O terminals.

## CAPACITANCE ( $T_A = +25^\circ\text{C}$ , $f = 1.0\text{MHz}$ )

Symbol	Parameter <sup>(1)</sup>	Conditions	Typ.	Max.	Unit
CIN	Input Capacitance	$V_{IN} = 0V$	3.5	6.0	pF
COUT	Output Capacitance	$V_{OUT} = 0V$	3.5	8.0	pF

### NOTE:

2532 lmk 04

- This parameter is measured at characterization but not tested.

## FUNCTION TABLE<sup>(1)</sup>

Inputs		Outputs
$\overline{xOE}$	$xAx$	$xYx$
L	L	L
L	H	H
H	X	Z

### NOTE:

2532 tbl 02

- H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Don't Care  
Z = High Impedance

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:  
Commercial:  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{CC} = 2.7\text{V}$  to  $3.6\text{V}$

Symbol	Parameter	Test Conditions <sup>(1)</sup>	Min.	Typ. <sup>(2)</sup>	Max.	Unit	
$V_{IH}$	Input HIGH Level (Input pins)	Guaranteed Logic HIGH Level	2.0	—	5.5	V	
	Input HIGH Level (I/O pins)		2.0	—	$V_{CC}+0.5$		
$V_{IL}$	Input LOW Level (Input and I/O pins)	Guaranteed Logic LOW Level	-0.5	—	0.8	V	
$I_{IH}$	Input HIGH Current (Input pins)	$V_{CC} = \text{Max.}$	$V_I = 5.5\text{V}$	—	—	$\pm 1$	$\mu\text{A}$
	Input HIGH Current (I/O pins)		$V_I = V_{CC}$	—	—	$\pm 1$	
$I_{IL}$	Input LOW Current (Input pins)		$V_I = \text{GND}$	—	—	$\pm 1$	
	Input LOW Current (I/O pins)		$V_I = \text{GND}$	—	—	$\pm 1$	
$I_{OZH}$	High Impedance Output Current (3-State Output pins)	$V_{CC} = \text{Max.}$	$V_O = V_{CC}$	—	—	$\pm 1$	$\mu\text{A}$
$I_{OZL}$			$V_O = \text{GND}$	—	—	$\pm 1$	
$V_{IK}$	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}$	—	-0.7	-1.2	V	
$I_{ODH}$	Output HIGH Current	$V_{CC} = 3.3\text{V}, V_{IN} = V_{IH}$ or $V_{IL}, V_O = 1.5\text{V}^{(3)}$	-36	-60	-110	$\text{mA}$	
$I_{ODL}$	Output LOW Current	$V_{CC} = 3.3\text{V}, V_{IN} = V_{IH}$ or $V_{IL}, V_O = 1.5\text{V}^{(3)}$	50	90	200	$\text{mA}$	
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -0.1\text{mA}$	$V_{CC}-0.2$	—	—	V
			$I_{OH} = -3\text{mA}$	2.4	3.0	—	
		$V_{CC} = 3.0\text{V}$ $V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -8\text{mA}$	2.4 <sup>(5)</sup>	3.0	—	
$V_{OL}$	Output LOW Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 0.1\text{mA}$	—	—	0.2	V
			$I_{OL} = 16\text{mA}$	—	0.2	0.4	
			$I_{OL} = 24\text{mA}$	—	0.3	0.55	
		$V_{CC} = 3.0\text{V}$ $V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 24\text{mA}$	—	0.3	0.50	
$I_{OS}$	Short Circuit Current <sup>(4)</sup>	$V_{CC} = \text{Max.}, V_O = \text{GND}^{(3)}$	-60	-135	-240	$\text{mA}$	
$V_H$	Input Hysteresis	—	—	150	—	$\text{mV}$	
$I_{CCL}$ $I_{CCH}$ $I_{CCZ}$	Quiescent Power Supply Current	$V_{CC} = \text{Max.},$ $V_{IN} = \text{GND}$ or $V_{CC}$	—	0.1	10	$\mu\text{A}$	

### NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at  $V_{CC} = 3.3\text{V}, +25^{\circ}\text{C}$  ambient.
- Not more than one output should be tested at one time. Duration of the test should not exceed one second.
- This parameter is guaranteed but not tested.
- $V_{OH} = V_{CC} - 0.6\text{V}$  at rated current.

## POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Typ. <sup>(2)</sup>	Max.	Unit
$\Delta I_{CC}$	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$	$V_{IN} = V_{CC} - 0.6V^{(3)}$	—	2.0	30	$\mu A$
$I_{CCD}$	Dynamic Power Supply Current <sup>(4)</sup>	$V_{CC} = \text{Max.}$ Outputs Open 50% Duty Cycle $\overline{xOE} = \text{GND}$ One Input Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	50	75	$\mu A / \text{MHz}$
$I_C$	Total Power Supply Current <sup>(6)</sup>	$V_{CC} = \text{Max.}$ Outputs Open $f_i = 10\text{MHz}$ 50% Duty Cycle $\overline{xOE} = \text{GND}$ One Bit Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	0.5	0.8	mA
			$V_{IN} = V_{CC} - 0.6V$ $V_{IN} = \text{GND}$	—	0.5	0.8	
		$V_{CC} = \text{Max.}$ Outputs Open $f_i = 2.5\text{MHz}$ 50% Duty Cycle $\overline{xOE} = \text{GND}$ Sixteen Bits Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	2.0	3.0 <sup>(5)</sup>	
			$V_{IN} = V_{CC} - 0.6V$ $V_{IN} = \text{GND}$	—	2.0	3.3 <sup>(5)</sup>	

### NOTES:

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- For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at  $V_{CC} = 3.3V$ ,  $+25^\circ C$  ambient.
- Per TTL driven input; all other inputs at  $V_{CC}$  or  $\text{GND}$ .
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the  $I_{CC}$  formula. These limits are guaranteed but not tested.
- $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$   
 $I_C = I_{CC} + \Delta I_{CC} \text{ DHNT} + I_{CCD} (f_{CP} \text{NCP}/2 + f_i \text{Ni})$   
 $I_{CC} = \text{Quiescent Current (IcCL, IcCH and Iccz)}$   
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input}$   
 $\text{DH} = \text{Duty Cycle for TTL Inputs High}$   
 $\text{NT} = \text{Number of TTL Inputs at DH}$   
 $I_{CCD} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$   
 $f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$   
 $\text{NCP} = \text{Number of Clock Inputs at } f_{CP}$   
 $f_i = \text{Input Frequency}$   
 $\text{Ni} = \text{Number of Inputs at } f_i$

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE<sup>(4)</sup>

Symbol	Parameter	Condition <sup>(1)</sup>	FCT163244		FCT163244A		FCT163244C		Unit
			Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	
$t_{PLH}$ $t_{PHL}$	Propagation Delay $xAx$ to $xYx$	$CL = 50\text{pF}$ $RL = 500\Omega$	1.5	6.5	1.5	4.8	1.5	4.1	ns
$t_{PZH}$ $t_{PZL}$	Output Enable Time		1.5	8.0	1.5	6.2	1.5	5.8	ns
$t_{PHZ}$ $t_{PLZ}$	Output Disable Time		1.5	7.0	1.5	5.6	1.5	5.2	ns
$t_{SK}(0)$	Output Skew <sup>(3)</sup>		—	0.5	—	0.5	—	0.5	ns

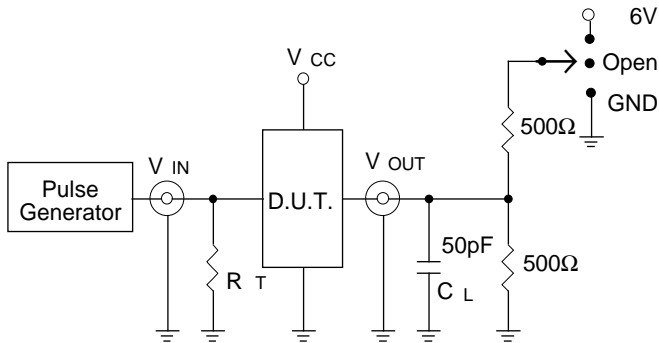
### NOTES:

2532 tbl 07

- See test circuit and waveforms.
- Minimum limits are guaranteed but not tested on Propagation Delays.
- Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.
- Propagation Delays and Enable/Disable times are with  $V_{CC} = 3.3V \pm 0.3V$ , Normal Range. For  $V_{CC} = 2.7V$  to  $3.6V$ , Extended Range, all Propagation Delays and Enable/Disable times should be degraded by 20%.

## TEST CIRCUITS AND WAVEFORMS

### TEST CIRCUITS FOR ALL OUTPUTS



2532 drw 05

### SWITCH POSITION

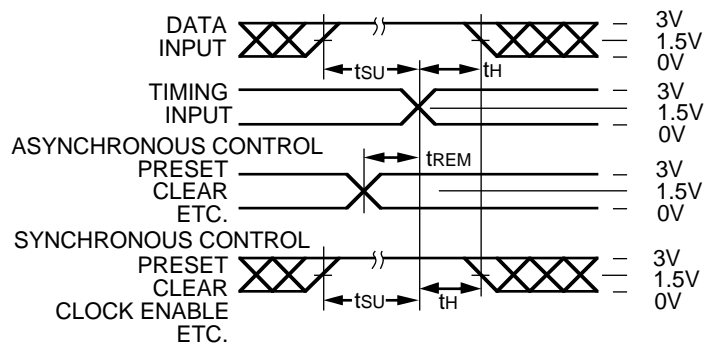
Test	Switch
Open Drain Disable Low Enable Low	6V
Disable High Enable High	GND
All Other tests	Open

#### DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance.  
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

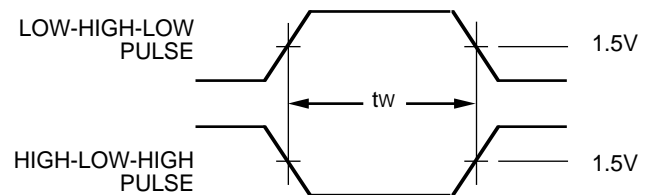
2532 Ink 08

### SET-UP, HOLD AND RELEASE TIMES



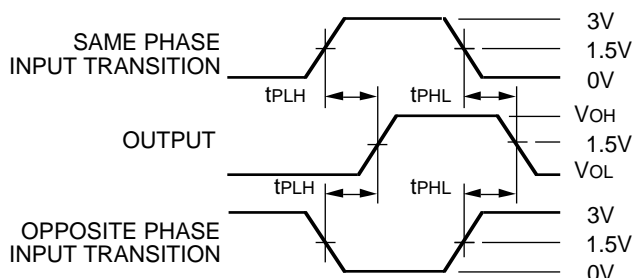
2532 drw 06

### PULSE WIDTH



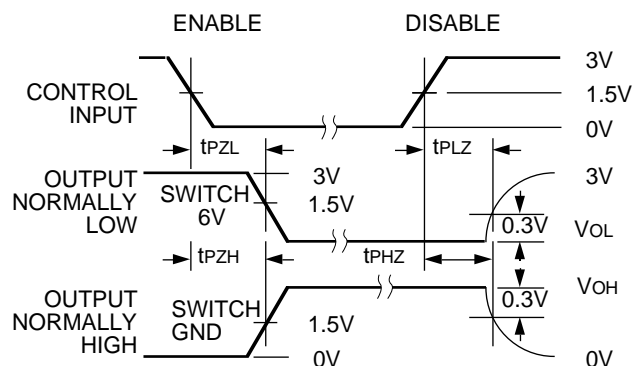
2532 drw 07

### PROPAGATION DELAY



2532 drw 08

### ENABLE AND DISABLE TIMES



2532 drw 09

#### NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate  $\leq 1.0\text{MHz}$ ;  $t_r \leq 2.5\text{ns}$ ;  $t_f \leq 2.5\text{ns}$ .
3. If VCC is below 3V, input voltage swings should be adjusted not to exceed VCC.

## ORDERING INFORMATION

