SN74LV244APW

PCB

SN54LV244A, SN74LV244A
OCTAL BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS

SCLS383B – SEPTEMBER 1997 – REVISED JUNE 1998

- **EPIC™ (Enhanced-Performance Implanted CMOS) Process**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC}, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC}, T_A = 25°C**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Package Options Include Plastic Small-Outline (DW, NS), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages, Ceramic Flat (W) Packages, Chip Carriers (FK), and DIPs (J)**

description

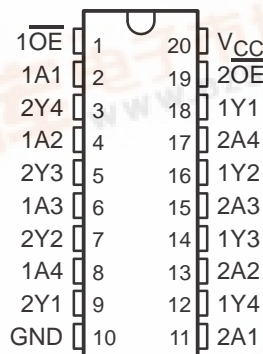These octal buffers/line drivers are designed for 2-V to 5.5-V V_{CC} operation.

The 'LV244A devices are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

These devices are organized as two 4-bit line drivers with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the device passes data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.
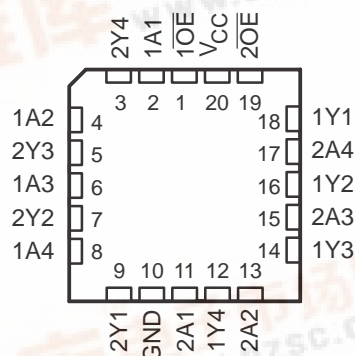
To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54LV244A is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LV244A is characterized for operation from –40°C to 85°C.

SN54LV244A . . . J OR W PACKAGE
SN74LV244A . . . DB, DGV, DW, NS, OR PW PACKAGE
(TOP VIEW)

1$\overline{OE}$	1	20 V_{CC}
1A1	2	19 2$\overline{OE}$
2Y4	3	18 1Y1
1A2	4	17 2A4
2Y3	5	16 1Y2
1A3	6	15 2A3
2Y2	7	14 1Y3
1A4	8	13 2A2
2Y1	9	12 1Y4
GND	10	11 2A1

SN54LV244A . . . FK PACKAGE
(TOP VIEW)

Top pins: 2Y4, 1A1, 1$\overline{OE}$, V_{CC}, 2$\overline{OE}$ (3 2 1 20 19)

1A2	4	18 1Y1
2Y3	5	17 2A4
1A3	6	16 1Y2
2Y2	7	15 2A3
1A4	8	14 1Y3

Bottom pins: 2Y1, GND, 2A1, 1Y4, 2A2 (9 10 11 12 13)

FUNCTION TABLE
(each buffer)

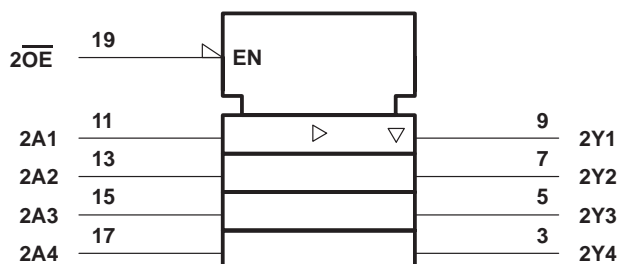| INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

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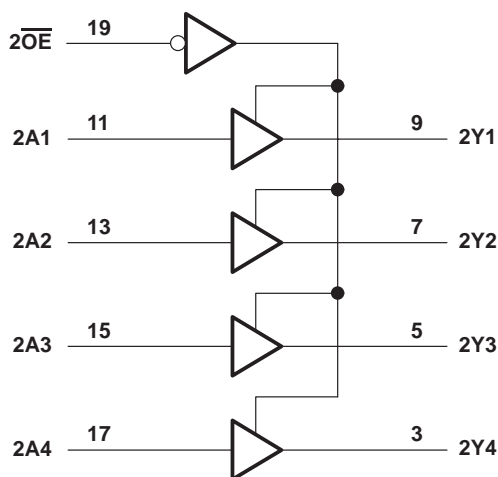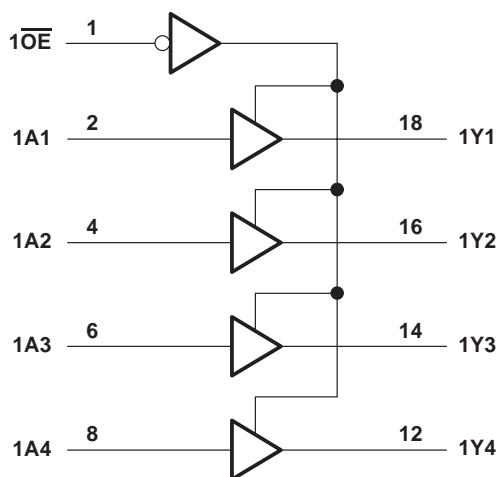EPIC is a trademark of Texas Instruments Incorporated.

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SN54LV244A, SN74LV244A
OCTAL BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS

logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} .... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) .... −0.5 V to 7 V
Output voltage range applied in the high or low state, V_O (see Notes 1 and 2) ...... −0.5 V to V_{CC} + 0.5 V
Output voltage range applied in high-impedance or power-off state, V_O (see Note 1) .... −0.5 V to 7 V
Input clamp current, I_{IK} (V_I < 0) .... −20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) .... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) .... ±35 mA
Continuous current through V_{CC} or GND .... ±70 mA
Package thermal impedance, θ_{JA} (see Note 3): DB package .... 115°C/W
                                           DGV package .... 146°C/W
                                           DW package .... 97°C/W
                                           NS package .... 100°C/W
                                           PW package .... 128°C/W
Storage temperature range, T_{stg} .... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
          2. This value is limited to 7 V maximum.
          3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			SN54LV244A		SN74LV244A		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	5.5	2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		1.5		V
		V_{CC} = 2.3 V to 2.7 V	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		
		V_{CC} = 3 V to 3.6 V	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		
		V_{CC} = 4.5 V to 5.5 V	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5		0.5	V
		V_{CC} = 2.3 V to 2.7 V		$V_{CC} \times 0.3$		$V_{CC} \times 0.3$	
		V_{CC} = 3 V to 3.6 V		$V_{CC} \times 0.3$		$V_{CC} \times 0.3$	
		V_{CC} = 4.5 V to 5.5 V		$V_{CC} \times 0.3$		$V_{CC} \times 0.3$	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage	High or low state	0	V_{CC}	0	V_{CC}	V
		3-state	0	5.5	0	5.5	
I_{OH}	High-level output current	V_{CC} = 2 V		−50		−50	μA
		V_{CC} = 2.3 V to 2.7 V		−2		−2	mA
		V_{CC} = 3 V to 3.6 V		−8		−8	
		V_{CC} = 4.5 V to 5.5 V		−16		−16	
I_{OL}	Low-level output current	V_{CC} = 2 V		50		50	μA
		V_{CC} = 2.3 V to 2.7 V		2		2	mA
		V_{CC} = 3 V to 3.6 V		8		8	
		V_{CC} = 4.5 V to 5.5 V		16		16	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 2.3 V to 2.7 V	0	200	0	200	ns/V
		V_{CC} = 3 V to 3.6 V	0	100	0	100	
		V_{CC} = 4.5 V to 5.5 V	0	20	0	20	
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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WITH 3-STATE OUTPUTS
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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	SN54LV244A MIN	SN54LV244A TYP	SN54LV244A MAX	SN74LV244A MIN	SN74LV244A TYP	SN74LV244A MAX	UNIT
V_{OH}	$I_{OH} = -50\ \mu A$	2 V to 5.5 V	V_{CC}–0.1			V_{CC}–0.1			V
	$I_{OH} = -2$ mA	2.3 V	2			2			
	$I_{OH} = -8$ mA	3 V	2.48			2.48			
	$I_{OH} = -16$ mA	4.5 V	3.8			3.8			
V_{OL}	$I_{OL} = 50\ \mu A$	2 V to 5.5 V			0.1			0.1	V
	$I_{OL} = 2$ mA	2.3 V			0.4			0.4	
	$I_{OL} = 8$ mA	3 V			0.44			0.44	
	$I_{OL} = 16$ mA	4.5 V			0.55			0.55	
I_I	$V_I = V_{CC}$ or GND	5.5 V			±1			±1	μA
I_{OZ}	$V_O = V_{CC}$ or GND	5.5 V			±5			±5	μA
I_{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			20			20	μA
I_{off}	V_I or $V_O = 0$ to 5.5 V	0 V			20			20	μA
C_i	$V_I = V_{CC}$ or GND	3.3 V		2.3			2.3		pF
		5 V		2.3			2.3		

switching characteristics over recommended operating free-air temperature range, V_{CC} = 2.5 V $\pm$ 0.2 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25°C$ MIN	$T_A = 25°C$ TYP	$T_A = 25°C$ MAX	SN54LV244A MIN	SN54LV244A MAX	SN74LV244A MIN	SN74LV244A MAX	UNIT
t_{pd}*	A	Y	C_L = 15 pF		7.5	12.5	1	15	1	15	ns
t_{en}*	$\overline{OE}$	Y			8.9	14.6	1	17	1	17	
t_{dis}*	$\overline{OE}$	Y			9.1	14.1	1	16	1	16	
t_{pd}	A	Y	C_L = 50 pF		9.5	15.3	1	18	1	18	ns
t_{en}	$\overline{OE}$	Y			10.8	17.8	1	21	1	21	
t_{dis}	$\overline{OE}$	Y			13.4	19.2	1	21	1	21	
$t_{sk(o)}$†						2				2	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.
† Skew between any two outputs of the same package switching in the same direction

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V $\pm$ 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25°C$ MIN	$T_A = 25°C$ TYP	$T_A = 25°C$ MAX	SN54LV244A MIN	SN54LV244A MAX	SN74LV244A MIN	SN74LV244A MAX	UNIT
t_{pd}*	A	Y	C_L = 15 pF		5.4	8.4	1	10	1	10	ns
t_{en}*	$\overline{OE}$	Y			6.3	10.6	1	12.5	1	12.5	
t_{dis}*	$\overline{OE}$	Y			7.6	11	1	13	1	13	
t_{pd}	A	Y	C_L = 50 pF		6.8	11.9	1	13.5	1	13.5	ns
t_{en}	$\overline{OE}$	Y			7.8	14.1	1	16	1	16	
t_{dis}	$\overline{OE}$	Y			11	16	1	18	1	18	
$t_{sk(o)}$†						1.5				1.5	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.
† Skew between any two outputs of the same package switching in the same direction

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switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V $\pm$ 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54LV244A		SN74LV244A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}*	A	Y	C_L = 15 pF		3.9	5.5	1	6.5	1	6.5	ns
t_{en}*	$\overline{OE}$	Y			4.5	7.3	1	8.5	1	8.5	
t_{dis}*	$\overline{OE}$	Y			6.5	12.2	1	13.5	1	13.5	
t_{pd}	A	Y	C_L = 50 pF		4.9	7.5	1	8.5	1	8.5	ns
t_{en}	$\overline{OE}$	Y			5.6	9.3	1	10.5	1	10.5	
t_{dis}	$\overline{OE}$	Y			8.8	14.2	1	15.5	1	15.5	
$t_{sk(o)}$†						1				1	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.
† Skew between any two outputs of the same package switching in the same direction

noise characteristics, V_{CC} = 3.3 V, C_L = 50 pF, T_A = 25°C (see Note 5)

PARAMETER		SN74LV244A			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.55		V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.5		V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		2.9		V
$V_{IH(D)}$	High-level dynamic input voltage	2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

NOTE 5: Characteristics are for surface-mount packages only.

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 10 MHz	3.3 V	14	pF
			5 V	16	

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PARAMETER MEASUREMENT INFORMATION

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}

LOAD CIRCUIT FOR TOTEM-POLE OUTPUTS

LOAD CIRCUIT FOR 3-STATE AND OPEN-DRAIN OUTPUTS

VOLTAGE WAVEFORMS PULSE DURATION

VOLTAGE WAVEFORMS SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES INVERTING AND NONINVERTING OUTPUTS

VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
   B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
      Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
   C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
   D. The outputs are measured one at a time with one input transition per measurement.
   E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
   F. t_{PZL} and t_{PZH} are the same as t_{en}.
   G. t_{PHL} and t_{PLH} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

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