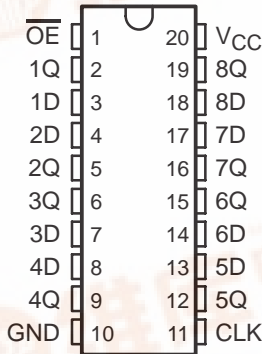# SN54LV374A, SN74LV374A
OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS
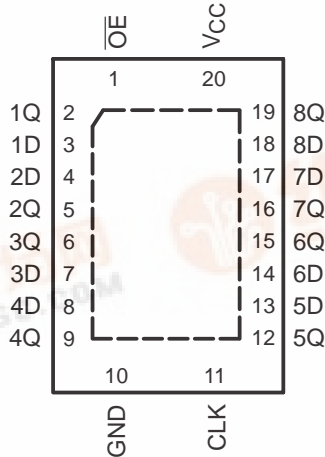## WITH 3-STATE OUTPUTS

SCLS408G – APRIL 1998 – REVISED DECEMBER 2004

- 2-V to 5.5-V V_{CC} Operation
- Max t_{pd} of 9.5 ns at 5 V
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) >2.3 V at V_{CC} = 3.3 V, T_A = 25°C
- Support Mixed-Mode Voltage Operation on All Ports

- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  – 2000-V Human-Body Model (A114-A)
  – 200-V Machine Model (A115-A)
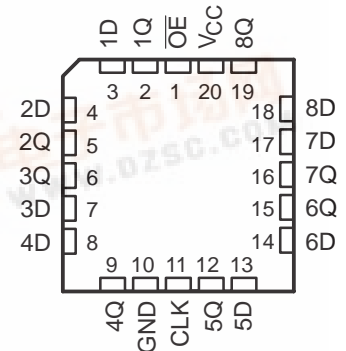 – 1000-V Charged-Device Model (C101)

SN54LV374A . . . J OR W PACKAGE
SN74LV374A . . . DB, DGV, DW, NS, OR PW PACKAGE
(TOP VIEW)

$\overline{OE}$	1	20	V_{CC}
1Q	2	19	8Q
1D	3	18	8D
2D	4	17	7D
2Q	5	16	7Q
3Q	6	15	6Q
3D	7	14	6D
4D	8	13	5D
4Q	9	12	5Q
GND	10	11	CLK

SN74LV374A . . . RGY PACKAGE
(TOP VIEW)

1Q	2	19	8Q
1D	3	18	8D
2D	4	17	7D
2Q	5	16	7Q
3Q	6	15	6Q
3D	7	14	6D
4D	8	13	5D
4Q	9	12	5Q

(1 = $\overline{OE}$, 20 = V_{CC}, 10 = GND, 11 = CLK)

SN54LV374A . . . FK PACKAGE
(TOP VIEW)

Pins: 1D, 1Q, $\overline{OE}$, V_{CC}, 8Q (top: 3 2 1 20 19)

2D	4	18	8D
2Q	5	17	7D
3Q	6	16	7Q
3D	7	15	6Q
4D	8	14	6D

(bottom: 9 10 11 12 13 = 4Q, GND, CLK, 5Q, 5D)

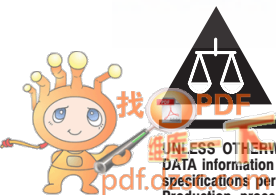## description/ordering information

The 'LV374A devices are octal edge-triggered D-type flip-flops designed for 2-V to 5.5-V V_{CC} operation.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	QFN – RGY	Reel of 1000	SN74LV374ARGYR	LV374A
	SOIC – DW	Tube of 25	SN74LV374ADW	LV374A
		Reel of 2000	SN74LV374ADWR	
	SOP – NS	Reel of 2000	SN74LV374ANSR	74LV374A
	SSOP – DB	Reel of 2000	SN74LV374ADBR	LV374A
	TSSOP – PW	Tube of 70	SN74LV374APW	LV374A
		Reel of 2000	SN74LV374APWR	LV374A
		Reel of 250	SN74LV374APWT	LV374A
	TVSOP – DGV	Reel of 2000	SN74LV374ADGVR	LV374A
	VFBGA – GQN	Reel of 1000	SN74LV374AGQNR	LV374A
−55°C to 125°C	CDIP – J	Tube of 20	SNJ54LV374AJ	SNJ54LV374AJ
	CFP – W	Tube of 85	SNJ54LV374AW	SNJ54LV374AW
	LCCC – FK	Tube of 55	SNJ54LV374AFK	SNJ54LV374AFK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

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TEXAS INSTRUMENTS

description/ordering information (continued)

These devices feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels set up at the data (D) inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

$\overline{OE}$ does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

These devices are fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

GQN PACKAGE
(TOP VIEW)
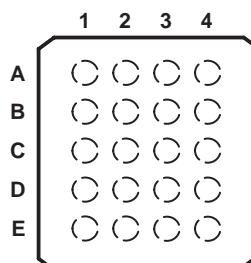
terminal assignments

	1	2	3	4
A	1Q	$\overline{OE}$	V_{CC}	8Q
B	2D	7D	1D	8D
C	3Q	2Q	6Q	7Q
D	4D	5D	3D	6D
E	GND	4Q	CLK	5Q

FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

logic diagram (positive logic)
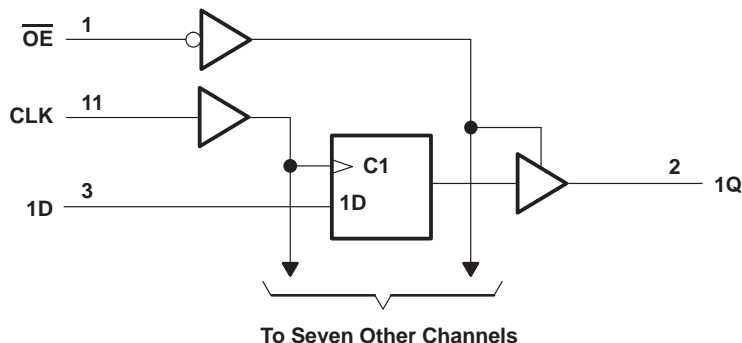
Pin numbers shown are for the DB, DGV, DW, FK, J, NS, PW, RGY, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) .... −0.5 V to 7 V
Voltage range applied to any output in the high-impedance or
  power-off state, V_O (see Note 1) .... −0.5 V to 7 V
Output voltage range, V_O (see Notes 1 and 2) .... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) .... −20 mA
Output clamp current, I_{OK} ($V_O < 0$) .... −50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) .... ±35 mA
Continuous current through V_{CC} or GND .... ±70 mA
Package thermal impedance, θ_{JA} (see Note 3): DB package .... 70°C/W
                            (see Note 3): DGV package .... 92°C/W
                            (see Note 3): DW package .... 58°C/W
                            (see Note 3): GQN package .... 78°C/W
                            (see Note 3): NS package .... 60°C/W
                            (see Note 3): PW package .... 83°C/W
                            (see Note 4): RGY package .... 37°C/W
Storage temperature range, T_{stg} .... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
       2. This value is limited to 5.5 V maximum.
       3. The package thermal impedance is calculated in accordance with JESD 51-7.
       4. The package thermal impedance is calculated in accordance with JESD 51-5.

recommended operating conditions (see Note 5)

			SN54LV374A		SN74LV374A		UNIT
			MIN	**MAX**	**MIN**	**MAX**	
V_{CC}	Supply voltage		2	5.5	2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		1.5		V
		V_{CC} = 2.3 V to 2.7 V	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		
		V_{CC} = 3 V to 3.6 V	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		
		V_{CC} = 4.5 V to 5.5 V	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5		0.5	V
		V_{CC} = 2.3 V to 2.7 V		$V_{CC} \times 0.3$		$V_{CC} \times 0.3$	
		V_{CC} = 3 V to 3.6 V		$V_{CC} \times 0.3$		$V_{CC} \times 0.3$	
		V_{CC} = 4.5 V to 5.5 V		$V_{CC} \times 0.3$		$V_{CC} \times 0.3$	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage	High or low state	0	V_{CC}	0	V_{CC}	V
		3-state	0	5.5	0	5.5	
I_{OH}	High-level output current	V_{CC} = 2 V		−50		−50	μA
		V_{CC} = 2.3 V to 2.7 V		−2		−2	mA
		V_{CC} = 3 V to 3.6 V		−8		−8	
		V_{CC} = 4.5 V to 5.5 V		−16		−16	
I_{OL}	Low-level output current	V_{CC} = 2 V		50		50	μA
		V_{CC} = 2.3 V to 2.7 V		2		2	mA
		V_{CC} = 3 V to 3.6 V		8		8	
		V_{CC} = 4.5 V to 5.5 V		16		16	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 2.3 V to 2.7 V		200		200	ns/V
		V_{CC} = 3 V to 3.6 V		100		100	
		V_{CC} = 4.5 V to 5.5 V		20		20	
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 5: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	SN54LV374A			SN74LV374A			UNIT
			MIN	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	
V_{OH}	I_{OH} = −50 μA	2 V to 5.5 V	V_{CC}−0.1			V_{CC}−0.1			V
	I_{OH} = −2 mA	2.3 V	2			2			
	I_{OH} = −8 mA	3 V	2.48			2.48			
	I_{OH} = −16 mA	4.5 V	3.8			3.8			
V_{OL}	I_{OL} = 50 μA	2 V to 5.5 V			0.1			0.1	V
	I_{OL} = 2 mA	2.3 V			0.4			0.4	
	I_{OL} = 8 mA	3 V			0.44			0.44	
	I_{OL} = 16 mA	4.5 V			0.55			0.55	
I_I	V_I = 5.5 V or GND	0 to 5.5 V			±1			±1	μA
I_{OZ}	V_O = V_{CC} or GND	5.5 V			±5			±5	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			20			20	μA
I_{off}	V_I or V_O = 0 to 5.5 V	0			5			5	μA
C_i	V_I = V_{CC} or GND	3.3 V		2.9			2.9		pF

TEXAS INSTRUMENTS

timing requirements over recommended operating free-air temperature range, V$_{CC}$ = 2.5 V $\pm$ 0.2 V (unless otherwise noted) (see Figure 1)

		T$_A$ = 25°C		SN54LV374A		SN74LV374A		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t$_w$	Pulse duration, CLK high or low	6		7		7		ns
t$_{su}$	Setup time, data before CLK↑	5		5.5		5.5		ns
t$_h$	Hold time, data after CLK↑	2.5		2.5		2.5		ns

timing requirements over recommended operating free-air temperature range, V$_{CC}$ = 3.3 V $\pm$ 0.3 V (unless otherwise noted) (see Figure 1)

		T$_A$ = 25°C		SN54LV374A		SN74LV374A		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t$_w$	Pulse duration, CLK high or low	5		5.5		5.5		ns
t$_{su}$	Setup time, data before CLK↑	4.5		4.5		4.5		ns
t$_h$	Hold time, data after CLK↑	2		2		2		ns

timing requirements over recommended operating free-air temperature range, V$_{CC}$ = 5 V $\pm$ 0.5 V (unless otherwise noted) (see Figure 1)

		T$_A$ = 25°C		SN54LV374A		SN74LV374A		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t$_w$	Pulse duration, CLK high or low	5		5		5		ns
t$_{su}$	Setup time, data before CLK↑	3		3		3		ns
t$_h$	Hold time, data after CLK↑	2		2		2		ns

switching characteristics over recommended operating free-air temperature range, V$_{CC}$ = 2.5 V $\pm$ 0.2 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T$_A$ = 25°C			SN54LV374A		SN74LV374A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f$_{max}$			C$_L$ = 15 pF	60*	105*		50*		50		MHz
			C$_L$ = 50 pF	50	85		40		40		
t$_{pd}$	CLK	Q	C$_L$ = 15 pF		9.7*	16.3*	1*	19*	1	19	ns
t$_{en}$	$\overline{OE}$	Q			8.9*	15.9*	1*	19*	1	19	
t$_{dis}$	$\overline{OE}$	Q			6.3*	12.6*	1*	15*	1	15	
t$_{pd}$	CLK	Q	C$_L$ = 50 pF		11.8	19.3	1	23	1	23	ns
t$_{en}$	$\overline{OE}$	Q			10.9	18.8	1	22	1	22	
t$_{dis}$	$\overline{OE}$	Q			8.2	17.3	1	19	1	19	
t$_{sk(o)}$						2				2	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

TEXAS
INSTRUMENTS

SN54LV374A, SN74LV374A
OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS
WITH 3-STATE OUTPUTS

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54LV374A		SN74LV374A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			C_L = 15 pF	80*	150*		70*		70		MHz
			C_L = 50 pF	55	110		50		50		
t_{pd}	CLK	Q	C_L = 15 pF		6.8*	12.7*	1*	15*	1	15	ns
t_{en}	$\overline{OE}$	Q			6.3*	11*	1*	13*	1	13	
t_{dis}	$\overline{OE}$	Q			4.7*	10.5*	1*	12.5*	1	12.5	
t_{pd}	CLK	Q	C_L = 50 pF		8.3	16.2	1	18.5	1	18.5	ns
t_{en}	$\overline{OE}$	Q			7.7	14.5	1	16.5	1	16.5	
t_{dis}	$\overline{OE}$	Q			5.9	14	1	16	1	16	
$t_{sk(o)}$						1.5				1.5	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54LV374A		SN74LV374A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			C_L = 15 pF	130*	205*		110*		110		MHz
			C_L = 50 pF	85	170		75		75		
t_{pd}	CLK	Q	C_L = 15 pF		4.9*	8.1*	1*	9.5*	1	9.5	ns
t_{en}	$\overline{OE}$	Q			4.6*	7.6*	1*	9*	1	9	
t_{dis}	$\overline{OE}$	Q			3.4*	6.8*	1*	8*	1	8	
t_{pd}	CLK	Q	C_L = 50 pF		5.9	10.1	1	11.5	1	11.5	ns
t_{en}	$\overline{OE}$	Q			5.5	9.6	1	11	1	11	
t_{dis}	$\overline{OE}$	Q			4	8.8	1	10	1	10	
$t_{sk(o)}$						1				1	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

noise characteristics, V_{CC} = 3.3 V, C_L = 50 pF, T_A = 25°C (see Note 6)

PARAMETER		SN74LV374A			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.6	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		−0.5	−0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		2.9		V
$V_{IH(D)}$	High-level dynamic input voltage	2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

NOTE 6:   Characteristics are for surface-mount packages only.

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS		V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	Outputs enabled	C_L = 50 pF, f = 10 MHz	3.3 V	21.1	pF
				5 V	22.8	

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INSTRUMENTS

PARAMETER MEASUREMENT INFORMATION

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}

LOAD CIRCUIT FOR TOTEM-POLE OUTPUTS

LOAD CIRCUIT FOR 3-STATE AND OPEN-DRAIN OUTPUTS

VOLTAGE WAVEFORMS PULSE DURATION

VOLTAGE WAVEFORMS SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES INVERTING AND NONINVERTING OUTPUTS

VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
   B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
       Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
   C. All input pulses are supplied by generators having the following characteristics: PRR $\leq$ 1 MHz, Z_O = 50 Ω, $t_r \leq$ 3 ns, $t_f \leq$ 3 ns.
   D. The outputs are measured one at a time, with one input transition per measurement.
   E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
   F. t_{PZL} and t_{PZH} are the same as t_{en}.
   G. t_{PHL} and t_{PLH} are the same as t_{pd}.
   H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

TEXAS
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PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
SN74LV374ADBR	ACTIVE	SSOP	DB	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/Level-1-235C-UNLIM
SN74LV374ADGVR	ACTIVE	TVSOP	DGV	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
SN74LV374ADW	ACTIVE	SOIC	DW	20	25	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/Level-1-235C-UNLIM
SN74LV374ADWR	ACTIVE	SOIC	DW	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/Level-1-235C-UNLIM
SN74LV374AGQNR	ACTIVE	VFBGA	GQN	20	1000	None	SNPB	Level-1-240C-UNLIM
SN74LV374ANSR	ACTIVE	SO	NS	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/Level-1-235C-UNLIM
SN74LV374APW	ACTIVE	TSSOP	PW	20	70	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
SN74LV374APWR	ACTIVE	TSSOP	PW	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
SN74LV374APWT	ACTIVE	TSSOP	PW	20	250	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
SN74LV374ARGYR	ACTIVE	QFN	RGY	20	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
SN74LV374AZQNR	ACTIVE	VFBGA	ZQN	20	1000	Pb-Free (RoHS)	SNAGCU	Level-1-260C-UNLIM

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - May not be currently available - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
None: Not yet available Lead (Pb-Free).
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDECindustry standard classifications, and peak solder temperature.
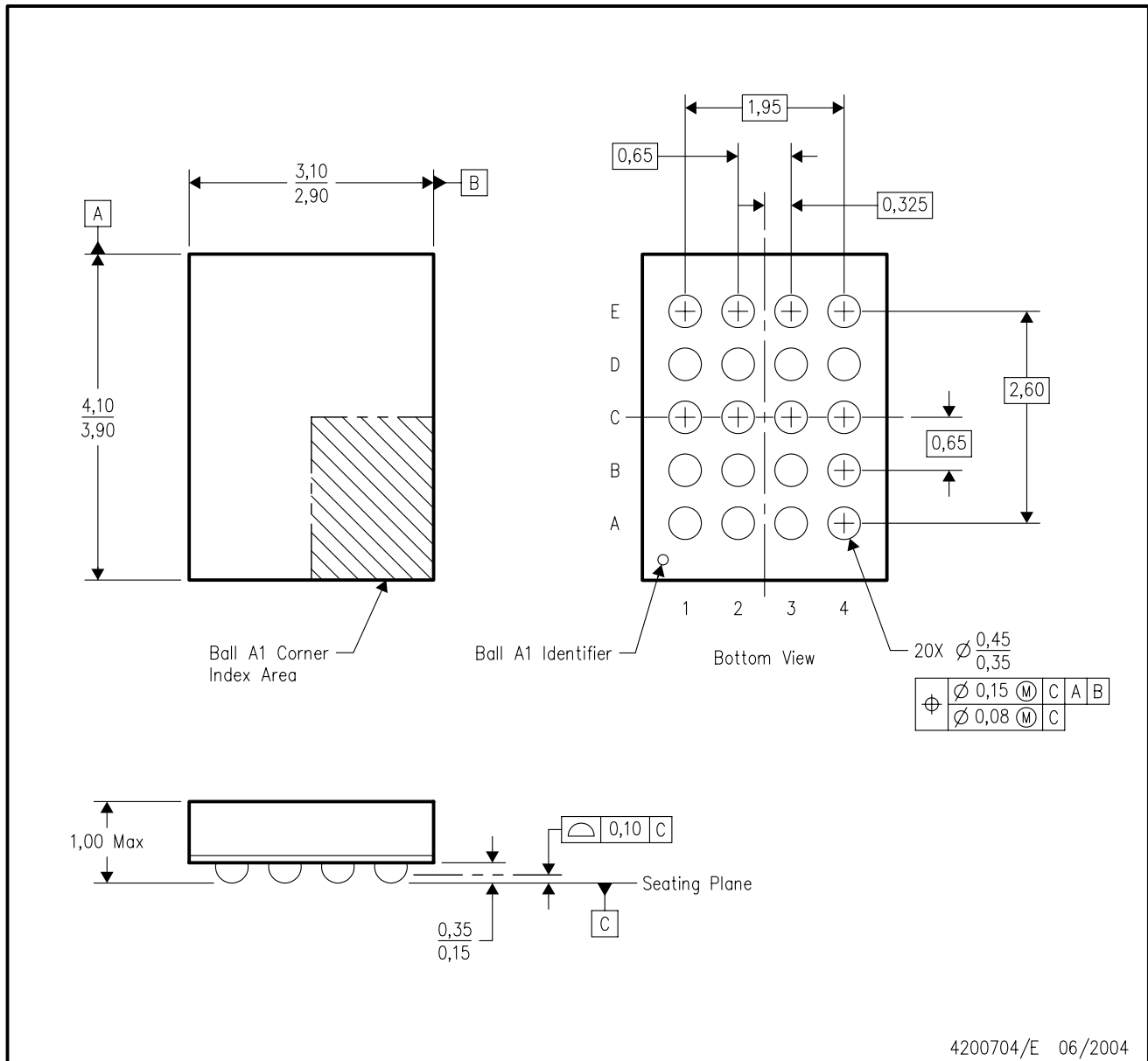
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GQN (R–PBGA–N20) PLASTIC BALL GRID ARRAY

3,10 / 2,90

4,10 / 3,90

Ball A1 Corner Index Area

Ball A1 Identifier

Bottom View

1,95

0,65

0,325

2,60

0,65

20X ∅ 0,45 / 0,35

∅ 0,15 Ⓜ C A B
∅ 0,08 Ⓜ C

1,00 Max

0,10 C

Seating Plane

0,35 / 0,15

C

4200704/E 06/2004

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO–225 variation BC.
D. This package is tin–lead (SnPb). Refer to the 20 ZQN package (drawing 4204492) for lead–free.

ZQN (R–PBGA–N20)   PLASTIC BALL GRID ARRAY

3,10
2,90

4,10
3,90

1,95

0,65

0,325

2,60

0,65

Ball A1 Corner
Index Area

Ball A1 Identifier

Bottom View

E
D
C
B
A

1 2 3 4

20X Ø 0,45
0,35

⌀	Ø 0,15 Ⓜ	C	A	B
	Ø 0,08 Ⓜ	C		

1,00 Max

0,10 C

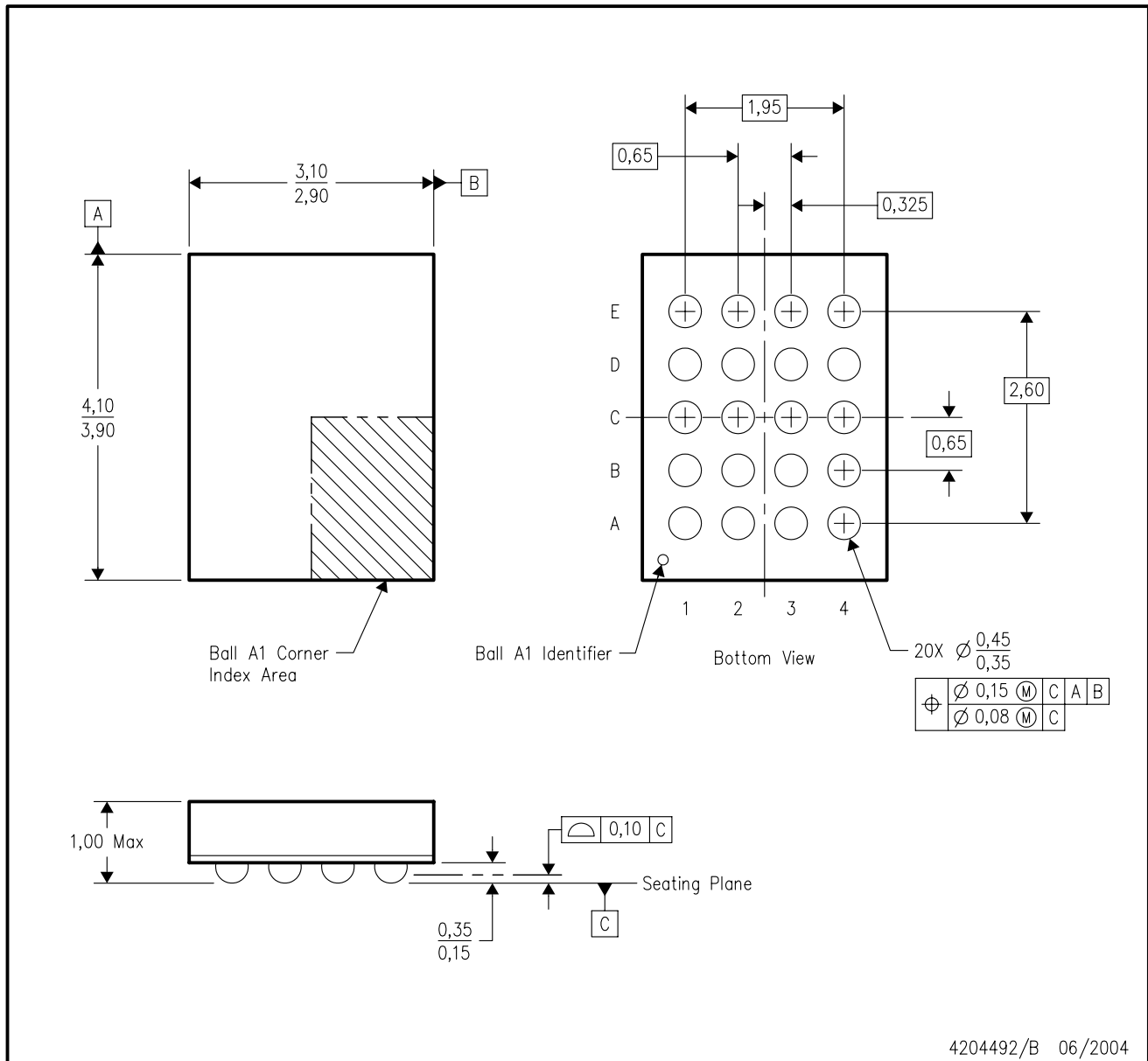Seating Plane

0,35
0,15

C

4204492/B 06/2004

NOTES: A. All linear dimensions are in millimeters.
         B. This drawing is subject to change without notice.
         C. Falls within JEDEC MO–225 variation BC.
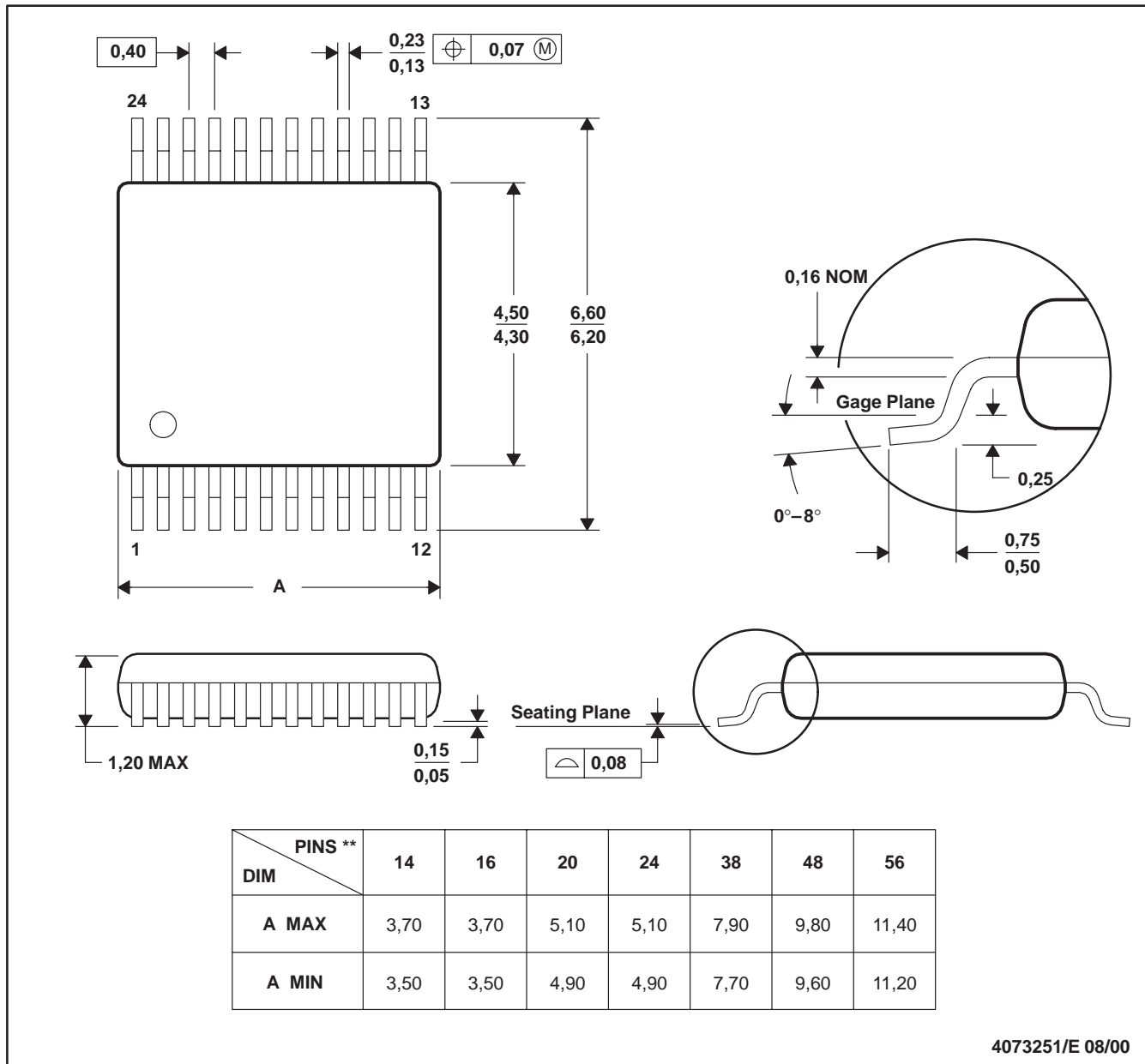   D. This package is lead–free. Refer to the 20 GQN package (drawing 4200704) for tin–lead (SnPb).

DGV (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN

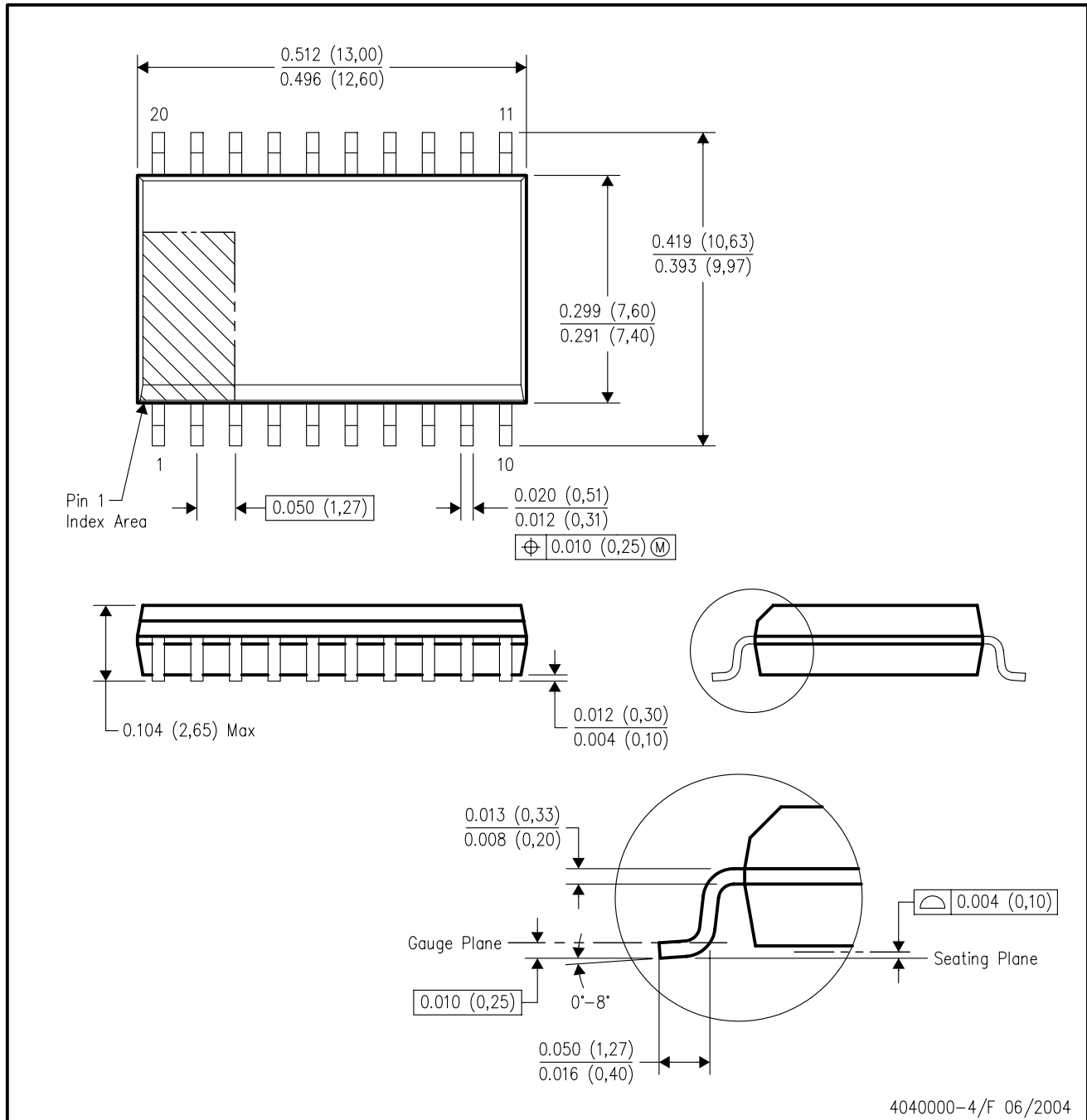| PINS ** DIM	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
       B. This drawing is subject to change without notice.
       C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
       D. Falls within JEDEC: 24/48 Pins – MO-153
                               14/16/20/56 Pins – MO-194

DW (R−PDSO−G20)   PLASTIC SMALL−OUTLINE PACKAGE

0.512 (13,00)
0.496 (12,60)

20   11

0.419 (10,63)
0.393 (9,97)

0.299 (7,60)
0.291 (7,40)

1   10

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ | 0.010 (0,25) Ⓜ

0.104 (2,65) Max

0.012 (0,30)
0.004 (0,10)

0.013 (0,33)
0.008 (0,20)

⌒ | 0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)   0°−8°

0.050 (1,27)
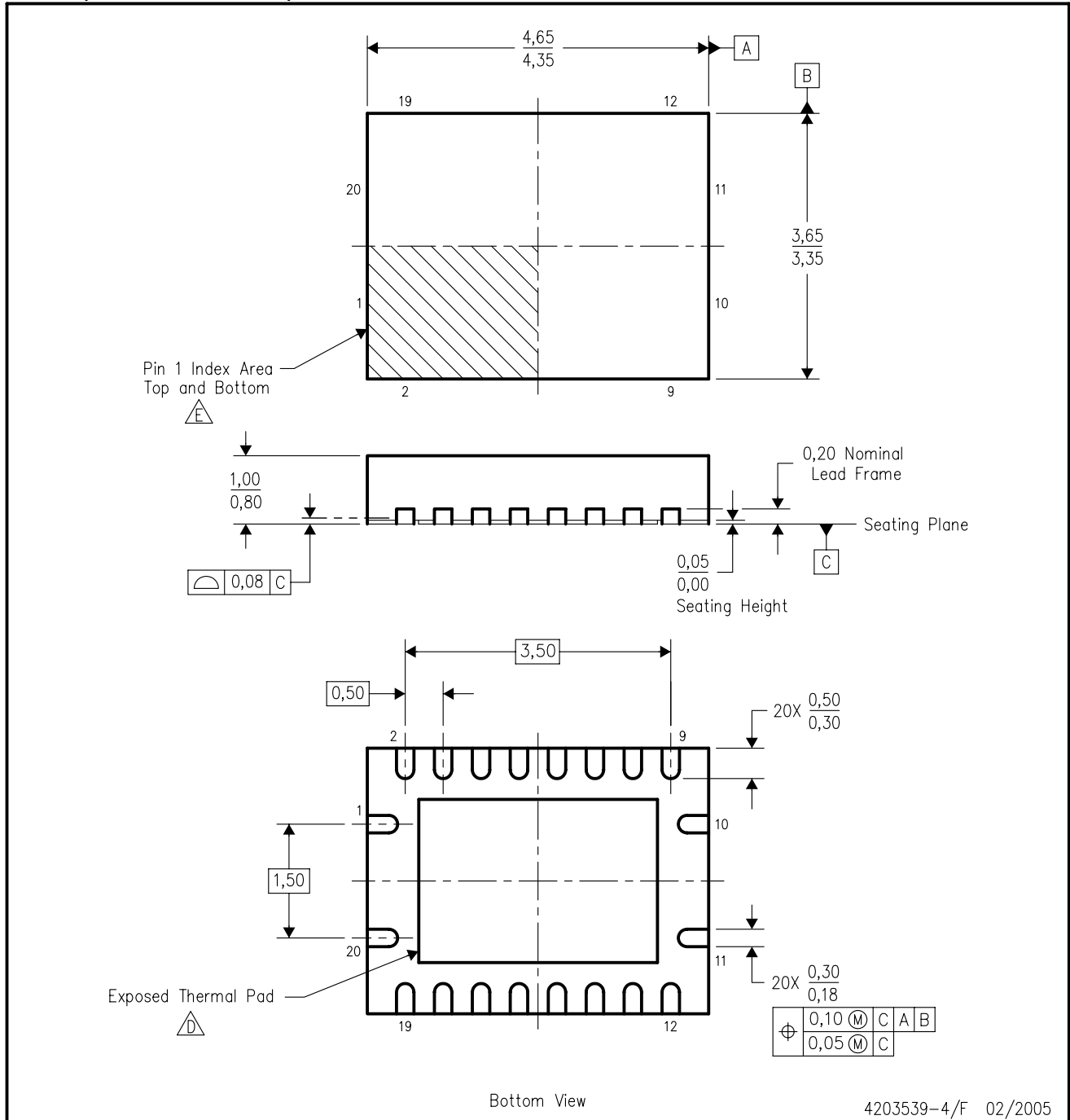0.016 (0,40)

4040000−4/F 06/2004

NOTES: A. All linear dimensions are in inches (millimeters).
          B. This drawing is subject to change without notice.
          C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
          D. Falls within JEDEC MS−013 variation AC.

RGY (R−PQFP−N20)   PLASTIC QUAD FLATPACK

4,65 / 4,35   A

B

19   12

20   11

3,65 / 3,35

1   10

2   9

Pin 1 Index Area
Top and Bottom
E

1,00 / 0,80

0,20 Nominal
Lead Frame

Seating Plane

0,08 C

0,05 / 0,00
Seating Height

3,50

0,50

20X 0,50 / 0,30

2   9

1   10

1,50

20   11

20X 0,30 / 0,18

Exposed Thermal Pad
D

19   12

0,10 M C A B
0,05 M C

Bottom View   4203539−4/F 02/2005
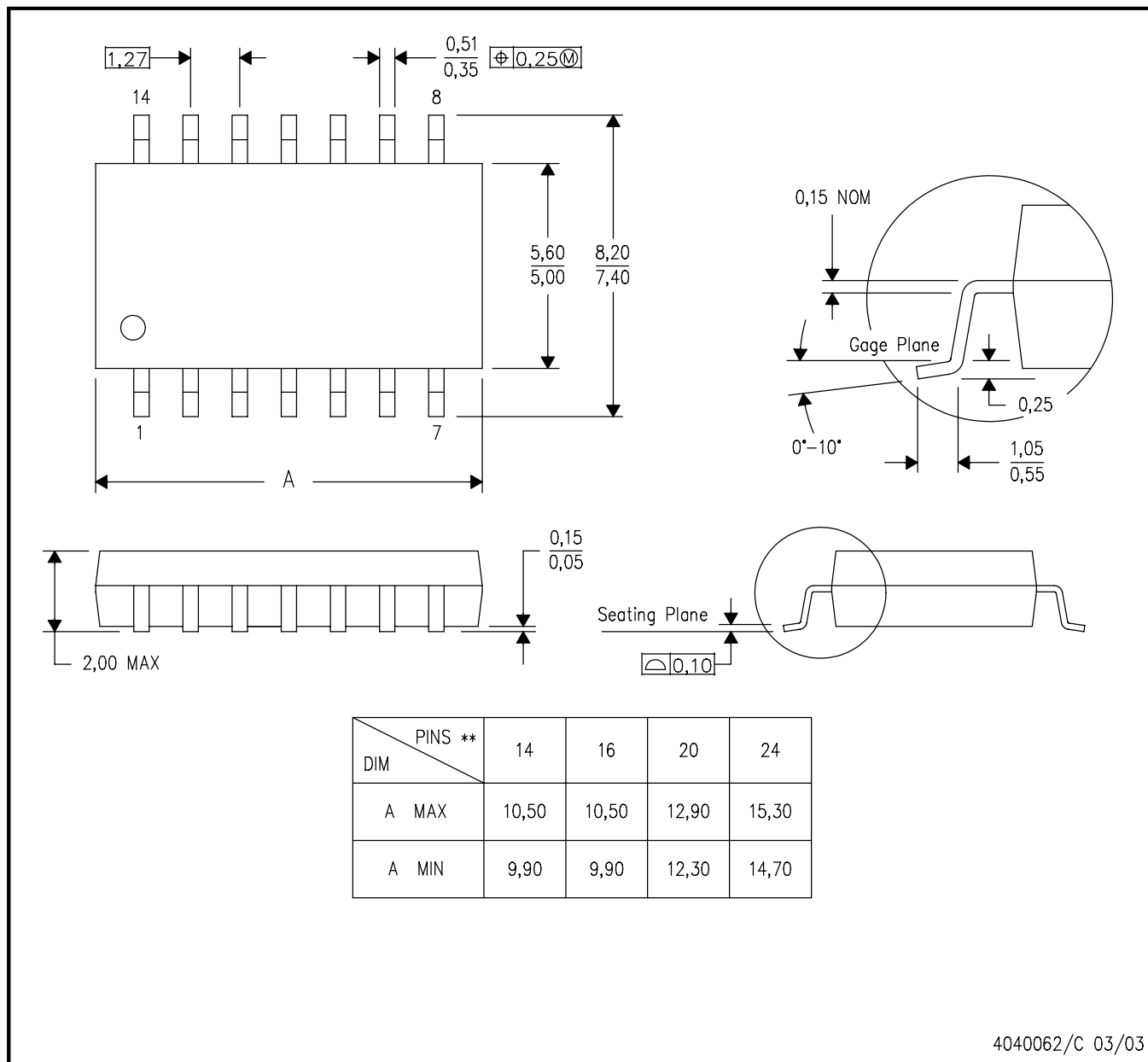
NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
        B. This drawing is subject to change without notice.
        C. QFN (Quad Flatpack No−Lead) package configuration.
        D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
            See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
        E. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated.
            The Pin 1 identifiers are either a molded, marked, or metal feature.
        F. Package complies to JEDEC MO−241 variation BC.

TEXAS INSTRUMENTS
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MECHANICAL DATA

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

DIM / PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES: A.   All linear dimensions are in millimeters.
          B.   This drawing is subject to change without notice.
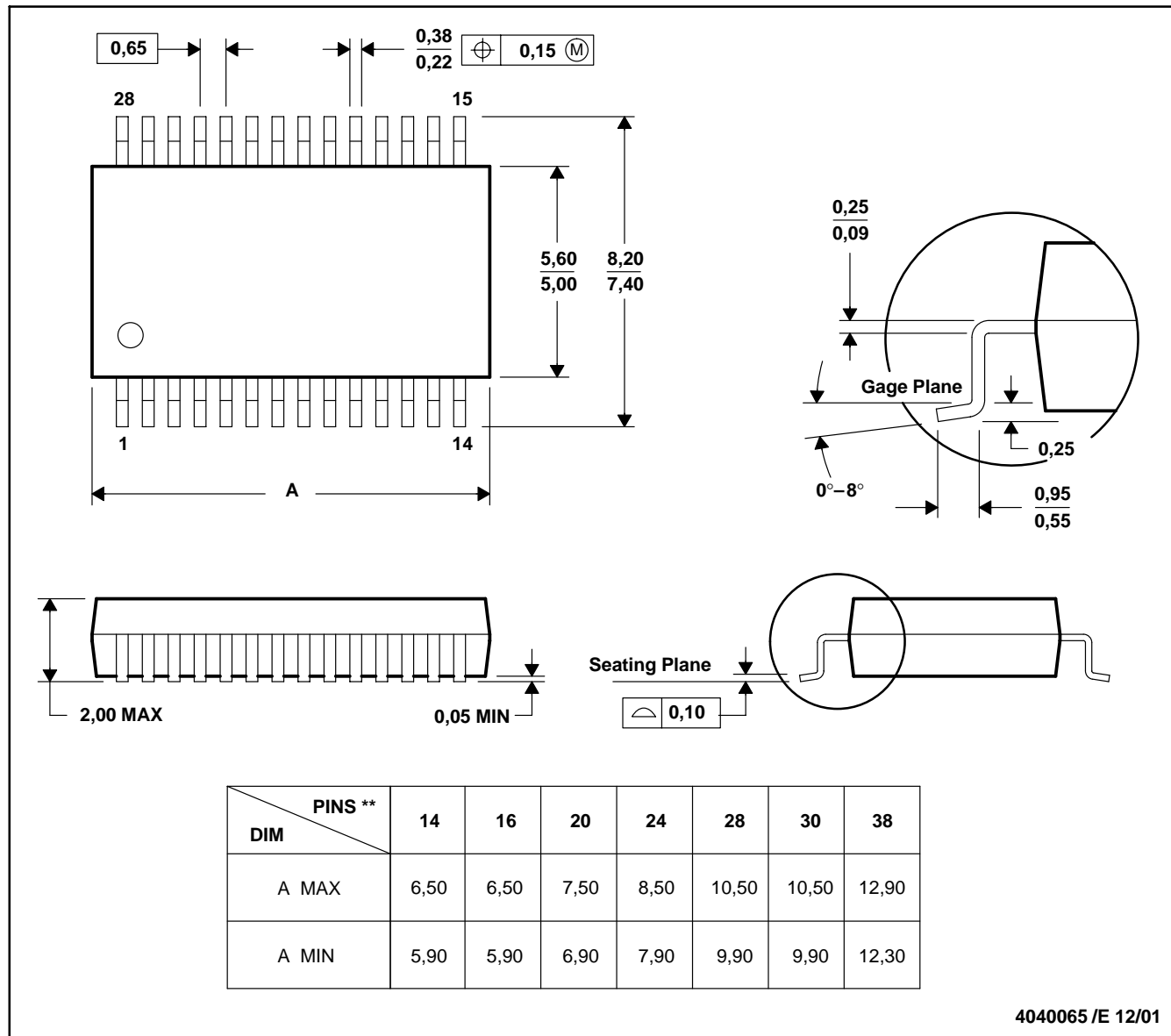   C.   Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

TEXAS
INSTRUMENTS

DB (R-PDSO-G**)　　　　　　　　　　　　　　　　　　**PLASTIC SMALL-OUTLINE**

28 PINS SHOWN

0,65

0,38
0,22

⊕ 0,15 Ⓜ

28　　　15

5,60
5,00

8,20
7,40

0,25
0,09

Gage Plane

0°−8°

0,25

0,95
0,55

1　　　14

A

2,00 MAX

0,05 MIN

Seating Plane

◁ 0,10

4040065 /E 12/01

DIM　PINS **	14	16	20	24	28	30	38
A　MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A　MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
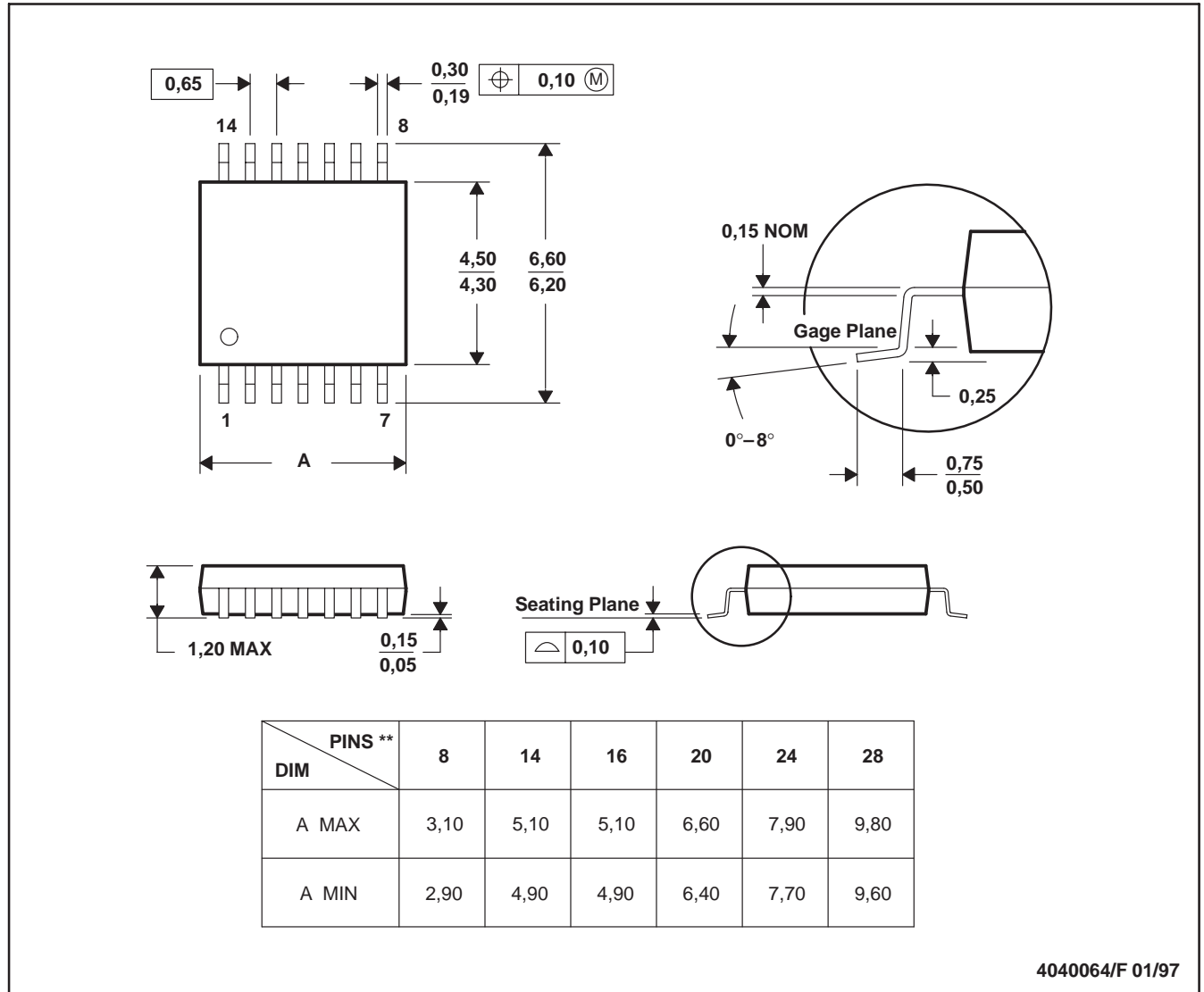D. Falls within JEDEC MO-150

MECHANICAL DATA

PW (R-PDSO-G)**   **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN

DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
   B. This drawing is subject to change without notice.
   C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
   D. Falls within JEDEC MO-153

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