MOTOROLA

Quad EIA-485 Line Drivers with Three-State Outputs

MC75172B
MC75174B

The Motorola MC75172B/174B Quad Line drivers are differential high speed drivers designed to comply with the EIA–485 Standard. Features include three–state outputs, thermal shutdown, and output current limiting in both directions. These devices also comply with EIA–422–A, and CCITT Recommendations V.11 and X.27.

The MC75172B/174B are optimized for balanced multipoint bus transmission at rates in excess of 10 MBPS. The outputs feature wide common mode voltage range, making them suitable for party line applications in noisy environments. The current limit and thermal shutdown features protect the devices from line fault conditions. These devices offer optimum performance when used with the MC75173 and MC75175 line receivers.

Both devices are available in 16–pin plastic DIP and 20–pin wide body surface mount packages.

- Meets EIA–485 Standard for Party Line Operation
- Meets EIA–422–A and CCITT Recommendations V.11 and X.27
- Operating Ambient Temperature: –40°C to +85°C
- High Impedance Outputs
- Common Mode Output Voltage Range: –7 to 12 V
- Positive and Negative Current Limiting
- Transmission Rates in Excess of 10 MBPS
- Thermal Shutdown at 150°C Junction Temperature, ($\pm$20°C)
- Single 5.0 V Supply
- Pin Compatible with TI SN75172/4 and NS μA96172/4
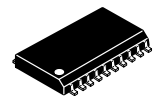- Interchangeable with MC3487 and AM26LS31 for EIA–422–A Applications

QUAD EIA–485 LINE DRIVERS

SEMICONDUCTOR TECHNICAL DATA
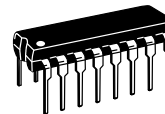
P SUFFIX
PLASTIC PACKAGE
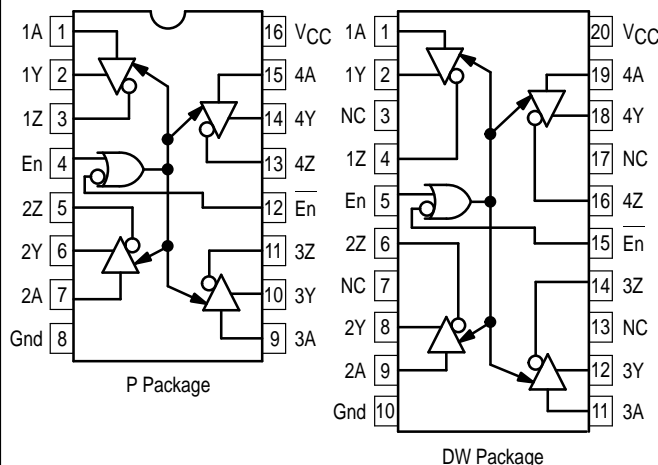CASE 648

DW SUFFIX
PLASTIC PACKAGE
CASE 751D
(SO–20L)

ORDERING INFORMATION
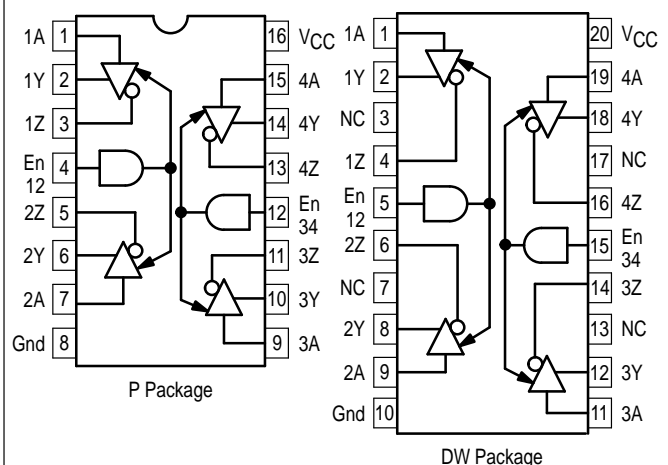
Device	Operating Temperature Range	Package
MC75172BDW		SO–20L
MC75174BDW	$T_A = -40°$ to $+85°C$	SO–20L
MC75174BP		Plastic DIP

PIN CONNECTIONS

MC75172B

P Package

DW Package

MC75174B

P Package

DW Package

Rev 1

MC75172B MC75174B

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	–0.5, +7.0	Vdc
Input Voltage (Data, Enable)	V_{in}	+7.0	Vdc
Input Current (Data, Enable)	I_{in}	–24	mA
Applied Output Voltage, when in 3–State Condition (V_{CC} = 5.0 V)	V_{za}	–10, +14	Vdc
Applied Output Voltage, when V_{CC} = 0 V	V_{zb}	±14	
Output Current	I_O	Self–Limiting	–
Storage Temperature	T_{stg}	–65, +150	°C

Devices should not be operated at these limits. The "Recommended Operating Conditions" table provides for actual device operation.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	V_{CC}	+4.75	+5.0	+5.25	Vdc
Input Voltage (All Inputs)	V_{in}	0	–	V_{CC}	Vdc
Output Voltage in 3–State Condition, or when V_{CC} = 0 V	V_{cm}	–7.0	–	+12	Vdc
Output Current (Normal data transmission)	I_O	–65	–	+65	mA
Operating Ambient Temperature (see text) EIA–485 EIA–422	T_A	–40 0	– –	+85 +85	°C

All limits are not necessarily functional concurrently.

ELECTRICAL CHARACTERISTICS ($-40°C \leq T_A \leq 85°C$, 4.75 V $\leq V_{CC} \leq$ 5.25 V, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage Single–Ended Voltage I_O = 0 High @ I_O = –33 mA Low @ I_O = +33 mA Differential Voltage Open Circuit (I_O = 0) R_L = 54 Ω (Figure 1)	V_O V_{OH} V_{OL} $|V_{OD1}|$ $|V_{OD2}|$	0 – – 1.5 1.5	– 4.0 1.6 3.4 2.3	6.0 – – 6.0 5.0	Vdc
Change in Differential*, R_L = 54 Ω (Figure 1)	$|\Delta V_{OD2}|$	–	5.0	200	mVdc
Differential Voltage, R_L = 100 Ω (Figure 1)	$|V_{OD2A}|$	–	2.2	–	Vdc
Change in Differential*, R_L = 100 Ω (Figure 1)	$|\Delta V_{OD2A}|$	–	5.0	200	mVdc
Differential Voltage, –7.0 V $\leq V_{cm} \leq$ 12 V (Figure 2)	$|V_{OD3}|$	1.5	–	5.0	Vdc
Change in Differential*, –7.0 V $\leq V_{cm} \leq$ 12 V (Figure 2)	$|\Delta V_{OD3}|$	–	5.0	200	mVdc
Offset Voltage, R_L = 54 Ω (Figure 1)	V_{OS}	–	2.9	–	Vdc
Change in Offset*, R_L = 54 Ω (Figure 1)	$|\Delta V_{OS}|$	–	5.0	200	mVdc
Output Current (Each Output) Power Off Leakage, V_{CC} = 0, –7.0 V $\leq V_O \leq$ 12 V Leakage in 3–State Mode, –7.0 V $\leq V_O \leq$ 12 V	$I_{O(off)}$ I_{OZ}	–50 –50	0 0	+50 +50	µA
Short Circuit Current to Ground Short Circuit Current, –7.0 V $\leq V_O \leq$ 12 V	I_{OSR} I_{OS}	–150 –250	– –	+150 +250	mA

*V_{in} switched from 0.8 to 2.0 V.
Typical values determined at 25°C ambient and 5.0 V supply.

MC75172B MC75174B

ELECTRICAL CHARACTERISTICS ($-40°C \leq T_A \leq 85°C$, 4.75 V $\leq V_{CC} \leq$ 5.25 V, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit

Inputs
  Low Level Voltage (Pins 4 & 12, MC75174B only)
  Low Level Voltage (All Other Pins)
  High Level Voltage (All Inputs)
	$V_{IL(A)}$
	$V_{IL(B)}$
	V_{IH}
		0
		0
		2.0
			–
			–
			–
				0.7
				0.8
				V_{CC}
					Vdc

Current @ V_{in} = 2.7 V (All Inputs) Current @ V_{in} = 0.5 V (All Inputs)	I_{IH} I_{IL}	– –100	0.2 –15	20 –	µA
Clamp Voltage (All Inputs, I_{in} = –18 mA)	V_{IK}	–1.5	–	–	Vdc
Thermal Shutdown Junction Temperature	T_{jts}	–	+150	–	°C

Power Supply Current (Outputs Open, V_{CC} = 5.25 V)
  Outputs Enable
  Outputs Disabled
	I_{CC}	
		–
		–
			
			60
			30
				
				70
				40
					mA

TIMING CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V)

| Characteristics	Symbol	Min	Typ	Max	Unit

Propagation Delay – Input to Single–ended Output (Figure 3)
  Output Low–to–High
  Output High–to–Low
	
	t_{PLH}
	t_{PHL}
		
		–
		–
			
			23
			18
				
				30
				30
					ns

Propagation Delay – Input to Differential Output (Figure 4)
  Input Low–to–High
  Input High–to–Low
	
	$t_{PLH(D)}$
	$t_{PHL(D)}$
		
		–
		–
			
			15
			17
				
				25
				25
					ns

Differential Output Transition Time (Figure 4)	t_{dr}, t_{df}	–	19	25	ns

Skew Timing
  $\lvert t_{PLHD} - t_{PHLD} \rvert$ for Each Driver
  Max – Min t_{PLHD} Within a Package
  Max – Min t_{PHLD} Within a Package
	
	t_{SK1}
	t_{SK2}
	t_{SK3}
		
		–
		–
		–
			
			0.2
			1.5
			1.5
				
				–
				–
				–
					ns

Enable Timing
  Single–ended Outputs (Figure 5)
    Enable to Active High Output
    Enable to Active Low Output
    Active High to Disable (using Enable)
    <u>Active</u> Low to Disable (using Enable)
    <u>Enable</u> to Active High Output (MC75172B only)
    Enable to Active Low Output (<u>MC751</u>72B only)
    Active High to Disable (using <u>Enable</u>, MC75172B only)
    Active Low to Disable (using Enable, MC75172B only)
	
	$t_{PZH(E)}$
	$t_{PZL(E)}$
	$t_{PHZ(E)}$
	$t_{PLZ(E)}$
	$t_{PZH(E)}$
	$t_{PZL(E)}$
	$t_{PHZ(E)}$
	$t_{PLZ(E)}$
		
		–
		–
		–
		–
		–
		–
		–
		–
			
			48
			20
			35
			30
			58
			28
			38
			36
				
				60
				30
				45
				50
				70
				35
				50
				50
					ns

Differential Outputs (Figure 6)
  <u>Enable</u> to Active Output
  Enable to Active Output (MC75172B only)
  <u>Enable</u> to 3–State Output
  Enable to 3–State Output (MC75172B only)
	
	$t_{PZD(E)}$
	$t_{PZD(E)}$
	$t_{PDZ(E)}$
	$t_{PDZ(E)}$
		
		–
		–
		–
		–
			
			47
			56
			32
			40
				
				–
				–
				–
				–
					ns

MC75172B MC75174B
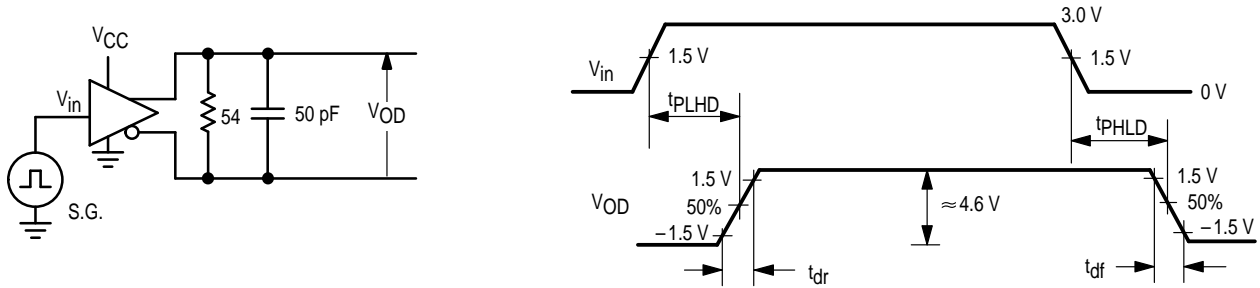
Figure 1. V$_{DD}$ Measurement
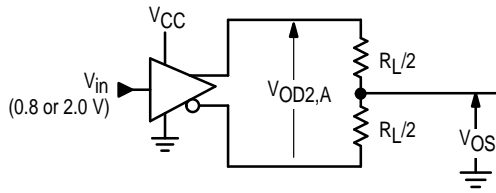
Figure 2. Common Mode Test
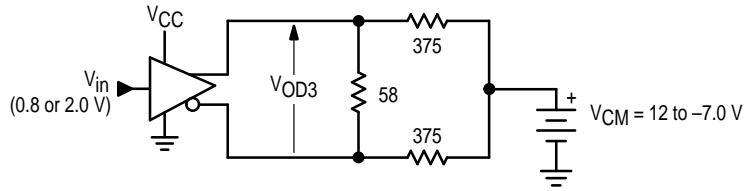
Figure 3. Propagation Delay, Single–Ended Outputs
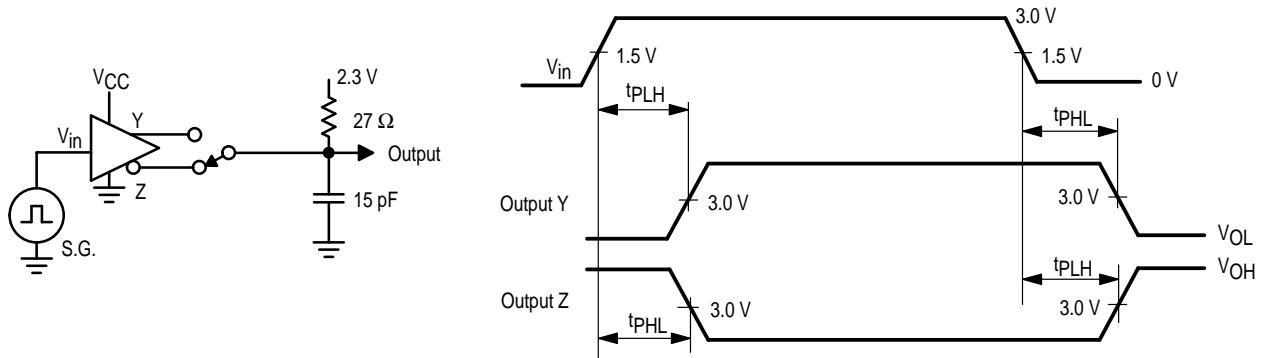
Figure 4. Propagation Delay, Differential Outputs

NOTES: 1. S.G. set to: f $\leq$ 1.0 MHz; duty cycle = 50%; t$_r$, t$_f$, $\leq$ 5.0 ns.
2. t$_{SK1}$ = $|$t$_{PLHD}$ − t$_{PHLD}$$|$ for each driver.
3. t$_{SK2}$ computed by subtracting the shortest t$_{PLHD}$ from the longest t$_{PLHD}$ of the 4 drivers within a package.
4. t$_{SK3}$ computed by subtracting the shortest t$_{PHLD}$ from the longest t$_{PHLD}$ of the 4 drivers within a package.

Figure 5. Enable Timing, Single–Ended Outputs

Figure 6. Enable Timing, Differential Outputs

NOTES: 1. S.G. set to: f ≤ 1.0 MHz; duty cycle = 50%; t_f, t_f, ≤ 5.0 ns.
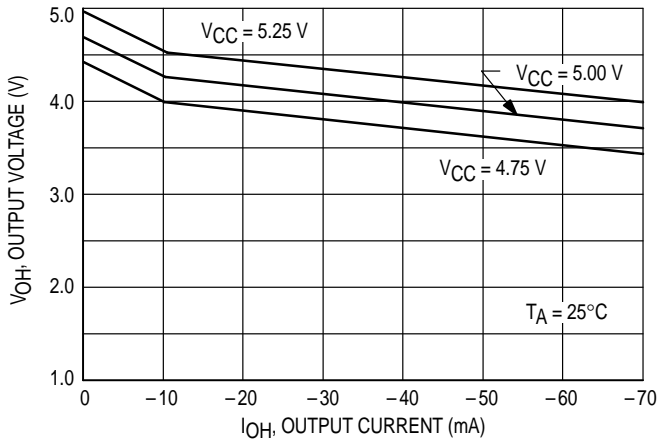2. V_{in} is inverted for Enable measurements.

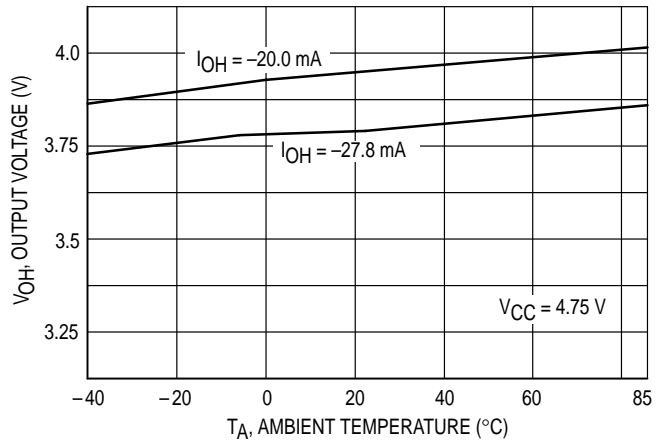**Figure 7. Single–Ended Output Voltage
versus Output Sink Current**

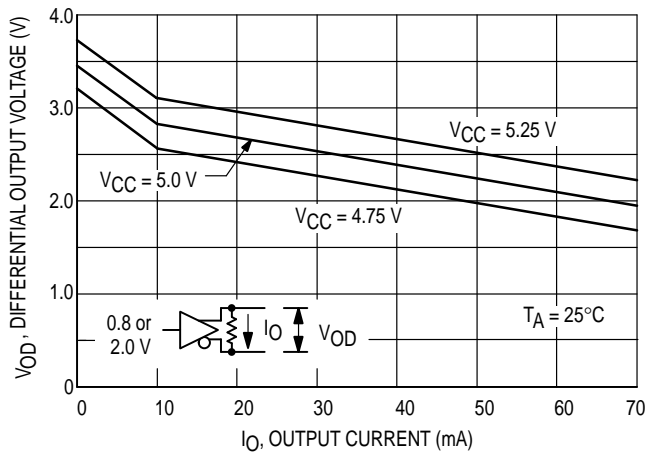**Figure 8. Single–Ended Output Voltage
versus Temperature**

**Figure 9. Single–Ended Output Voltage
versus Output Source Current**

**Figure 10. Single–Ended Output
Voltage versus Temperature**

**Figure 11. Output Differential Voltage
versus Load Current**

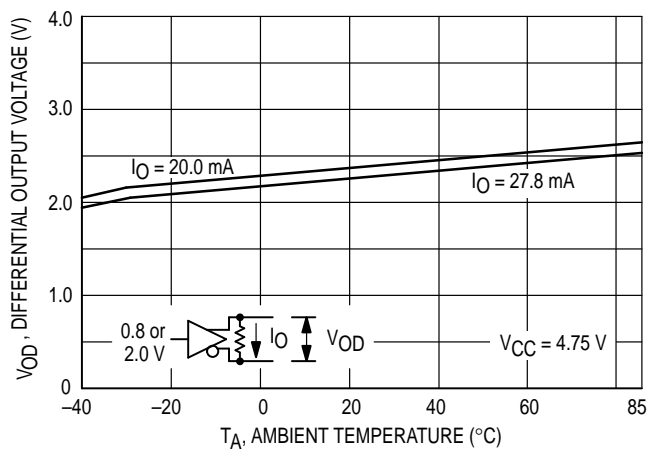**Figure 12. Output Differential Voltage
versus Temperature**

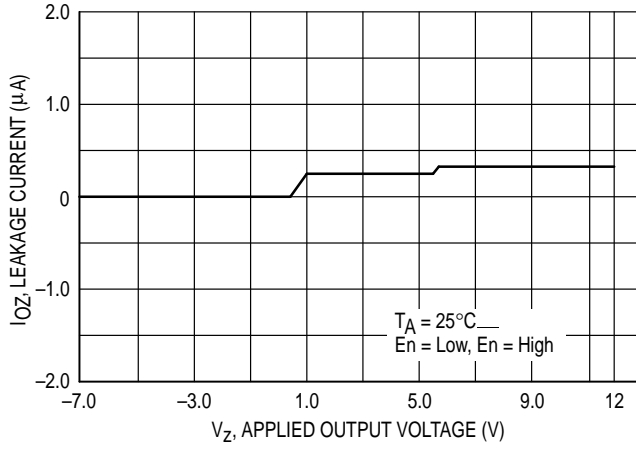**Figure 13. Output Leakage Current
versus Output Voltage**

**Figure 14. Output Leakage Current
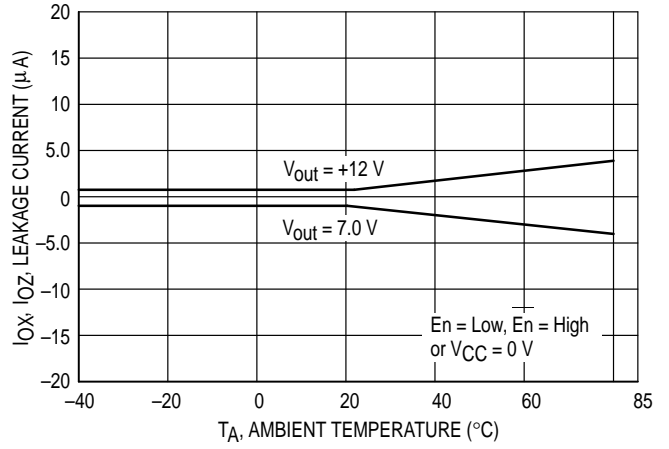versus Temperature**
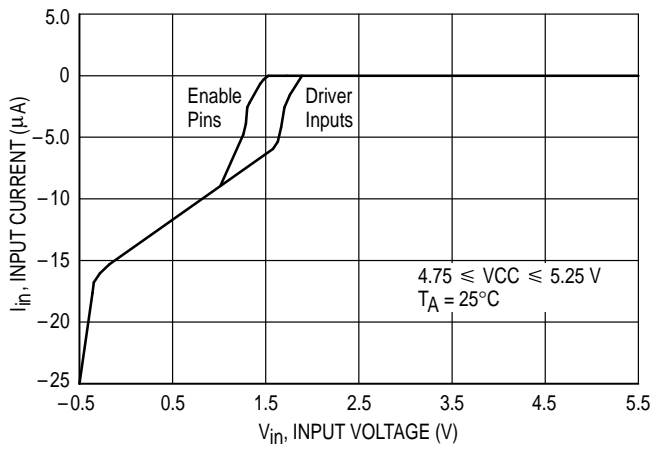

**Figure 15. Input Current
versus Input Voltage**

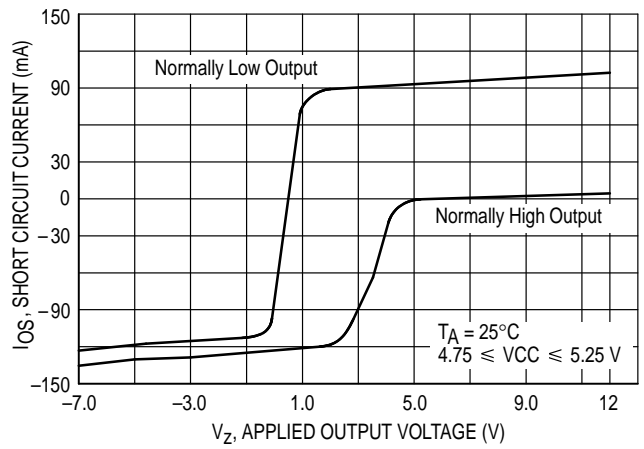**Figure 16. Short Circuit Current
versus Common Mode Voltage**

APPLICATIONS INFORMATION

Description

The MC75172B and MC75174B are differential line drivers designed to comply with EIA–485 Standard (April 1983) for use in balanced digital multipoint systems containing multiple drivers. The drivers also comply with EIA–422–A and CCITT Recommendations V.11 and X.27. The drivers meet the EIA–485 requirement for protection from damage in the event that two or more drivers attempt to transmit data simultaneoulsy on the same cable. Data rates in excess of 10 MBPS are possible, depending on the cable length and cable characteristics. A single power supply, 5.0 V, ±5%, is required at a nominal current of 60 mA, plus load currents.

Outputs

Each output (when active) will be a low or a high voltage, which depends on the input state and the load current (see Table 1, 2 and Figures 7 to 10). The graphs apply to each driver, regardless of how many other drivers within the package are supplying load current.

Table 1. MC75172B Truth Table

Data Input	Enables		Outputs	
	EN	EN	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

Table 2. MC75174B Truth Table

Data Input	Enable	Outputs	
		Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

H = Logic high, L = Logic low, X = Irrelevant, Z = High impedance

The two outputs of a driver are always complementary. A "high" output can only source current out, while a "low" output can only sink current (except for short circuit current – see Figure 16).

The outputs will be in the high impedance mode when:

a) the Enable inputs are set according to Table 1 or 2;

b) V_{CC} is less than 1.5 V;

c) the junction temperature exceeds the trip point of the thermal shutdown circuit (see below). When in this condition, the output's source and sink capability are shut off, and only leakage currents will flow (see Figures 13, 14). Disabled outputs may be taken to any voltage between –7.0 V and 12 V without damage.

The drivers are protected from short circuits by two methods:

a) Current limiting is provided at each output, in both the source and sink direction, for shorts to any voltage within the range of 12 V to –7.0 V, with respect to circuit ground (see Figure 16). The short circuit current will flow until the fault is removed, or until the thermal shutdown circuit activates (see below). The current limiting circuit has a negative temperature coefficient and requires no resetting upon removal of the fault condition.

b) A thermal shutdown circuit disables the outputs when the junction temperature reaches 150°C, ±20°C. The thermal shutdown circuit has a hysteresis of ≈ 12°C to prevent oscillations. When this circuit activates, the output stage of each driver is put into the high impedance mode, thereby shutting off the output currents. The remainder of the internal circuitry remains biased. The outputs will become active once again as the IC cools down.

Driver Inputs

The driver inputs determine the state of the outputs in accordance with Tables 1 and 2. The driver inputs have a nominal threshold of 1.2 V, and their voltage must be kept within the range of 0 V to V_{CC} for proper operation. If the voltage is taken more than 0.5 V below ground, excessive currents will flow, and proper operation of the drivers will be affected. An open pin is equivalent to a logic high, but good design practices dictate that inputs should never be left open. The characteristics of the driver inputs are shown in Figure 15. This graph is not affected by the state of the Enable pins.

Enable Logic

Each driver's outputs are active when the Enable inputs (Pins 4 and 12) are true according to Tables 1 and 2.

The Enable inputs have a nominal threshold of 1.2 V and their voltage must be kept within the range of 0 V to V_{CC} for proper operation. If the voltage is taken more than 0.5 V below ground, excessive currents will flow, and proper operation of the drivers will be affected. An open pin is equivalent to a logic high, but good design practices dictate that inputs should never be left open. The Enable input characteristics are shown in Figure 15.

Operating Temperature Range

The minimum ambient operating temperature is listed as –40°C to meet EIA–485 specifications, and 0°C to meet EIA–422–A specifications. The higher V_{OD} required by EIA–422–A is the reason for the narrower temperature range.

The maximum ambient operating temperature (applicable to both EIA–485 and EIA–422–A) is listed as 85°C. However, a lower ambient may be required depending on system use (i.e. specifically how many drivers within a package are used) and at what current levels they are operating. The maximum power which may be dissipated within the package is determined by:

$$PD_{max} = \frac{T_{Jmax} - T_A}{R_{\theta JA}}$$

where: $R_{\theta JA}$ = package thermal resistance (typical 70°C/W for the DIP package, 85°C/W for SOIC package);

T_{Jmax} = max. operating junction temperature, and

T_A = ambient temperature.

Since the thermal shutdown feature has a trip point of 150°C, ±20°C, T_{Jmax} is selected to be 130°C. The power dissipated within the package is calculated from:

PD $= \{[(V_{CC} - V_{OH}) \bullet I_{OH}] + V_{OL} \bullet I_{OL})\}$ each driver $+ (V_{CC} \bullet I_{CC})$

where: V_{CC} = the supply voltage;

V_{OH}, V_{OL} are measured or estimated from Figures 7 to 10;

I_{CC} = the quiescent power supply current (typical 60 mA).

As indicated in the equation, the first term (in brackets) must be calculated and summed for each of the four drivers, while the last term is common to the entire package.

Example 1: T_A = 25°C, $I_{OL} = I_{OH}$ = 55 mA for each driver, V_{CC} = 5.0 V, DIP package. How many drivers per package can be used?

Maximum allowable power dissipation is:

$$PD_{max} = \frac{130°C - 25°C}{70°C/W} = 1.5 \text{ W}$$

Since the power supply current of 60 mA dissipates 300 mW, that leaves 1.2 W (1.5 W – 0.3 W) for the drivers. From Figures 7 and 9, $V_{OL} \approx 1.75$ V, and $V_{OH} \approx 3.85$ V. The power dissipated in each driver is:

$\{(5.0 – 3.85) \bullet 0.055\} + (1.75 \bullet 0.055) = 160$ mW.

Since each driver dissipates 160 mW, the four drivers per package could be used in this application

Example 2: T_A = 85°C, I_{OL} = 27.8 mA, I_{OH} = 20 mA for each driver, V_{CC} = 5.0 V, SOIC package. How many drivers per package can be used?

Maximum allowable power dissipation is:

$$PD_{max} = \frac{130°C - 85°C}{85°C/W} = 0.53 \text{ W}$$

Since the power supply current of 60 mA dissipates 300 mW, that leaves 230 mW (530 mW – 300 mW) for the drivers. From Figures 8 and 10 (adjusted for V_{CC} = 5.0 V), $V_{OL} \approx 1.38$ V, and $V_{OH} \approx 4.27$ V. The power dissipated in each driver is:

$\{(5.0 – 4.27) \bullet 0.020\} + (1.38 \bullet 0.0278) = 53$ mW

Since each driver dissipates 53 mW, the use of all four drivers in a package would be marginal. Options include reducing the load current, reducing the ambient temperature, and/or providing a heat sink.

System Requirements

EIA–485 requires each driver to be capable of transmitting data differentially to at least 32 unit loads, plus an equivalent DC termination resistance of 60Ω, over a common mode voltage of –7.0 to 12 V. A unit load (U.L.), as defined by EIA–485, is shown in Figure 17.

Figure 17. Unit Load Definition
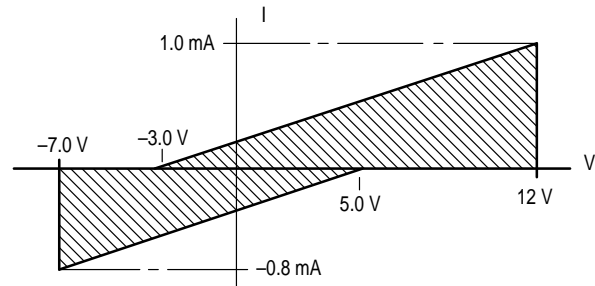
Reprinted from EIA–485, Electronic Industries Association, Washington,DC.

A load current within the shaded regions represents an impedance of less than one U.L., while a load current of a magnitude outside the shaded area is greater than one U.L. A system's total load is the sum of the unit load equivalents of each receiver's input current, and each disabled driver's output leakage current. The 60Ω termination resistance mentioned above allows for two 120Ω terminating resistors.

Using the EIA–485 requirements (worst case limits), and the graphs of Figures 7 and 9, it can be determined that the maximum current an MC75172B or MC75174B driver will source or sink is ≈65 mA.

System Example

An example of a typical EIA–485 system is shown in Figure 18. In this example, it is assumed each receiver's input characteristics correspond to 1.0 U.L. as defined in Figure 17. Each "off" driver, with a maximum leakage of ±50 μA over the common mode range, presents a load of ≈0.06 U.L. The total load for the active driver is therefore 8.3 unit loads, plus the parallel combination of the two terminating resistors (60Ω). It is up to the system software to control the driver Enable pins to ensure that only one driver is active at any time.
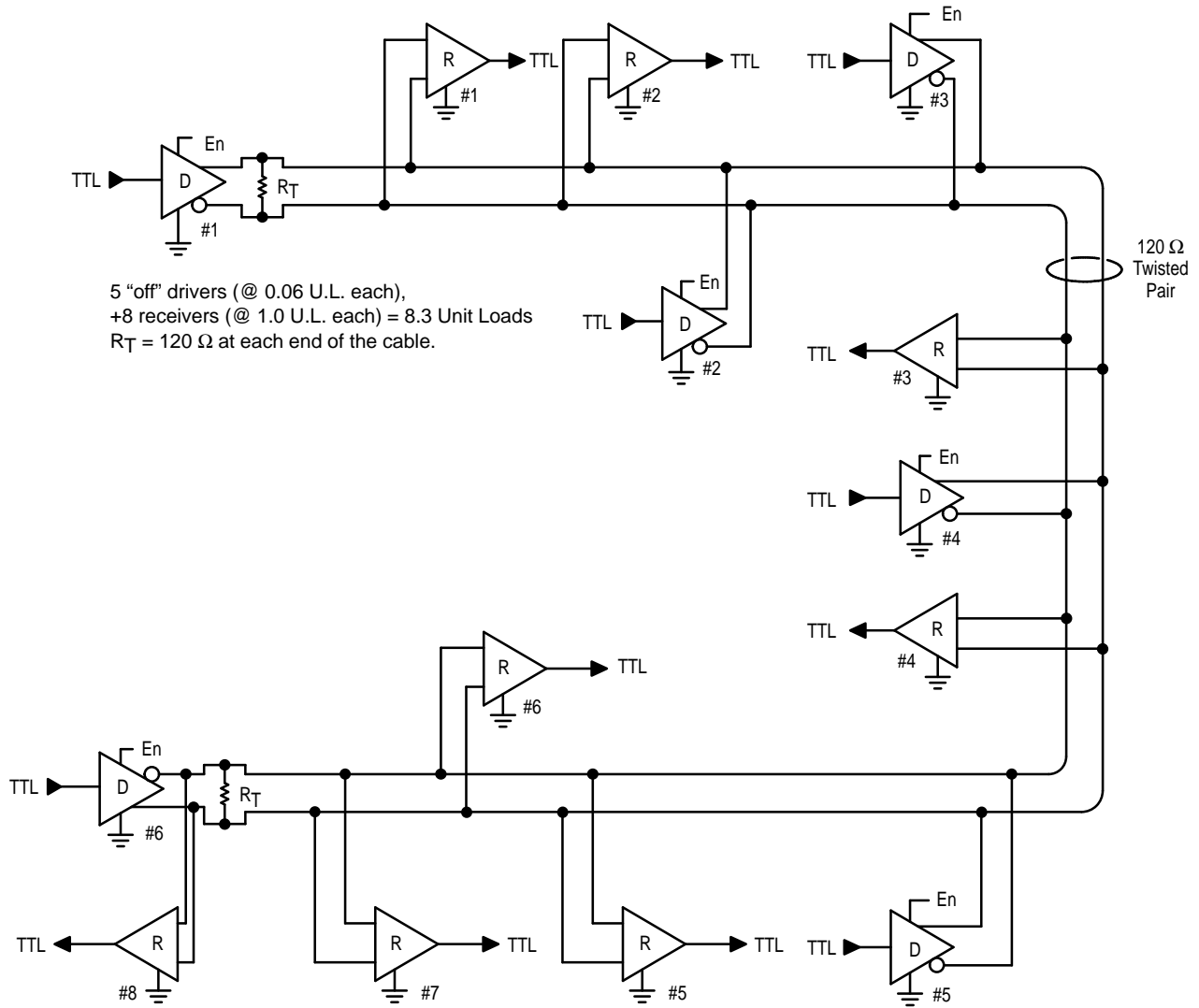
Termination Resistors

Transmission line theory states that, in order to preserve the shape and integrity of a waveform traveling along a cable, the cable must be terminated in an impedance equal to its characteristic impedance. In a system such as that depicted in Figure 18, in which data can travel in both directions, both physical ends of the cable must be terminated. Stubs, leading to each receiver and driver, should be as short as possible.

Leaving off the terminations will generally result in reflections which can have amplitudes of several volts above V_{CC} or below ground. These overshoots and undershoots can disrupt the driver and/or receiver operation, create false data, and in some cases damage components on the bus.

Figure 18. Typical EIA–485 System

5 "off" drivers (@ 0.06 U.L. each),
+8 receivers (@ 1.0 U.L. each) = 8.3 Unit Loads
R_T = 120 Ω at each end of the cable.

NOTES: 1. Terminating resistors R_T must be located at the physical ends of the cable.
2. Stubs should be as short as possible.
3. Circuit ground of all drivers and receivers must be connected via a dedicated wire within the cable. Do not rely on chassis ground or power line ground.

Comparing System Requirements

Characteristic	Symbol	EIA–485	EIA–422–A	V.11 and X.27
GENERATOR (DRIVER)				
Output Impedance (Note 1)	Z_{out}	Not Specified	$< 100\ \Omega$	50 10 100 Ω

Open Circuit Voltage
  Differential
  Single–Ended
	V_{OCD}
	V_{OCS}
		1.5 to 6.0 V
		< 6.0 V
			$\leqslant 6.0$ V
			$\leqslant 6.0$ V
				$\leqslant 6.0$ V, w/3.9 kΩ, Load
				$\leqslant 6.0$ V, w/3.9 kΩ, Load

Loaded Differential Voltage	V_{OD}	1.5 to 5.0 V, w/54 Ω load	$\geqslant 2.0$ V or $\geqslant 0.5$ V_{OCD}, w/100 Ω load	$\geqslant 2.0$ V or $\geqslant 0.5$ V_{OCD}, w/100 Ω load
Differential Voltage Balance	ΔV_{OD}	< 200 mV	$\leqslant 400$ mV	< 400 mV
Output Common Mode Range	V_{CM}	-7.0 to $+12$ V	Not Specified	Not Specified
Offset Voltage	V_{OS}	$-1.0 < V_{OS} < 3.0$ V	$\leqslant 3.0$ V	$\leqslant 3.0$ V
Offset Voltage Balance	ΔV_{OS}	< 200 mV	$\leqslant 400$ mV	< 400 mV
Short Circuit Current	I_{OS}	$\leqslant 250$ mA for -7.0 to 12 V	$\leqslant 150$ mA to ground	$\leqslant 150$ mA to ground
Leakage Current ($V_{CC} = 0$)	I_{OLK}	Not Specified	$\leqslant 100$ µA to -0.25 V thru 6.0 V	$\leqslant 100$ µA to ± 0.25 V
Output Rise/Fall Time (Note 2)	t_r, t_f	$\leqslant 0.3\ T_B$, w/54 Ω/1150 pF load	$\leqslant 0.1\ T_B$ or $\leqslant 20$ ns, w/100 Ω load	$\leqslant 0.1\ T_B$ or $\leqslant 20$ ns, w/100 Ω load
RECEIVER				
Input Sensitivity	V_{th}	± 200 mV	± 200 mV	± 300 mV
Input Bias Voltage	V_{bias}	$\leqslant 3.0$ V	$\leqslant 3.0$ V	$\leqslant 3.0$ V
Input Common Mode Range	V_{cm}	-7.0 to 12 V	-7.0 to 7.0 V	-7.0 to 7.0 V
Dynamic Input Impedance	R_{in}	Spec number of U.L.	$\geqslant 4$ kΩ	$\geqslant 4$ kΩ

NOTES: 1. Compliance with V.11 and X.27 (Blue book) output impedance requires external resistors in series with the outputs of the MC75172B and MC75174B.
   2. T_B = Bit time.

Additional Information

    Copies of the EIA Recommendations (EIA–485 and EIA–422–A) can be obtained from the Electronics Industries Association, Washington, D.C. (202–457–4966). Copies of the CCITT Recommendations (V.11 and X.27) can be obtained from the United States Department of Commerce, Springfield, VA (703–487–4600).

OUTLINE DIMENSIONS

P SUFFIX
PLASTIC PACKAGE
CASE 648–08
ISSUE R
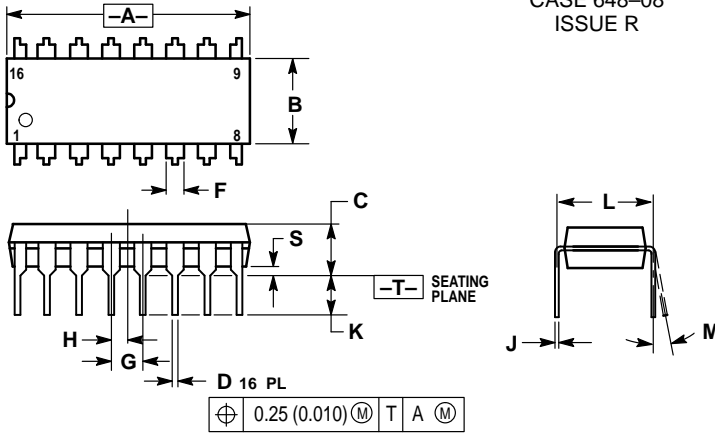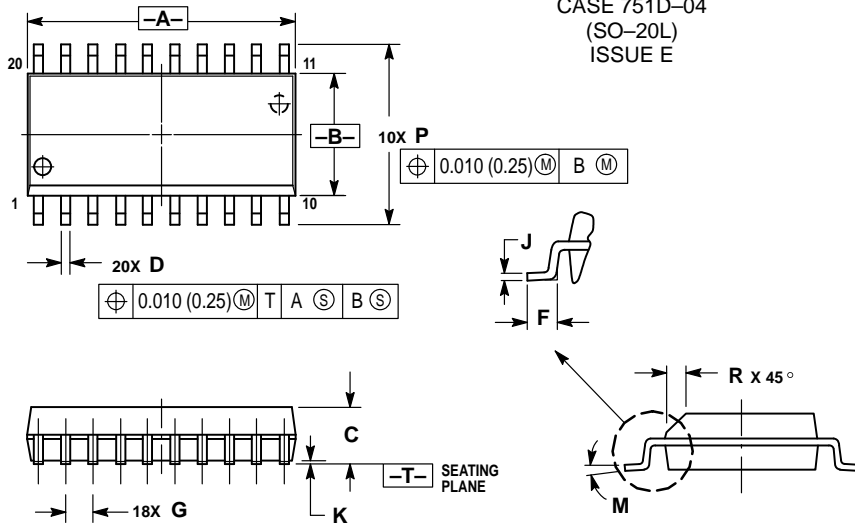
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

⊕ | 0.25 (0.010) Ⓜ | T | A Ⓜ

DW SUFFIX
PLASTIC PACKAGE
CASE 751D–04
(SO–20L)
ISSUE E

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.150 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

⊕ | 0.010 (0.25) Ⓜ | B Ⓜ

⊕ | 0.010 (0.25) Ⓜ | T | A Ⓢ | B Ⓢ

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	12.65	12.95	0.499	0.510
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

Ⓜ **MOTOROLA**

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