SN54CBT16209 . . . WD PACKAGE

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- **5-**Ω Switch Connection Between Two Ports
- TTL-Compatible Input Levels
- Package Options Include Plastic Thin Shrink Small-Outline (DGG), Thin Very Small-Outline (DGV), 300-mil Shrink Small-Outline (DL), and 380-mil Fine-Pitch Ceramic Flat (WD) Packages

description

The SN54CBT16209 and SN74CBT16209A devices provide 18 bits of high-speed TTL-compatible bus switching or exchanging. The low on-state resistance of the switches allows connections to be made with minimal propagation delay.

The devices operate as an 18-bit bus switch or a 9-bit bus exchanger, which provides data exchanging between the four signal ports via the data-select (S0, S1, S2) terminals.

The SN54CBT16209 is characterized for operation over the full military temperature range of -55° C to 125° C. The SN74CBT16209A is characterized for operation from -40° C to 85° C.

			FUNCTIO	NIABLE			
	INPUTS		INPUTS/	OUTPUTS	FUNCTION		
S2	S 1	S0	A1	A2	FUNCTION		
L	L	L	Z	Z	Disconnect		
L	L	Н	B1	Z	A1 port = B1 port		
L	Н	L	B2	Z	A1 port = B2 port		
L	Н	Н	Z	B1	A2 port = B1 port		
н	L	L	Z	B2	A2 port = B2 port		
н	L	Н	Z	Z	Disconnect		
н	Н	L	B1	B2	A1 port = B1 port A2 port = B2 port		
н	н	Н	B2	B1	A1 port = B2 port A2 port = B1 port		

FUNCTION TABLE



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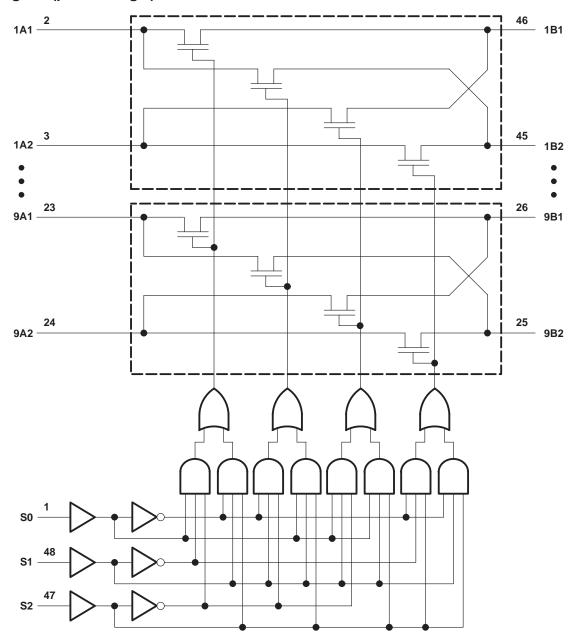
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logic diagram (positive logic)





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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC} Input voltage range, V _I (see Note 1)		
Continuous channel current		128 mA
Input clamp current, I _{IK} (V _I < 0)		–50 mA
Package thermal impedance, θ_{JA} (see Note 2):	: DGG package	89°C/W
	DGV package	93°C/W
	DL package	94°C/W
Storage temperature range, Tstg		–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

				SN74CBT1	UNIT	
		MIN	MAX	MIN	MAX	
VCC	Supply voltage	4	5.5	4	5.5	V
VIH	High-level control input voltage	2		2		V
VIL	Low-level control input voltage		0.8		0.8	V
ТА	Operating free-air temperature	-55	125	-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			MIN	түр‡	MAX	UNIT		
VIK		V _{CC} = 4.5 V,	I _I = -18 mA				-1.2	V
Ц		$V_{CC} = 0,$	V _I = 5.5 V				10	μA
		V _{CC} = 5.5 V,	$V_{I} = 5.5 \text{ V or GND}$				±1	μΑ
ICC		V _{CC} = 5.5 V,	$I_{O} = 0,$	$V_I = V_{CC}$ or GND			3	μΑ
∆ICC§	Control inputs	V _{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
Ci	Control inputs	V _I = 3 V or 0				4		pF
Cio(OFF)		$V_{O} = 3 V \text{ or } 0,$	S0, S1, or S2 = V_{CC}	· · · · · · · · · · · · · · · · · · ·		7.5		pF
r _{on} ¶		$V_{CC} = 4 V$, TYP at $V_{CC} = 4 V$	V _I = 2.4 V,	lı = 15 mA				
			$V_{1} = 0$	lı = 64 mA		4	8	Ω
		$V_{CC} = 4.5 V$	V VI = 0	lı = 30 mA		4	8	
			V _I = 2.4 V,	lı = 15 mA		6	15	

[‡] All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

\$ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

¶ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.



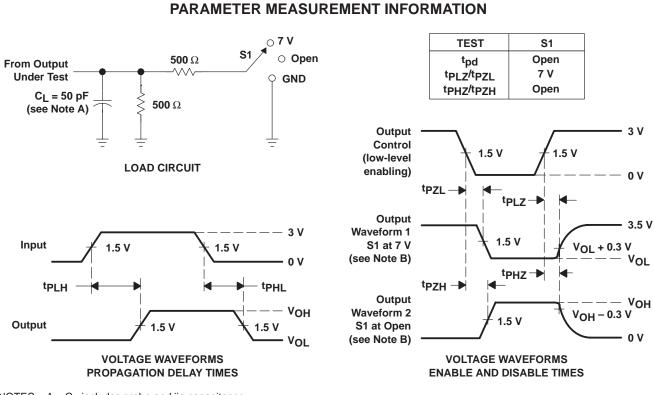
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switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

		TO (OUTPUT)	SN54CBT16209				SN74CBT16209A				
PARAMETER	FROM (INPUT)		V _{CC} = 4 V		V _{CC} = 5 V ± 0.5 V		V _{CC} = 4 V		V _{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd} †	A or B	B or A				0.8*		0.35		0.25	ns
^t pd	S	A or B		14	2	13.1		9.9	1.5	9	ns
ten	S	A or B		16	1.7	15.3		10.3	1.5	9.8	ns
^t dis	S	A or B		14.5	1	13.2		9.3	1.5	8.8	ns

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

[†] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).



NOTES: A. CL includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_Q = 50 Ω , t_r \leq 2.5 ns, t_f \leq 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{P7I} and t_{P7H} are the same as t_{en} .
- G. tPLH and tPHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



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