

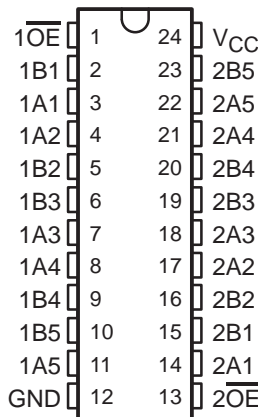
# SN74CBTD3384C

## 10-BIT FET BUS SWITCH WITH LEVEL SHIFTING 5-V BUS SWITCH WITH –2-V UNDERSHOOT PROTECTION

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- Undershoot Protection for Off-Isolation on A and B Ports Up To –2 V
- Integrated Diode to  $V_{CC}$  Provides 5-V Input Down To 3.3-V Output Level Shift
- Bidirectional Data Flow, With Near-Zero Propagation Delay
- Low ON-State Resistance ( $r_{on}$ ) Characteristics ( $r_{on} = 3 \Omega$  Typical)
- Low Input/Output Capacitance Minimizes Loading and Signal Distortion ( $C_{iO(OFF)} = 5 \text{ pF}$  Typical)
- Data and Control Inputs Provide Undershoot Clamp Diodes
- $V_{CC}$  Operating Range From 4.5 V to 5.5 V
- Data I/Os Support 0 to 5-V Signaling Levels (0.8-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, 5-V)
- Control Inputs Can be Driven by TTL or 5-V/3.3-V CMOS Outputs
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22 – 2000-V Human-Body Model (A114-B, Class II) – 1000-V Charged-Device Model (C101)
- Supports Both Digital and Analog Applications: Memory Interleaving, Bus Isolation, Low-Distortion Signal Gating

DB, DBQ, DGV, DW, OR PW PACKAGE  
(TOP VIEW)



### description/ordering information

#### ORDERING INFORMATION

T <sub>A</sub>	PACKAGE†	ORDERABLE PART NUMBER	TOP-SIDE MARKING	
–40°C to 85°C	SOIC – DW	Tube	SN74CBTD3384CDW	
		Tape and reel	SN74CBTD3384CDWR	
	SSOP – DB	Tube	SN74CBTD3384CDB	
		Tape and reel	SN74CBTD3384CDBR	
	SSOP (QSOP) – DBQ	Tape and reel	SN74CBTD3384CDBQR	CBTD3384C
	TSSOP – PW	Tube	SN74CBTD3384CPW	CC384C
Tape and reel		SN74CBTD3384CPWR		
TVSOP – DGV	Tape and reel	SN74CBTD3384CDGVR	CC384C	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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# SN74CBTD3384C

## 10-BIT FET BUS SWITCH WITH LEVEL SHIFTING

### 5-V BUS SWITCH WITH $-2$ -V UNDERSHOOT PROTECTION

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#### description/ordering information (continued)

The SN74CBTD3384C is a high-speed TTL-compatible FET bus switch with low ON-state resistance ( $r_{on}$ ), allowing for minimal propagation delay. This device features an integrated diode in series with  $V_{CC}$  to provide level shifting for 5-V input down to 3.3-V output levels. Active Undershoot-Protection Circuitry on the A and B ports of the SN74CBTD3384C provides protection for undershoot up to  $-2$  V by sensing an undershoot event and ensuring that the switch remains in the proper OFF state.

The SN74CBTD3384C is organized as two 5-bit bus switches with separate output-enable ( $1\overline{OE}$ ,  $2\overline{OE}$ ) inputs. It can be used as two 5-bit bus switches or as one 10-bit bus switch. When  $\overline{OE}$  is low, the associated 5-bit bus switch is ON, and the A port is connected to the B port, allowing bidirectional data flow between ports. When  $\overline{OE}$  is high, the associated 5-bit bus switch is OFF, and a high-impedance state exists between the A and B ports.

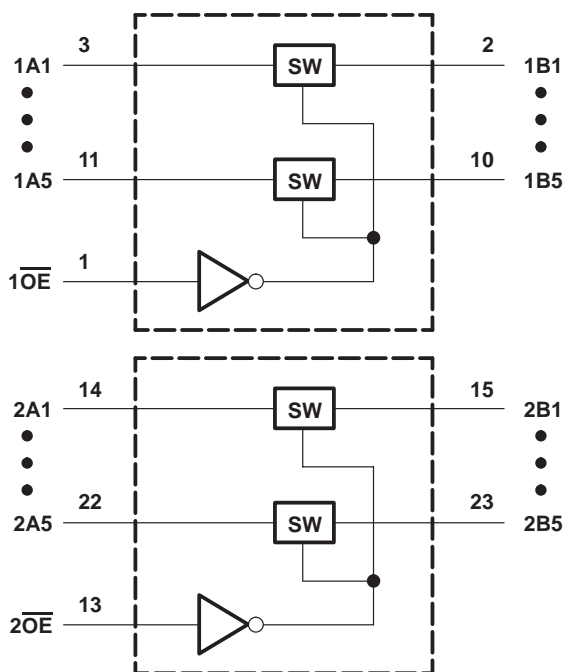
This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

FUNCTION TABLE  
(each 5-bit bus switch)

INPUT $\overline{OE}$	INPUT/OUTPUT A	FUNCTION
L	B	A port = B port
H	Z	Disconnect

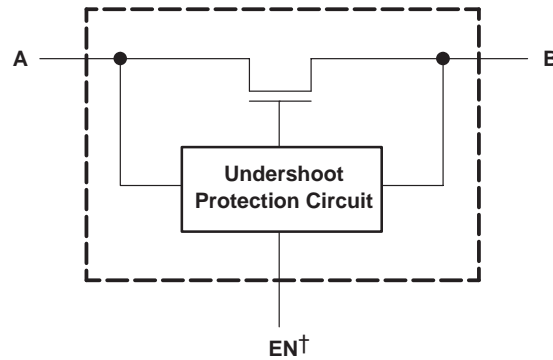
#### logic diagram (positive logic)



**SN74CBTD3384C**  
**10-BIT FET BUS SWITCH WITH LEVEL SHIFTING**  
**5-V BUS SWITCH WITH -2-V UNDERSHOOT PROTECTION**

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simplified schematic, each FET switch (SW)



† EN is the internal enable signal applied to the switch.

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡**

Supply voltage range, $V_{CC}$ .....	-0.5 V to 7 V
Control input voltage range, $V_{IN}$ (see Notes 1 and 2) .....	-0.5 V to 7 V
Switch I/O voltage range, $V_{I/O}$ (see Notes 1, 2, and 3) .....	-0.5 V to 7 V
Control input clamp current, $I_{IK}$ ( $V_{IN} < 0$ ) .....	-50 mA
I/O port clamp current, $I_{I/OK}$ ( $V_{I/O} < 0$ ) .....	-50 mA
ON-state switch current, $I_{I/O}$ (see Note 4) .....	$\pm 128$ mA
Continuous current through $V_{CC}$ or GND terminals .....	$\pm 100$ mA
Package thermal impedance, $\theta_{JA}$ (see Note 5): DB package .....	63°C/W
DBQ package .....	61°C/W
DGV package .....	86°C/W
DW package .....	46°C/W
PW package .....	88°C/W
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltages are with respect to ground unless otherwise specified.  
 2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
 3.  $V_I$  and  $V_O$  are used to denote specific conditions for  $V_{I/O}$ .  
 4.  $I_I$  and  $I_O$  are used to denote specific conditions for  $I_{I/O}$ .  
 5. The package thermal impedance is calculated in accordance with JESD 51-7.

**recommended operating conditions (see Notes 6 and 7)**

	MIN	MAX	UNIT
$V_{CC}$ Supply voltage	4.5	5.5	V
$V_{IH}$ High-level control input voltage	2	5.5	V
$V_{IL}$ Low-level control input voltage	0	0.8	V
$V_{I/O}$ Data input/output voltage	0	5.5	V
$T_A$ Operating free-air temperature	-40	85	°C

- NOTES: 6. All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.  
 7. In applications with fast edge rates, multiple outputs switching, and operating at high frequencies, the output may have little or no level-shifting effect.



# SN74CBTD3384C

## 10-BIT FET BUS SWITCH WITH LEVEL SHIFTING

### 5-V BUS SWITCH WITH -2-V UNDERSHOOT PROTECTION

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V <sub>IK</sub>	Control inputs	V <sub>CC</sub> = 4.5 V,	I <sub>IN</sub> = -18 mA			-1.8	V
V <sub>IKU</sub>	Data inputs	V <sub>CC</sub> = 5 V,	0 mA > I <sub>I</sub> ≥ -50 mA, V <sub>IN</sub> = V <sub>CC</sub> or GND, Switch OFF			-2	V
V <sub>OH</sub>		See Figures 4 and 5					
I <sub>IN</sub>	Control inputs	V <sub>CC</sub> = 5.5 V,	V <sub>IN</sub> = V <sub>CC</sub> or GND			±1	μA
I <sub>OZ</sub> ‡		V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0 to 5.5 V, V <sub>I</sub> = 0, Switch OFF, V <sub>IN</sub> = V <sub>CC</sub> or GND			±10	μA
I <sub>off</sub>		V <sub>CC</sub> = 0,	V <sub>O</sub> = 0 to 5.5 V, V <sub>I</sub> = 0			10	μA
I <sub>CC</sub>		V <sub>CC</sub> = 5.5 V,	I <sub>I/O</sub> = 0, V <sub>IN</sub> = V <sub>CC</sub> or GND, Switch ON or OFF			1.5	mA
ΔI <sub>CC</sub> §	Control inputs	V <sub>CC</sub> = 5.5 V,	One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND			2.5	mA
C <sub>in</sub>	Control inputs	V <sub>IN</sub> = 3 V or 0				3.5	pF
C <sub>io(OFF)</sub>		V <sub>I/O</sub> = 3 V or 0,	Switch OFF, V <sub>IN</sub> = V <sub>CC</sub> or GND			5	pF
C <sub>io(ON)</sub>		V <sub>I/O</sub> = 3 V or 0,	Switch ON, V <sub>IN</sub> = V <sub>CC</sub> or GND			12.5	pF
r <sub>on</sub> ¶		V <sub>CC</sub> = 4.5 V	V <sub>I</sub> = 0	I <sub>O</sub> = 64 mA	3	6	Ω
				I <sub>O</sub> = 30 mA	3	6	
			V <sub>I</sub> = 2.4 V,	I <sub>O</sub> = -15 mA	8	20	

V<sub>IN</sub> and I<sub>IN</sub> refer to control inputs. V<sub>I</sub>, V<sub>O</sub>, I<sub>I</sub>, and I<sub>O</sub> refer to data pins.

† All typical values are at V<sub>CC</sub> = 5 V (unless otherwise noted), T<sub>A</sub> = 25°C.

‡ For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.

§ This is the increase in supply current for each input that is at the specified voltage level, rather than V<sub>CC</sub> or GND.

¶ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 5 V ± 0.5 V		UNIT
			MIN	MAX	
t <sub>pd</sub> #	A or B	B or A	0.15		ns
t <sub>en</sub>	$\overline{OE}$	A or B	1.5	4.8	ns
t <sub>dis</sub>	$\overline{OE}$	A or B	1.5	4.8	ns

# The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

**SN74CBTD3384C**  
**10-BIT FET BUS SWITCH WITH LEVEL SHIFTING**  
**5-V BUS SWITCH WITH -2-V UNDERSHOOT PROTECTION**

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undershoot characteristics (see Figures 1 and 2)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$V_{OUTU}$	$V_{CC} = 5.5\text{ V}$ , Switch OFF, $V_{IN} = V_{CC}$ or GND	2	$V_{OH} - 0.3$		V

† All typical values are at  $V_{CC} = 5\text{ V}$  (unless otherwise noted),  $T_A = 25^\circ\text{C}$ .

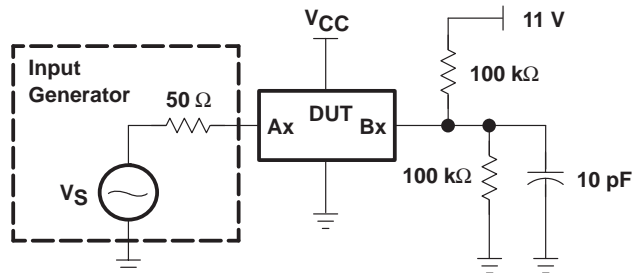


Figure 1. Device Test Setup

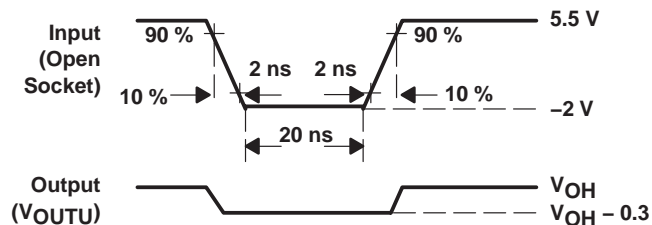
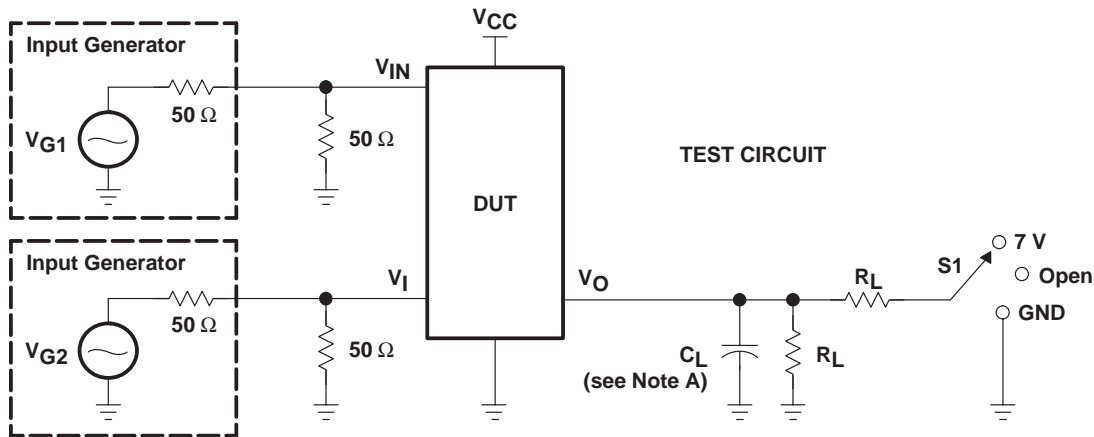


Figure 2. Transient Input Voltage ( $V_i$ ) and Output Voltage ( $V_{OUTU}$ ) Waveforms (Switch OFF)

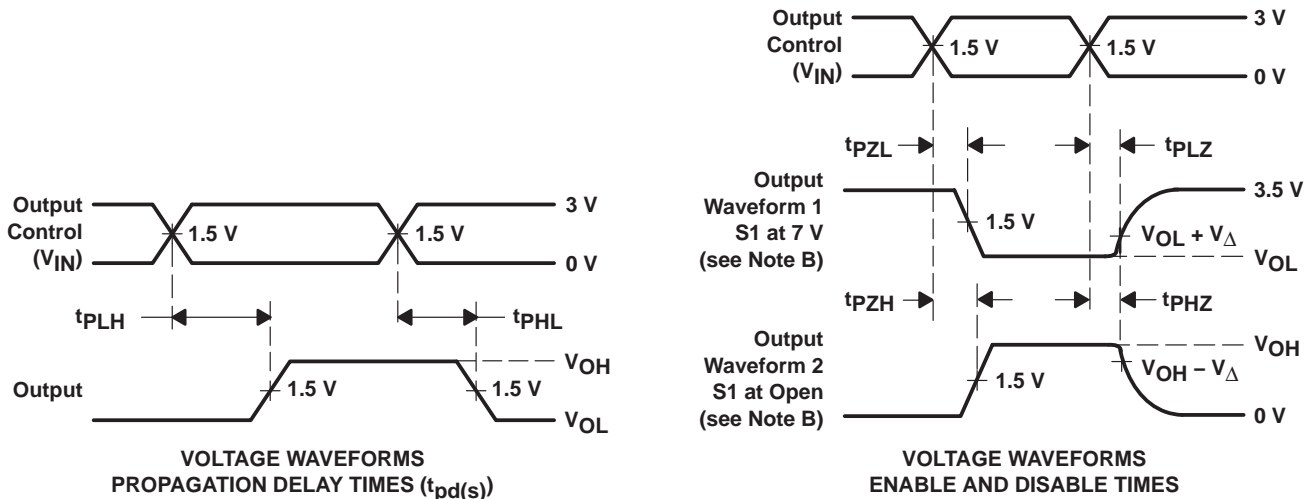
**SN74CBTD3384C**  
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**5-V BUS SWITCH WITH -2-V UNDERSHOOT PROTECTION**

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**PARAMETER MEASUREMENT INFORMATION  
 FOR LEVEL SHIFTER**



TEST	V <sub>CC</sub>	S1	R <sub>L</sub>	V <sub>I</sub>	C <sub>L</sub>	V <sub>Δ</sub>
t <sub>pd</sub> (s)	5 V ± 0.5 V	Open	500 Ω	V <sub>CC</sub> or GND	50 pF	
t <sub>PLZ</sub> /t <sub>PZL</sub>	5 V ± 0.5 V	7 V	500 Ω	GND	50 pF	0.3 V
t <sub>PHZ</sub> /t <sub>PZH</sub>	5 V ± 0.5 V	Open	500 Ω	V <sub>CC</sub>	50 pF	0.3 V



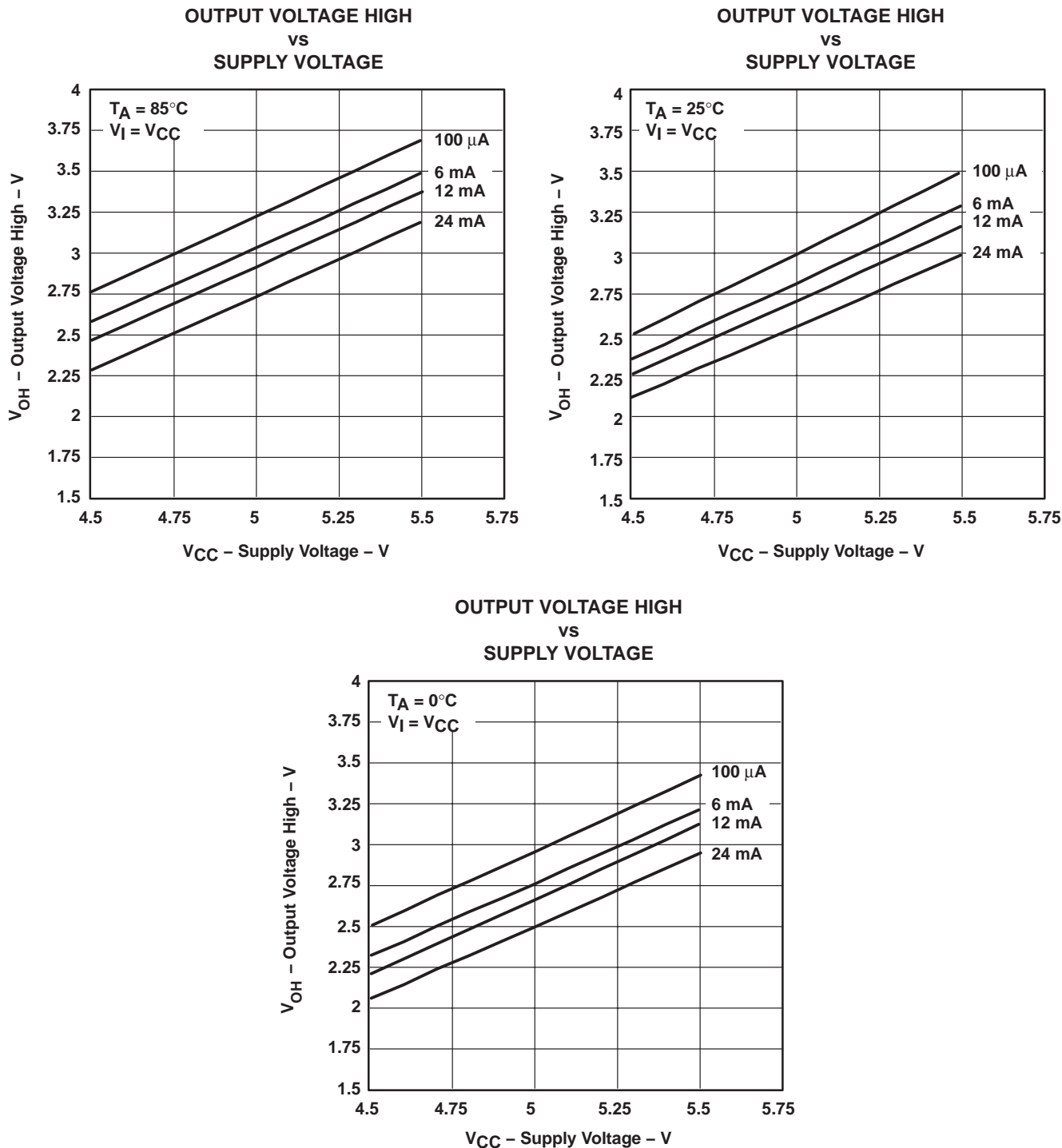
- NOTES:
- A. C<sub>L</sub> includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>O</sub> = 50 Ω, t<sub>r</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.
  - D. The outputs are measured one at a time with one transition per measurement.
  - E. t<sub>PLZ</sub> and t<sub>PHZ</sub> are the same as t<sub>dis</sub>.
  - F. t<sub>PZL</sub> and t<sub>PZH</sub> are the same as t<sub>en</sub>.
  - G. t<sub>PLH</sub> and t<sub>PHL</sub> are the same as t<sub>pd</sub>(s). The t<sub>pd</sub> propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
  - H. All parameters and waveforms are not applicable to all devices.

**Figure 3. Test Circuit and Voltage Waveforms**

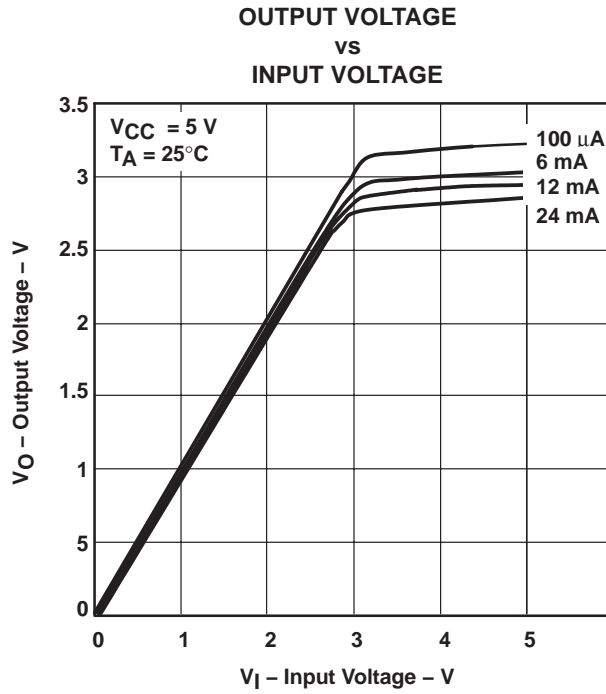
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**TYPICAL CHARACTERISTICS**



**TYPICAL CHARACTERISTICS (continued)**



**Figure 5. Data Output Voltage vs Data Input Voltage**



**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
74CBTD3384CDBQRE4	ACTIVE	SSOP/QSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
74CBTD3384CDGVRE4	ACTIVE	TVSOP	DGV	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBTD3384CDBQR	ACTIVE	SSOP/QSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
SN74CBTD3384CDBR	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBTD3384CDBRE4	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBTD3384CDGVR	ACTIVE	TVSOP	DGV	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBTD3384CDW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBTD3384CDWE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBTD3384CDWR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBTD3384CDWRE4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBTD3384CPW	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBTD3384CPWE4	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBTD3384CPWR	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBTD3384CPWRE4	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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DGV (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN

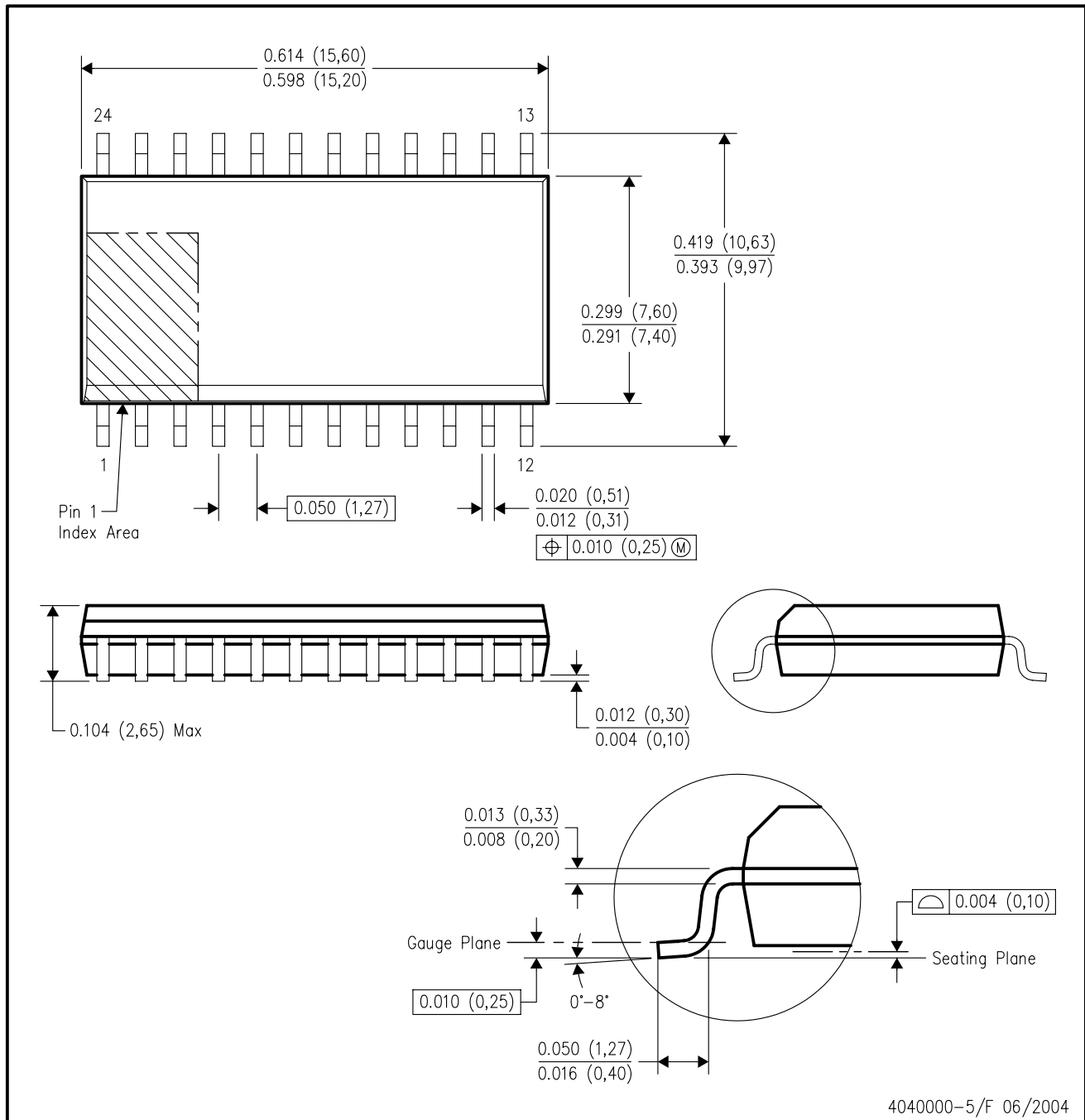


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- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

DW (R-PDSO-G24)

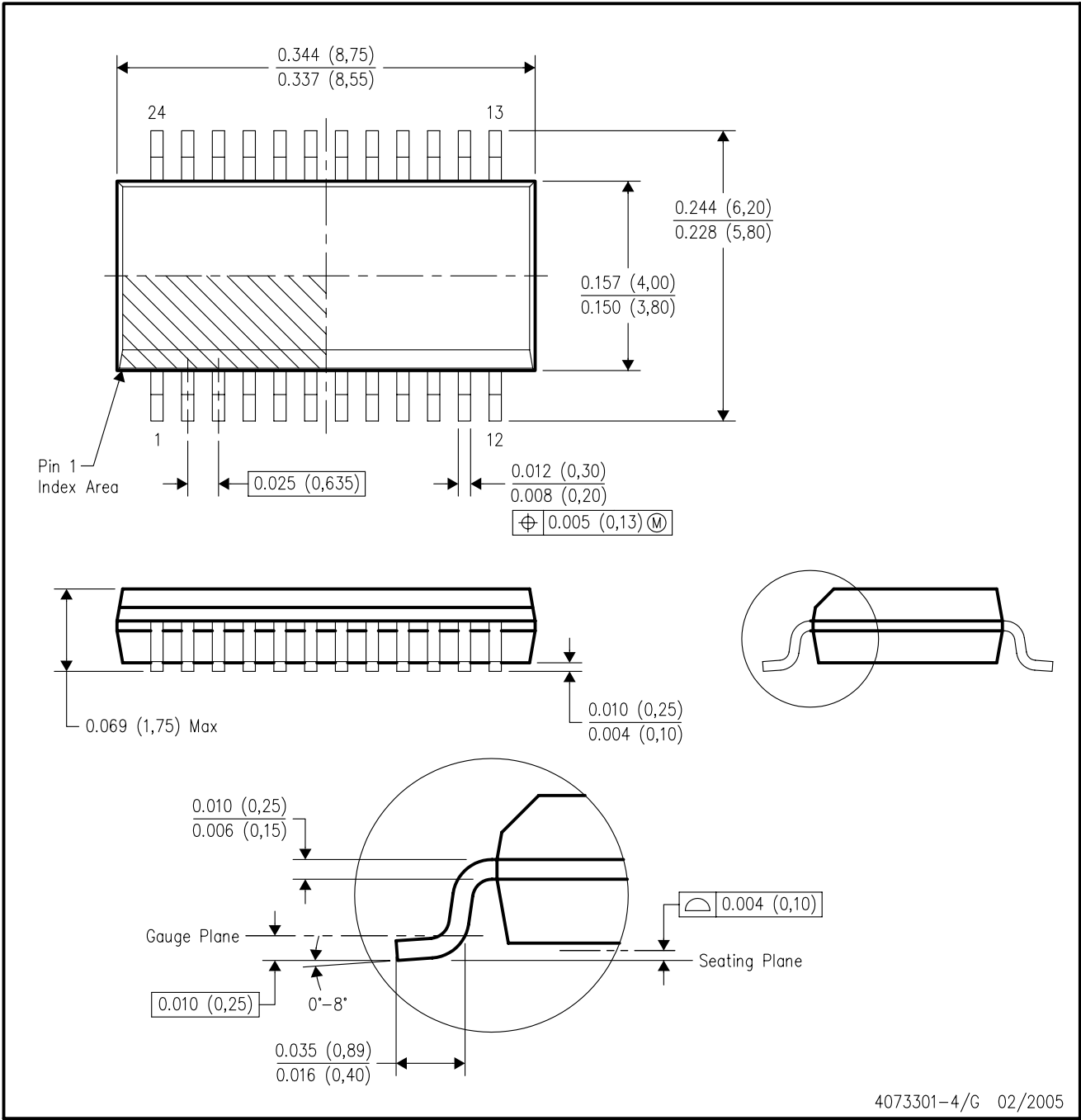
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AD.

DBQ (R-PDSO-G24)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
  - D. Falls within JEDEC MO-137 variation AE.

DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

PW (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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Mailing Address: Texas Instruments  
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