LTC1654

Dual 14-Bit Rail-to-Rail DAC in 16-Lead SSOP Package

April 2000

FEATURES

- **14-Bit Monotonic Over Temperature**
- **Individually Programmable Speed/Power:**
  3.5µs Settling Time at 750µA
  8µs Settling Time at 450µA
- Maximum Update Rate: 0.9MHz
- **Smallest Dual 14-Bit DAC: 16-Lead Narrow SSOP Package**
- Buffered True Rail-to-Rail Voltage Outputs
- **3V to 5V Single Supply Operation**
- User Selectable Gain
- Power-On Reset and Clear Function
- Schmitt Trigger On Clock Input Allows Direct Optocoupler Interface

APPLICATIONS

- Digital Calibration
- Industrial Process Control
- Automatic Test Equipment
- Offset/Gain Adjustment

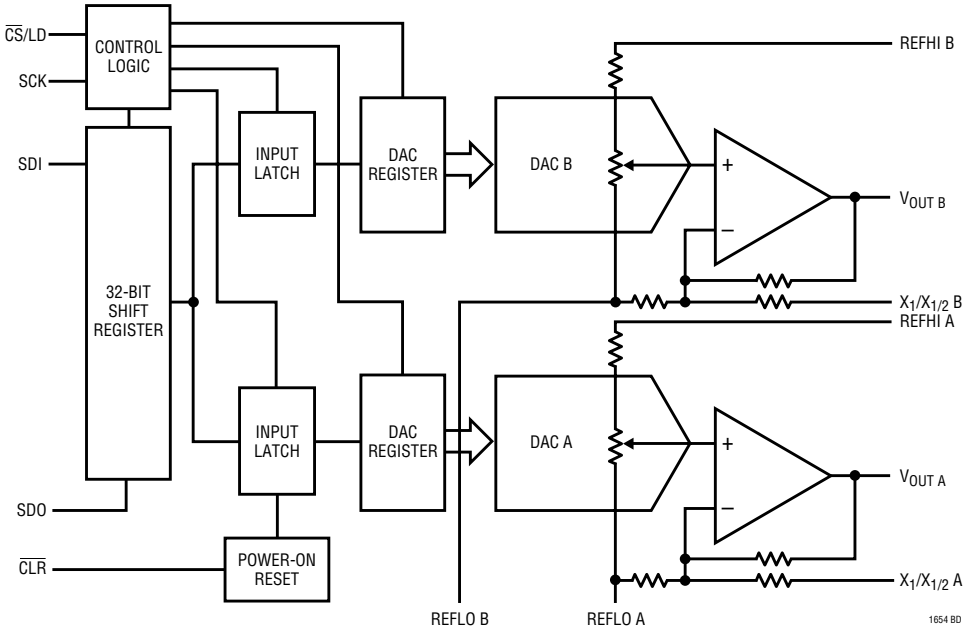
DESCRIPTION

The LTC®1654 is a dual, rail-to-rail voltage output, 14-bit digital-to-analog converter (DAC). It is available in a 16-lead narrow SSOP package, making it the smallest dual 14-bit DAC available. It includes output buffer amplifiers and a flexible serial interface.

The LTC1654 has REFHI pins for each DAC that can be driven up to V_{CC}. The output will swing from 0V to V_{CC} in gain of 1 configuration or $V_{CC}/2$ in gain of 1/2 configuration. It operates from a single 2.7V to 5.5V supply.

The LTC1654 has two programmable speeds: a FAST and SLOW mode with ±1LSB settling times of 3.5µs or 8µs respectively and supply currents of 750µA and 450µA in the two modes. The LTC1654 also has shutdown capability, power-on reset and clear function to 0V.

BLOCK DIAGRAM

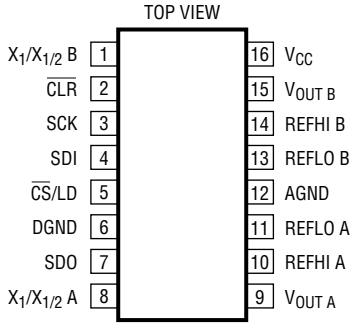


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{CC} to GND ..... –0.5V to 7.5V
TTL Input Voltage, REFHI,
REFLO, $X_1/X_{1/2}$ ..... –0.5V to 7.5V
V_{OUT}, SDO ..... –0.5V to (V_{CC} + 0.5V)
Operating Temperature Range
LTC1654C ..... 0°C to 70°C
LTC1654I ..... –40°C to 85°C
Maximum Junction Temperature ..... 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)..... 300°C

PACKAGE/ORDER INFORMATION



GN PACKAGE
16-LEAD NARROW PLASTIC SSOP

T_{JMAX} = 125°C, θ_{JA} = 95°C/W

ORDER PART NUMBER
LTC1654CGN LTC1654IGN
GN PART MARKING
1654 1654I

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V_{CC} = 2.7V to 5.5V, $V_{OUT\,A}$, $V_{OUT\,B}$ unloaded, REFHI A, REFHI B = 4.096V (V_{CC} = 5V), REFHI A, REFHI B = 2.048V (V_{CC} = 2.7V), REFLO = 0V, $X_1/X_{1/2}$ = 0V.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
DAC							
	Resolution		●	14			Bits
	Monotonicity		●	14			Bits
DNL	Differential Nonlinearity	Guaranteed Monotonic (Note 2)	●			±1	LSB
INL	Integral Nonlinearity	Integral Nonlinearity (Note 2)	●			±4	LSB
ZSE	Zero Scale Error	C Grade I Grade	● ●	0		6.5 9.0	mV mV
V_{OS}	Offset Error	Measured at Code 50, C Grade Measured at Code 50, I Grade	● ●			±6.5 ±9.0	mV mV
$V_{OS}TC$	Offset Error Tempco				±15		µV/°C
	Gain Error		●			±15	LSB
	Gain Error Drift				5		ppm/°C
Power Supply							
V_{CC}	Positive Supply Voltage	For Specified Performance	●	2.7		5.5	V
I_{CC}	Supply Current (SLOW/FAST)	2.7V ≤ V_{CC} ≤ 5.5V (Note 5) SLOW 2.7V ≤ V_{CC} ≤ 5.5V (Note 5) FAST 2.7V ≤ V_{CC} ≤ 3.3V (Note 5) SLOW 2.7V ≤ V_{CC} ≤ 3.3V (Note 5) FAST In Shutdown (Note 5)	● ● ● ● ●		450 750 250 450 7	800 1300 500 900 30	µA µA µA µA µA
Op Amp DC Performance							
	Short-Circuit Current Low	V_{OUT} Shorted to GND	●		70	120	mA
	Short-Circuit Current High	V_{OUT} Shorted to V_{CC}	●		80	120	mA
	Output Impedance to GND	Input Code = 0	●		40	200	Ω
	Output Line Regulation	Input Code = 16383, V_{CC} = 2.7V to 5.5V, V_{REF} = 2.048V	●			2.25	mV/V

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V_{CC} = 2.7V to 5.5V, $V_{OUT\,A}$, $V_{OUT\,B}$ unloaded, REFHI A, REFHI B = 4.096V (V_{CC} = 5V), REFHI A, REFHI B = 2.048V (V_{CC} = 2.7V), REFLO = 0V, $X_1/X_{1/2}$ = 0V.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
AC Performance							
	Voltage Output Slew Rate	(Note 3) SLOW (Note 3) FAST	● ●	0.20 1.25			V/µs V/µs
	Voltage Output Settling Time	(Note 4) to ±1LSB, SLOW (Note 4) to ±1LSB, FAST			8.0 3.5		µs µs
	Digital Feedthrough	(Note 8)			1		nV•s
	Midscale Glitch Impulse	DAC Switch Between 8000 and 7FFF			20		nV•s
	Output Noise Voltage Density	at 1kHz, SLOW at 1kHz, FAST			540 320		nV/√Hz nV/√Hz
Digital I/O							
V_{IH}	Digital Input High Voltage	V_{CC} = 5V	●	2.4			V
V_{IL}	Digital Input Low Voltage	V_{CC} = 5V	●			0.8	V
V_{OH}	Digital Output High Voltage	V_{CC} = 5V, I_{OUT} = –1mA, D_{OUT} Only	●	V_{CC} – 0.75			V
V_{OL}	Digital Output Low Voltage	V_{CC} = 5V, I_{OUT} = 1mA, D_{OUT} Only	●			0.4	V
V_{IH}	Digital Input High Voltage	V_{CC} = 3V	●	2.4			V
V_{IL}	Digital Input Low Voltage	V_{CC} = 3V	●			0.8	V
V_{OH}	Digital Output High Voltage	V_{CC} = 3V, I_{OUT} = –1mA, D_{OUT} Only	●	V_{CC} – 0.75			V
V_{OL}	Digital Output Low Voltage	V_{CC} = 3V, I_{OUT} = 1mA, D_{OUT} Only	●			0.4	V
I_{LEAK}	Digital Input Leakage	V_{IN} = GND to V_{CC}	●			±10	µA
C_{IN}	Digital Input Capacitance	(Note 6)				10	pF
Reference Input							
	Reference Input Resistance	REFHI to REFLO	●	30	60		kΩ
	Reference Input Range	(Notes 6, 7)	●	0		V_{CC}	V
	Reference Input Current	In Shutdown	●			1	µA
Switching Characteristics (V_{CC} = 4.5V to 5.5V)							
t_1	SDI Valid to SCK Setup		●	30			ns
t_2	SDI Valid to SCK Hold	(Note 6)	●	0			ns
t_3	SCK High Time	(Note 6)	●	15			ns
t_4	SCK Low Time	(Note 6)	●	15			ns
t_5	$\overline{CS}$/LD Pulse Width	(Note 6)	●	15			ns
t_6	LSB SCK to $\overline{CS}$/LD	(Note 6)	●	10			ns
t_7	$\overline{CS}$/LD Low to SCK	(Note 6)	●	10			ns
t_8	SDO Output Delay	C_{LOAD} = 100pF	●	5		100	ns
t_9	SCK Low to $\overline{CS}$/LD Low	(Note 6)	●	10			ns
Switching Characteristics (V_{CC} = 2.7V to 5.5V)							
t_1	SDI Valid to SCK Setup		●	45			ns
t_2	SDI Valid to SCK Hold	(Note 6)	●	0			ns
t_3	SCK High Time	(Note 6)	●	20			ns
t_4	SCK Low Time	(Note 6)	●	20			ns
t_5	$\overline{CS}$/LD Pulse Width	(Note 6)	●	20			ns
t_6	LSB SCK to $\overline{CS}$/LD	(Note 6)	●	15			ns
t_7	$\overline{CS}$/LD Low to SCK	(Note 6)	●	15			ns
t_8	SDO Output Delay	C_{LOAD} = 100pF	●	5		150	ns
t_9	SCK Low to $\overline{CS}$/LD Low	(Note 6)	●	15			ns

ELECTRICAL CHARACTERISTICS

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: Nonlinearity is defined from code 50 to code 16383 (full scale). See Applications Information.

Note 3: 100pF Load Capacitor

Note 4: DAC switched between code 200 and code 16383.

Note 5: Digital inputs at 0V or V_{CC}.

Note 6: Guaranteed by design.

Note 7: V_{OUT} can only swing from (GND + $|V_{OS}|$) to ($V_{CC} - |V_{OS}|$) when output is unloaded. See Applications Information.

Note 8: $\overline{CS}$/LD = 0, V_{OUT} = 4.096 and data is being clocked in.

PIN FUNCTIONS

$X_1/X_{1/2}$ B, $X_1/X_{1/2}$ A (Pins 1, 8): The Gain of 1 or Gain of 1/2 Pin. When this pin is tied to V_{OUT}, the output will swing up to REFHI/2 and when this pin is tied to REFLO, the output will swing up to REFHI. These pins should not be left floating.

$\overline{CLR}$ (Pin 2): The Asynchronous Clear Input.

SCK (Pin 3): The TTL Level Input for the Serial Interface Clock.

SDI (Pin 4): The TTL Level Input for the Serial Interface Data. Data on the SDI pin is latched into the shift register on the rising edge of the serial clock. The LTC1654 requires a 24-bit word. The first 8 bits are control/address followed by 16 data bits. The last two of the 16 data bits are don't cares. If daisy-chaining is desired, then a 32-bit data word can be used with the first 8 being don't cares and the following 24 bits as above.

$\overline{CS}$/LD (Pin 5): The TTL Level Input for the Serial Interface Enable and Load Control. When $\overline{CS}$/LD is low, the SCK signal is enabled, so the data can be clocked in. When $\overline{CS}$/LD is pulled high, the control/address bits are decoded.

DGND/AGND (Pins 6, 12): Digital and Analog Grounds.

SDO (Pin 7): The output of the shift register that becomes valid on the rising edge of the serial clock.

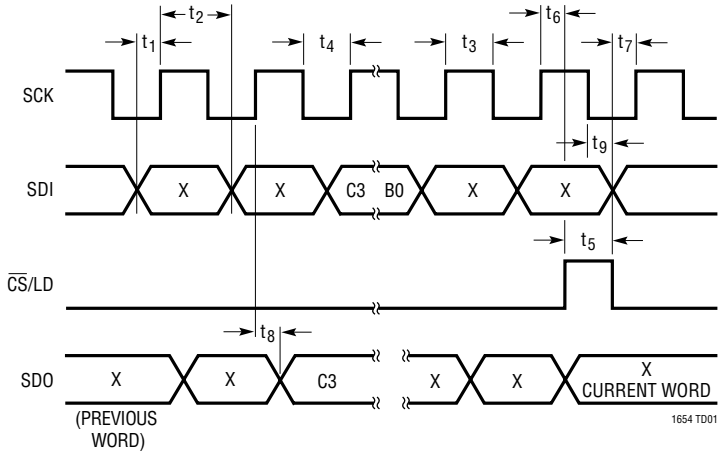
$V_{OUT\ A/B}$ (Pins 9, 15): The Buffered DAC Outputs.

REFHI A/B (Pins 10, 14): The Reference High Inputs of the LTC1654. There is a gain of 1 from this pin to the output in a gain of 1 configuration. In a gain of 1/2 configuration, there is a gain of 1/2 from this pin to V_{OUT}.

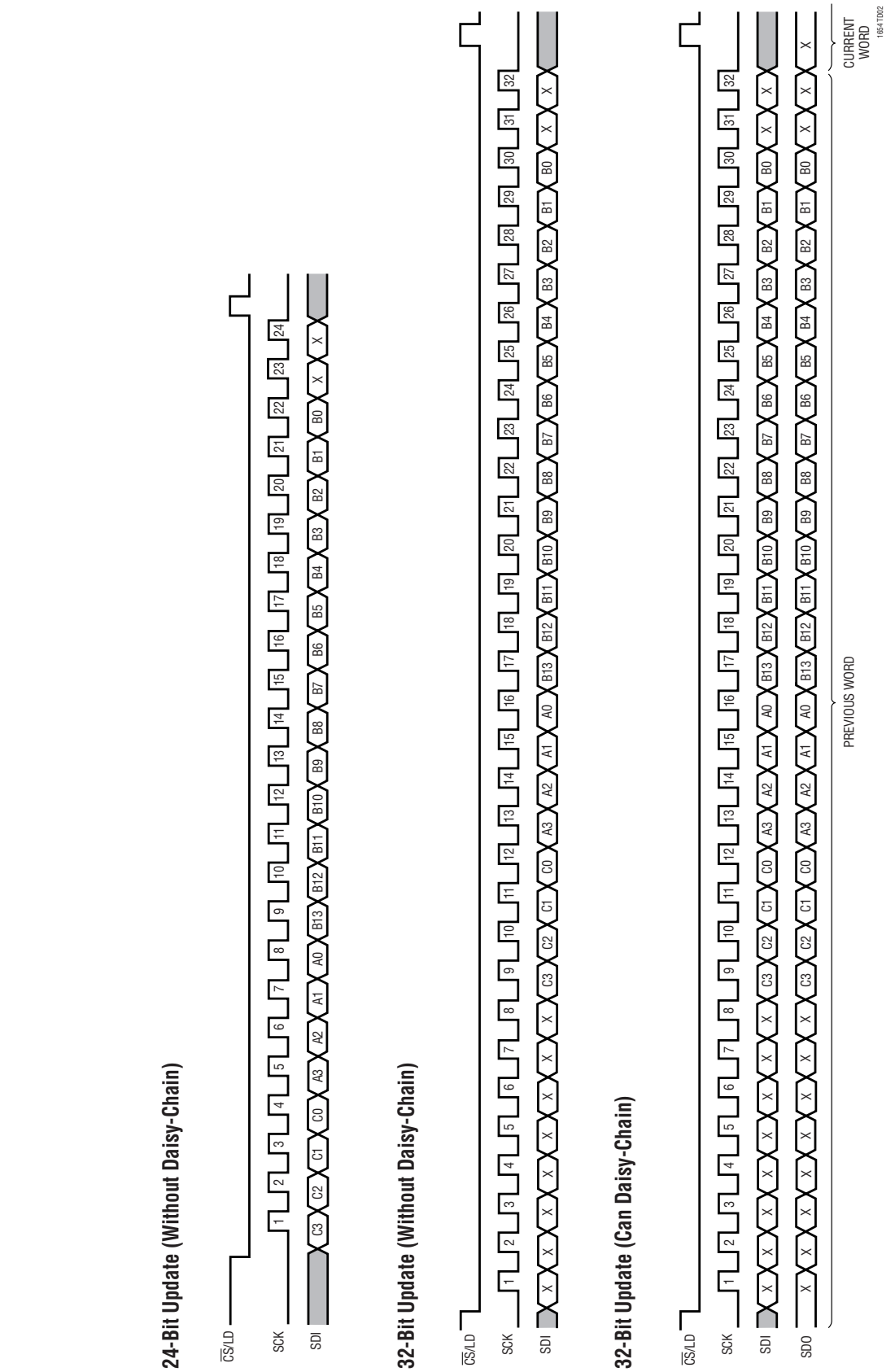
REFLO A/B (Pins 11, 13): The Reference Low Inputs of the LTC1654.

V_{CC} (Pin 16): The Positive Supply Input. $2.7V \leq V_{CC} \leq 5.5V$. Requires a 0.1µF bypass capacitor to ground.

TIMING DIAGRAMS



TIMING DIAGRAMS



OPERATION

Serial Interface

The data on the SDI input is loaded into the shift register on the rising edge of SCK. The MSB is loaded first. The Clock is disabled internally when $\overline{CS}$/LD is high. Note: SCK must be low before $\overline{CS}$/LD is pulled low to avoid an extra internal clock pulse.

If no daisy-chaining is required, the input word can be 24-bit wide, as shown in the timing diagrams. The 8 MSBs, which are loaded first, are the control and address bits followed by a 16-bit data word. The last two LSBs in the data word are don't cares. The input word can be a stream of three 8-bit wide segments as shown in the "24-Bit Update" timing diagram.

If daisy-chaining is required or if the input needs to be written in two 16-bit wide segments, then the input word can be 32 bits wide and the top 8 bits (MSBs) are don't cares. The remaining 24 bits are control/address and data. This is also shown in the timing diagrams. The buffered output of the internal 32-bit shift register is available on the SDO pin, which swings from GND to V_{CC}.

Multiple LTC1654s may be daisy-chained together by connecting the SDO pin to the SDI pin of the next IC. The SCK and $\overline{CS}$/LD signals remain common to all ICs in the daisy-chain. The serial data is clocked to all of the chips, then the $\overline{CS}$/LD signal is pulled high to update all DACs simultaneously.

Table 1 shows the truth table for the control/address bits. When the supplies are first applied, the LTC1654 uses SLOW mode, the outputs are set at 0V, and zeros are loaded into the 32-bit input shift register. Three examples are given to illustrate the DAC's operation:

1. **Load and update DAC A in FAST mode. Leave DAC B unchanged.** Perform the following sequence for the control, address and DATA bits:

   Step 1: Set DAC A in FAST mode

   $\overline{CS}$/LD ↓ clock in 0101 0000 XXXXXXXX XXXXXXXX; $\overline{CS}$/LD ↑

   Step 2: Load and update DAC A with DATA

   $\overline{CS}$/LD ↓ clock in 0011 0000 + DATA; $\overline{CS}$/LD ↑

2. **Load and update DAC A in SLOW mode. Power down DAC B.** Perform the following sequence for the control, address and DATA bits:

   Step 1: Set DAC A in SLOW mode

   $\overline{CS}$/LD ↓ clock in 0110 0000 XXXXXXXX XXXXXXXX; $\overline{CS}$/LD ↑

   Step 2: Load and update DAC A with DATA

   $\overline{CS}$/LD ↓ clock in 0011 0000 + DATA; $\overline{CS}$/LD ↑

   Step 3: Power down DAC B

   $\overline{CS}$/LD ↓ clock in 0100 0001 XXXXXXXX XXXXXXXX; $\overline{CS}$/LD ↑

3. **Power down both DACs at the same time.** Perform the following sequence for the control, address and DATA bits:

   Step 1: Power down both DACs simultaneously

   $\overline{CS}$/LD ↓ clock in 0100 1111 XXXXXXXX XXXXXXXX; $\overline{CS}$/LD ↑

Voltage Output

The LTC1654 comes complete with rail-to-rail voltage output buffer amplifiers. These amplifiers will swing to within a few millivolts of either supply rail when unloaded and to within a 300mV of either supply rail when sinking or sourcing 5mA.

There are two GAIN configuration modes for the LTC1654:

a) GAIN of 1: ($X_1/X_{1/2}$ tied to REFLO)

$$V_{OUT} = (V_{REFHI} - V_{REFLO})(SDI/16384) + V_{REFLO}$$

b) GAIN of 1/2: ($X_1/X_{1/2}$ tied to V_{OUT})

$$V_{OUT} = (1/2)(V_{REFHI} - V_{REFLO})(SDI/16384) + V_{REFLO}$$

The LTC 1654 has two SPEED modes: A FAST mode and a SLOW mode. When operating in the FAST mode, the output amplifiers will settle in 3.5μs (typ) to 14 bits on a 4V output swing. In the SLOW mode, they will settle in 8μs. The total supply current is 750μA in the FAST mode and 450μA in the SLOW mode.

OPERATION

Power Down

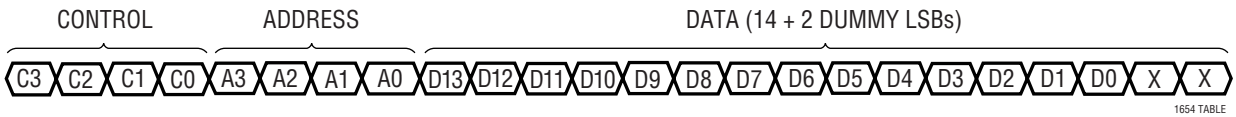
Each DAC can also be independently powered down to less than 5μA/DAC of supply current. The reference pin also goes into a high impedance state when the DAC is powered down and the reference current will drop to below 0.1μA. The amplifiers' output stage is also three-stated but the V_{OUT} pins still have the internal gain-setting resistors connected to them resulting in an effective resistance from V_{OUT} to REFLO. This resistance is typically 90k when the $X_1/X_{1/2}$ pin is tied to V_{OUT} and 36k when $X_1/X_{1/2}$ is tied to REFLO. Because of this resistance, V_{OUT} will go to V_{REFLO} when the DAC is powered down and V_{OUT} is unloaded.

Table 1.

CONTROL				
C3	**C2**	**C1**	**C0**	
0	0	0	0	Load Input Register n
0	0	0	1	Update (Power-Up) DAC Register n
0	0	1	0	Load Input Register n, Update (Power-Up) All
0	0	1	1	Load and Update n
0	1	0	0	Power Down n
0	1	0	1	Fast n (Speed States are Maintained Even If DAC is Put in Power-Down Mode)
0	1	1	0	Slow n (Default State is Slow When Supplies are Powered Up)
0	1	1	1	Reserved (Do Not Use)
1	0	0	0	Reserved (Do Not Use)
1	0	0	1	Reserved (Do Not Use)
1	0	1	0	Reserved (Do Not Use)
1	0	1	1	Reserved (Do Not Use)
1	1	0	0	Reserved (Do Not Use)
1	1	0	1	Reserved (Do Not Use)
1	1	1	0	Reserved (Do Not Use)
1	1	1	1	No Operation

ADDRESS (n)				
A3	**A2**	**A1**	**A0**	
0	0	0	0	DAC A
0	0	0	1	DAC B
0	0	1	0	Reserved (Do Not Use)
0	0	1	1	Reserved (Do Not Use)
0	1	0	0	Reserved (Do Not Use)
0	1	0	1	Reserved (Do Not Use)
0	1	1	0	Reserved (Do Not Use)
0	1	1	1	Reserved (Do Not Use)
1	0	0	0	Reserved (Do Not Use)
1	0	0	1	Reserved (Do Not Use)
1	0	1	0	Reserved (Do Not Use)
1	0	1	1	Reserved (Do Not Use)
1	1	0	0	Reserved (Do Not Use)
1	1	0	1	Reserved (Do Not Use)
1	1	1	0	Reserved (Do Not Use)
1	1	1	1	Both DACs

INPUT WORD



APPLICATIONS INFORMATION

Rail-to-Rail Output Considerations

In any rail-to-rail DAC, the output swing is limited to voltages within the supply range.

If the DAC offset is negative, the output for the lowest codes limits at 0V as shown in Figure 2b.

Similarly, limiting can occur near full scale when the REF pin is tied to V_{CC}. If $V_{REF} = V_{CC}$ and the DAC full-scale error (FSE) is positive, the output for the highest codes limits at V_{CC} as shown in Figure 2c. No full-scale limiting can occur if V_{REF} is less than (V_{CC} – FSE).

Offset and linearity are defined and tested over the region of the DAC transfer function where no output limiting can occur.

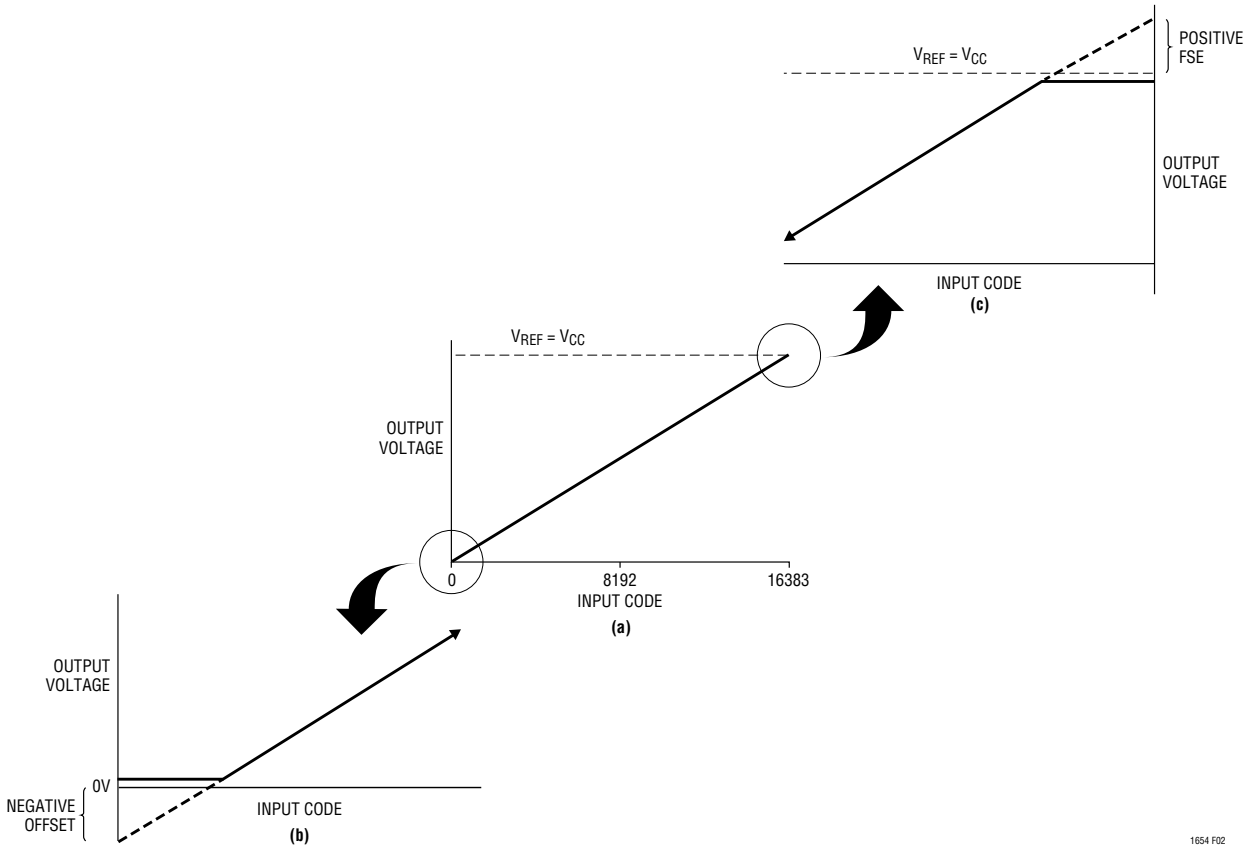


Figure 2. Effects of Rail-to-Rail Operation On a DAC Transfer Curve. (a) Overall Transfer Function (b) Effect of Negative Offset for Codes Near Zero Scale (c) Effect of Positive Full-Scale Error for Input Codes Near Full Scale When $V_{REF} = V_{CC}$

DEFINITIONS

Resolution (n): Resolution is defined as the number of digital input bits (n). It is also the number of DAC output states (2^n) that divide the full-scale range. Resolution does not imply linearity.

Full-Scale Voltage (V_{FS}): This is the output of the DAC when all bits are set to 1.

Voltage Offset Error (V_{OS}): Normally, DAC offset is the voltage at the output when the DAC is loaded with all zeros. The DAC can have a true negative offset, but because the part is operated from a single supply, the output cannot go below 0V. If the offset is negative, the output will remain near 0V resulting in the transfer curve shown in Figure 1.

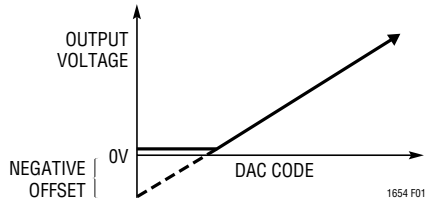


Figure 1. Effect of Negative Offset

The offset of the part is measured at the code that corresponds to the maximum offset specification:

$$V_{OS} = V_{OUT} - [(Code)(V_{FS})/(2^n - 1)]$$

Least Significant Bit (LSB): One LSB is the ideal voltage difference between two successive codes.

$$LSB = (V_{FS} - V_{OS})/(2^n - 1) = (V_{FS} - V_{OS})/16383$$

Nominal LSBs:

LTC1654 LSB = 4.09575V/16383 = 250µV

Zero-Scale Error (ZSE): The output voltage when the DAC is loaded with all zeros. Since this is a single supply part, this value cannot be less than 0V.

Integral Nonlinearity (INL): End-point INL is the maximum deviation from a straight line passing through the end points of the DAC transfer curve. Because the part operates from a single supply and the output cannot go below zero, the linearity is measured between full scale and the code corresponding to the maximum offset specification. The INL error at a given input code is calculated as follows:

$$INL = [V_{OUT} - V_{OS} - (V_{FS} - V_{OS})(code/16383)]/LSB$$

V_{OUT} = The output voltage of the DAC measured at the given input code

Differential Nonlinearity (DNL): DNL is the difference between the measured change and the ideal one LSB change between any two adjacent codes. The DNL error between any two codes is calculated as follows:

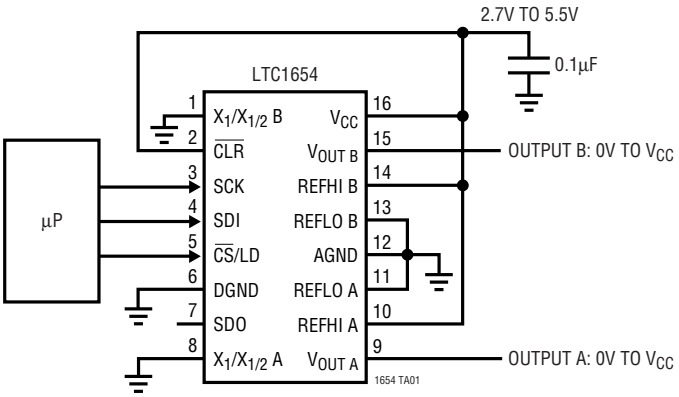
$$DNL = (\Delta V_{OUT} - LSB)/LSB$$

ΔV_{OUT} = The measured voltage difference between two adjacent codes

Digital Feedthrough: The glitch that appears at the analog output caused by AC coupling from the digital inputs when they change state. The area of the glitch is specified in nV • s.

TYPICAL APPLICATION

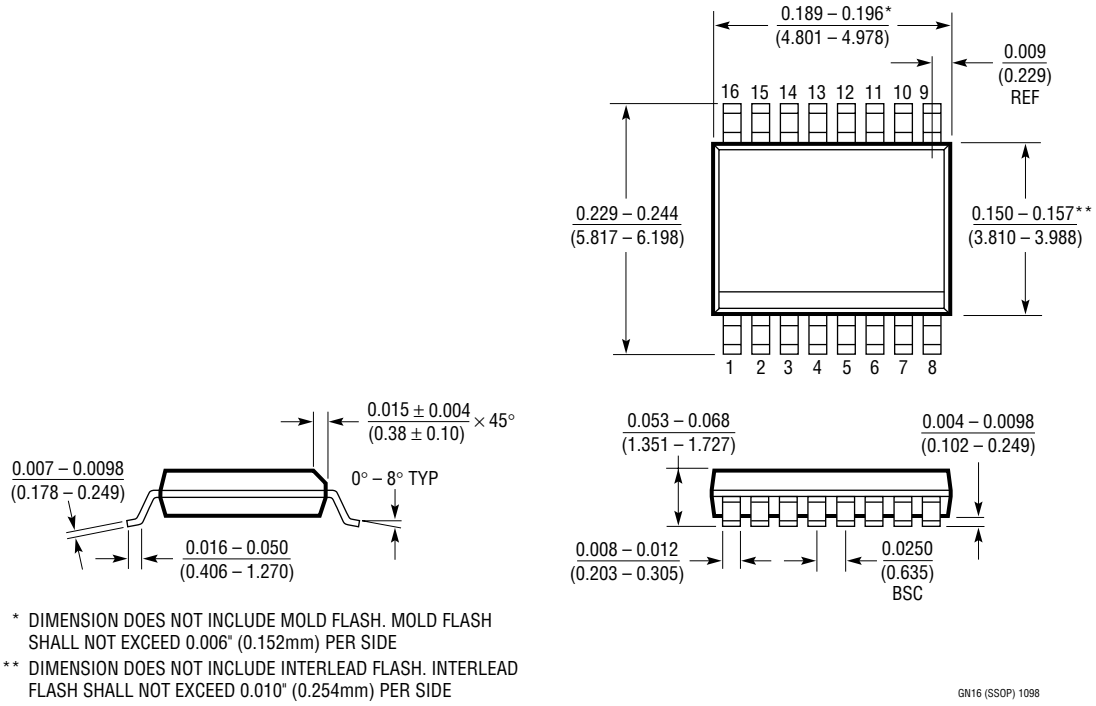
Dual 14-Bit Voltage Output DAC



PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

GN Package
16-Lead Plastic SSOP (Narrow 0.150)
(LTC DWG # 05-08-1641)



* DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

** DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

GN16 (SSOP) 1098

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1257	Single 12-Bit V_{OUT} DAC, Full Scale: 2.048V, V_{CC}: 4.75V to 15.75V, Reference Can Be Overdriven Up to 12V, i.e., FS_{MAX} = 12V	5V to 15V Single Supply, Complete V_{OUT} DAC in SO-8 Package
LTC1446/LTC1446L	Dual 12-Bit V_{OUT} DACs in SO-8 Package	LTC1446: V_{CC} = 4.5V to 5.5V, V_{OUT} = 0V to 4.095V LTC1446L: V_{CC} = 2.7V to 5.5V, V_{OUT} = 0V to 2.5V
LTC1448	Dual 12-Bit V_{OUT} DAC, V_{CC}: 2.7V to 5.5V	Output Swings from GND to REF. REF Input Can Be Tied to V_{CC}
LTC1450/LTC1450L	Single 12-Bit V_{OUT} DACs with Parallel Interface	LTC1450: V_{CC} = 4.5V to 5.5V, V_{OUT} = 0V to 4.095V LTC1450L: V_{CC} = 2.7V to 5.5V, V_{OUT} = 0V to 2.5V
LTC1451	Single Rail-to-Rail 12-Bit DAC, Full Scale: 4.095V, V_{CC}: 4.5V to 5.5V, Internal 2.048V Reference Brought Out to Pin	5V, Low Power Complete V_{OUT} DAC in SO-8 Package
LTC1452	Single Rail-to-Rail 12-Bit V_{OUT} Multiplying DAC, V_{CC}: 2.7V to 5.5V	Low Power, Multiplying V_{OUT} DAC with Rail-to-Rail Buffer Amplifier in SO-8 Package
LTC1453	Single Rail-to-Rail 12-Bit V_{OUT} DAC, Full Scale: 2.5V, V_{CC}: 2.7V to 5.5V	3V, Low Power, Complete V_{OUT} DAC in SO-8 Package
LTC1454/LTC1454L	Dual 12-Bit V_{OUT} DACs in SO-16 Package with Added Functionality	LTC1454: V_{CC} = 4.5V to 5.5V, V_{OUT} = 0V to 4.095V LTC1454L: V_{CC} = 2.7V to 5.5V, V_{OUT} = 0V to 2.5V
LTC1456	Single Rail-to-Rail Output 12-Bit DAC with Clear Pin, Full Scale: 4.095V, V_{CC}: 4.5V to 5.5V	Low Power, Complete V_{OUT} DAC in SO-8 Package with Clear Pin
LTC1458/LTC1458L	Quad 12 Bit Rail-to-Rail Output DACs with Added Functionality	LTC1458: V_{CC} = 4.5V to 5.5V, V_{OUT} = 0V to 4.095V LTC1458L: V_{CC} = 2.7V to 5.5V, V_{OUT} = 0V to 2.5V
LTC1658	14-Bit Rail-to-Rail Micropower DAC in MSOP, V_{CC}: 2.7V to 5.5V	Output Swings from GND to REF. REF Input Can Be Tied to V_{CC}
LTC1659	Single Rail-to-Rail 12-Bit V_{OUT} DAC in 8-Pin MSOP, V_{CC}: 2.7V to 5.5V	Low Power, Multiplying V_{OUT} DAC in MS8 Package. Output Swings from GND to REF. REF Input Can Be Tied to V_{CC}.
References		
LT1460	Micropower Precision Reference	Low Cost, 10ppm Drift
LT1461	Precision Voltage Reference	Ultralow Drift 3ppm/°C, Initial Accuracy: 0.04%
LT1634	Micropower Precision Reference	Low Drift 10ppm/°C, Initial Accuracy: 0.05%

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