Quad 16-Bit Rail-to-Rail DACs in 16-Lead SSOP

FEATURES

- **Smallest Pin Compatible Quad 16-Bit DAC:**
  LTC2604: 16-Bits
  LTC2614: 14-Bits
  LTC2624: 12-Bits
- **Guaranteed 16-Bit Monotonic Over Temperature**
- Separate Reference Inputs for each DAC
- Wide 2.5V to 5.5V Supply Range
- Low Power Operation: 250µA per DAC at 3V
- Individual DAC Power-Down to 1µA, Max
- Ultralow Crosstalk Between DACs (<5µV)
- High Rail-to-Rail Output Drive (±15mA)
- Double Buffered Digital Inputs
- 16-Lead Narrow SSOP Package

APPLICATIONS

- Mobile Communications
- Process Control and Industrial Automation
- Instrumentation
- Automatic Test Equipment

DESCRIPTION

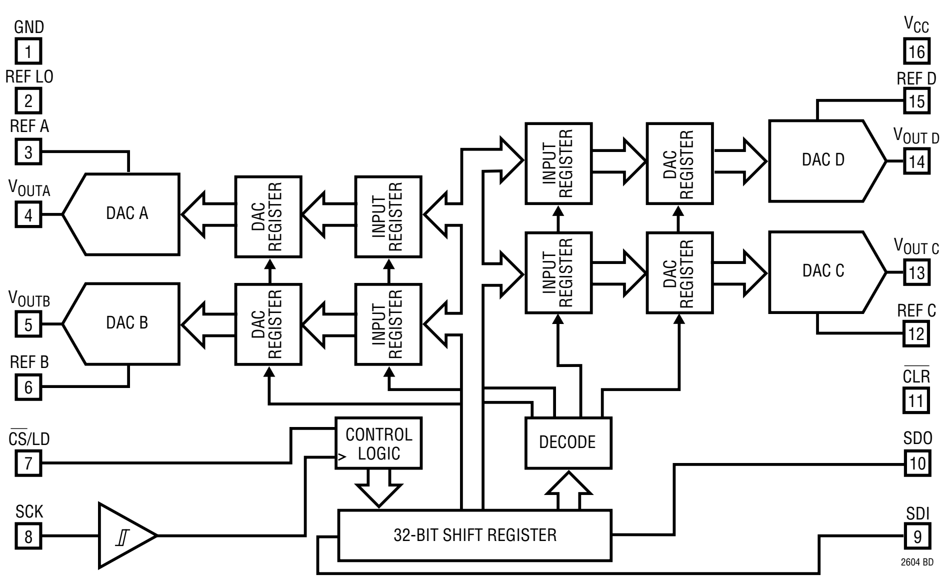
The LTC®2604/LTC2614/LTC2624 are quad 16-,14- and 12-bit 2.5V to 5.5V rail-to-rail voltage output DACs in 16-lead narrow SSOP packages. These parts have separate reference inputs for each DAC. They have built-in high performance output buffers and are guaranteed monotonic.

These parts establish advanced performance standards for output drive, crosstalk and load regulation in single-supply, voltage output multiples.

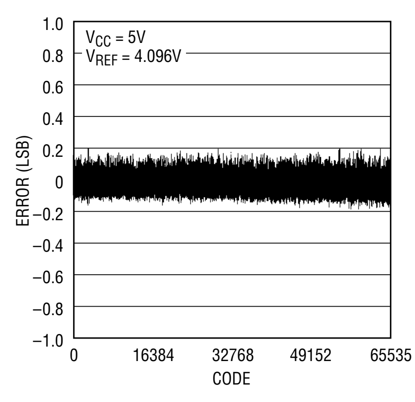
The parts use a simple SPI/MICROWIRE™ compatible 3-wire serial interface which can be operated at clock rates up to 50MHz. Daisy-chain capability and a hardware $\overline{\text{CLR}}$ function are included.

The LTC2604/LTC2614/LTC2624 incorporate a power-on reset circuit. During power-up, the voltage outputs rise less than 10mV above zero scale; and after power-up, they stay at zero scale until a valid write and update take place.

BLOCK DIAGRAM



Differential Nonlinearity (LTC2604)

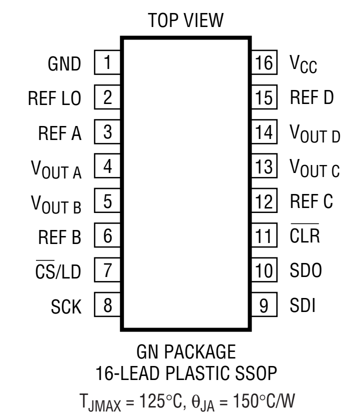


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Any Pin to GND .... −0.3V to 6V
Any Pin to V_{CC} .... −6V to 0.3V
Maximum Junction Temperature .... 125°C
Operating Temperature Range
  LTC2604/LTC2614/LTC2624C .... 0°C to 70°C
  LTC2604/LTC2614/LTC2624I .... −40°C to 85°C
Storage Temperature Range .... −65°C to 150°C
Lead Temperature (Soldering, 10 sec)................ 300°C

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER
LTC2604CGN
LTC2604IGN
LTC2614CGN
LTC2614IGN
LTC2624CGN
LTC2624IGN

GN PART MARKING	
2604	2614I
2604I	2624
2614	2624I

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. REF A = REF B = REF C = REF D = 4.096V (V_{CC} = 5V), REF A = REF B = REF C = REF D = 2.048V (V_{CC} = 2.5V), REF LO = 0V, V_{OUT} unloaded, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LTC2624 MIN	LTC2624 TYP	LTC2624 MAX	LTC2614 MIN	LTC2614 TYP	LTC2614 MAX	LTC2604 MIN	LTC2604 TYP	LTC2604 MAX	UNITS
DC Performance													
	Resolution		●	12			14			16			Bits
	Monotonicity	(Note 2)	●	12			14			16			Bits
DNL	Differential Nonlinearity	(Note 2)	●			±0.5			±1			±1	LSB
INL	Integral Nonlinearity	(Note 2)	●		±0.9	±4		±4	±16		±14	±64	LSB
	Load Regulation	$V_{REF} = V_{CC}$ = 5V, Midscale											
		I_{OUT} = 0mA to 15mA Sourcing	●		0.025	0.125		0.1	0.5		0.3	2	LSB/mA
		I_{OUT} = 0mA to 15mA Sinking	●		0.025	0.125		0.1	0.5		0.3	2	LSB/mA
		$V_{REF} = V_{CC}$ = 2.5V, Midscale											
		I_{OUT} = 0mA to 7.5mA Sourcing	●		0.05	0.25		0.2	1		0.7	4	LSB/mA
		I_{OUT} = 0mA to 7.5mA Sinking	●		0.05	0.25		0.2	1		0.7	4	LSB/mA
ZSE	Zero-Scale Error		●		1.5	9		1.5	9		1.5	9	mV
V_{OS}	Offset Error	(Note 7)	●		±1.5	±9		±1.5	±9		±1.5	±9	mV
	V_{OS} Temperature Coefficient				±5			±5			±5		µV/°C
GE	Gain Error		●		±0.1	±0.7		±0.1	±0.7		±0.1	±0.7	%FSR
	Gain Temperature Coefficient				±5			±5			±5		ppm/°C

SYMBOL	PARAMETER	CONDITIONS		LTC2604/LTC2614/LTC2624 MIN	TYP	MAX	UNITS
PSR	Power Supply Rejection	V_{CC} = 5V ±10%			−80		dB
		V_{CC} = 3V ±10%			−80		dB
R_{OUT}	DC Output Impedance	$V_{REF} = V_{CC}$ = 5V, Midscale; −15mA ≤ I_{OUT} ≤ 15mA	●		0.025	0.15	Ω
		$V_{REF} = V_{CC}$ = 2.5V, Midscale; −7.5mA ≤ I_{OUT} ≤ 7.5mA	●		0.030	0.15	Ω

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. REF A = REF B = REF C = REF D = 4.096V (V_{CC} = 5V), REF A = REF B = REF C = REF D = 2.048V (V_{CC} = 2.5V), REF LO = 0V, V_{OUT} unloaded, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LTC2604/LTC2614/LTC2624 MIN	TYP	MAX	UNITS
	DC Crosstalk (Note 4)	Due to Full Scale Output Change (Note 5) Due to Load Current Change Due to Powering Down (per Channel)			±5 ±1 ±3.5		µV µV/mA µV
I_{SC}	Short-Circuit Output Current	V_{CC} = 5.5V, V_{REF} = 5.5V Code: Zero Scale; Forcing Output to V_{CC} Code: Full Scale; Forcing Output to GND	 ● ●	 15 15	 34 36	 60 60	 mA mA
		V_{CC} = 2.5V, V_{REF} = 2.5V Code: Zero Scale; Forcing Output to V_{CC} Code: Full Scale; Forcing Output to GND	 ● ●	 7.5 7.5	 18 24	 50 50	 mA mA
Reference Input							
	Input Voltage Range		●	0		V_{CC}	V
	Resistance	Normal Mode	●	88	128	160	kΩ
	Capacitance				14		pF
I_{REF}	Reference Current, Power Down Mode	All DACs Powered Down	●		0.001	1	µA
Power Supply							
V_{CC}	Positive Supply Voltage	For Specified Performance	●	2.5		5.5	V
I_{CC}	Supply Current	V_{CC} = 5V (Note 3) V_{CC} = 3V (Note 3) All DACs Powered Down (Note 3) V_{CC} = 5V All DACs Powered Down (Note 3) V_{CC} = 3V	● ● ● ●		1.3 1 0.35 0.10	2 1.6 1 1	mA mA µA µA
Digital I/O							
V_{IH}	Digital Input High Voltage	V_{CC} = 2.5V to 5.5V V_{CC} = 2.5V to 3.6V	● ●	2.4 2.0			V V
V_{IL}	Digital Input Low Voltage	V_{CC} = 4.5V to 5.5V V_{CC} = 2.5V to 5.5V	● ●			0.8 0.6	V V
V_{OH}	Digital Output High Voltage	Load Current = –100µA	●	V_{CC} – 0.4			V
V_{OL}	Digital Output Low Voltage	Load Current = +100µA	●			0.4	V
I_{LK}	Digital Input Leakage	V_{IN} = GND to V_{CC}	●			±1	µA
C_{IN}	Digital Input Capacitance	(Note 6)	●			8	pF

SYMBOL	PARAMETER	CONDITIONS		LTC2624 MIN	TYP	MAX	LTC2614 MIN	TYP	MAX	LTC2604 MIN	TYP	MAX	UNITS
AC Performance													
t_S	Settling Time (Note 8)	±0.024% (±1LSB at 12 Bits) ±0.006% (±1LSB at 14 Bits) ±0.0015% (±1LSB at 16 Bits)			7			7 9			7 9 10		µs µs µs
	Settling Time for 1LSB Step (Note 9)	±0.024% (±1LSB at 12 Bits) ±0.006% (±1LSB at 14 Bits) ±0.0015% (±1LSB at 16 Bits)			2.7			2.7 4.8			2.7 4.8 5.2		µs µs µs
	Voltage Output Slew Rate				0.80			0.80			0.80		V/µs
	Capacitive Load Driving				1000			1000			1000		pF
	Glitch Impulse	At Midscale Transition			12			12			12		nV • s
	Multiplying Bandwidth				180			180			180		kHz
e_n	Output Voltage Noise Density	At f = 1kHz At f = 10kHz			120 100			120 100			120 100		$nV/\sqrt{Hz}$ $nV/\sqrt{Hz}$
	Output Voltage Noise	0.1Hz to 10Hz			15			15			15		μV_{P-P}

TIMING CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. REF A = REF B = REF C = REF D = 4.096V (V_{CC} = 5V), REF A = REF B = REF C = REF D = 2.048V (V_{CC} = 2.5V), REF LO = 0V, V_{OUT} unloaded, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LTC2604/LTC2614/LTC2624 MIN	TYP	MAX	UNITS
V_{CC} = 2.5V to 5.5V							
t_1	SDI Valid to SCK Setup		●	4			ns
t_2	SDI Valid to SCK Hold		●	4			ns
t_3	SCK High Time		●	9			ns
t_4	SCK Low Time		●	9			ns
t_5	$\overline{CS}$/LD Pulse Width		●	10			ns
t_6	LSB SCK High to $\overline{CS}$/LD High		●	7			ns
t_7	$\overline{CS}$/LD Low to SCK High		●	7			ns
t_8	SDO Propagation Delay from SCK Falling Edge	C_{LOAD} = 10pF V_{CC} = 4.5V to 5.5V V_{CC} = 2.5V to 5.5V	 ● ●			 20 45	 ns ns
t_9	$\overline{CLR}$ Pulse Width		●	20			ns
t_{10}	$\overline{CS}$/LD High to SCK Positive Edge		●	7			ns
	SCK Frequency	50% Duty Cycle	●			50	MHz

Note 1: Absolute maximum ratings are those values beyond which the life of a device may be impaired.

Note 2: Linearity and monotonicity are defined from code k_L to code $2^N – 1$, where N is the resolution and k_L is given by $k_L = 0.016(2^N/V_{REF})$, rounded to the nearest whole code. For V_{REF} = 4.096V and N = 16, k_L = 256, linearity is defined from code 256 to code 65,535.

Note 3: Digital inputs at 0V or V_{CC}.

Note 4: DC crosstalk is measured with V_{CC} = 5V and V_{REF} = 4.096V, with the measured DAC at midscale, unless otherwise noted.

Note 5: R_L = 2kΩ to GND or V_{CC}.

Note 6: Guaranteed by design and not production tested.

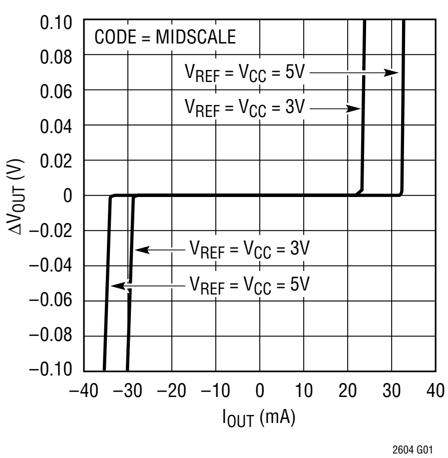
Note 7: Inferred from measurement at code 256 (LTC2604), code 64 (LTC2614) or code 16 (LTC2624), and at full scale.

Note 8: V_{CC} = 5V, V_{REF} = 4.096V. DAC is stepped 1/4 scale to 3/4 scale and 3/4 scate to 1/4 scale. Load is 2k in parallel with 200pF to GND.

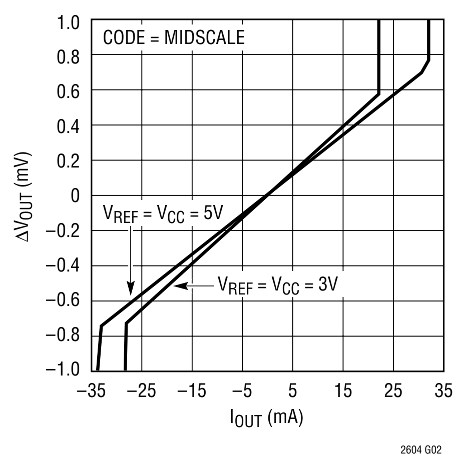
Note 9: V_{CC} = 5V, V_{REF} = 4.096V. DAC is stepped 1LSB between half scale and half scale –1. Load is 2k in parallel with 200pF to GND.

TYPICAL PERFORMANCE CHARACTERISTICS (LTC2604/LTC2614/LTC2624)

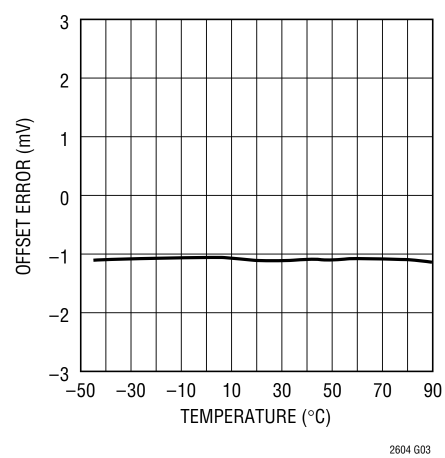
Current Limiting



Load Regulation

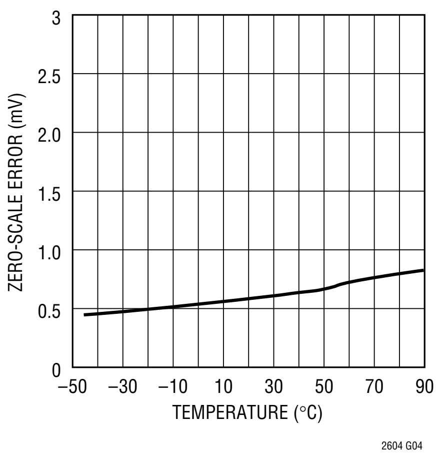


Offset Error vs Temperature

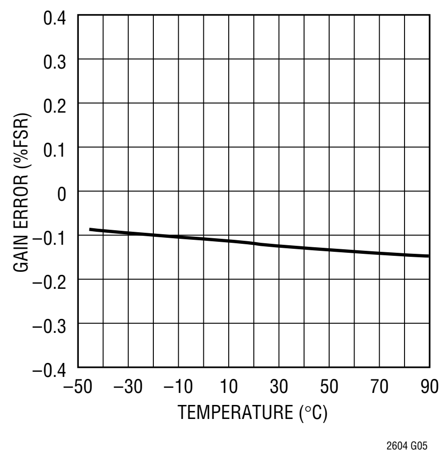


TYPICAL PERFORMANCE CHARACTERISTICS (LTC2604/LTC2614/LTC2624)

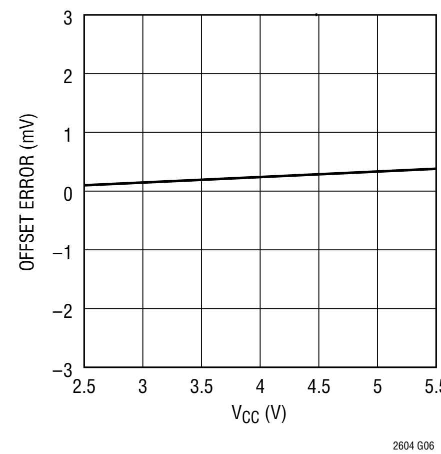
Zero-Scale Error vs Temperature



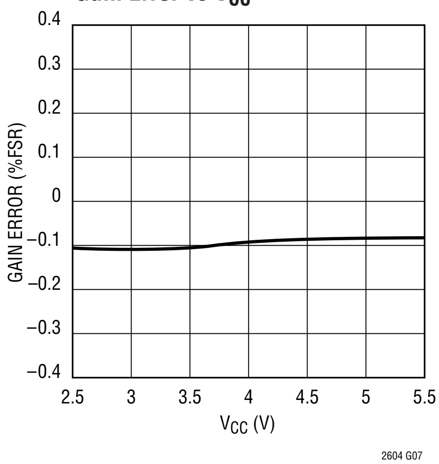
Gain Error vs Temperature



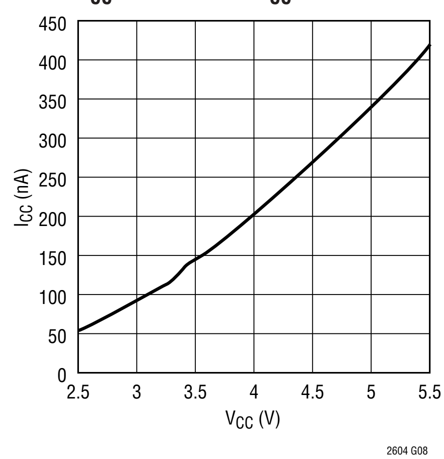
Offset Error vs V_{CC}



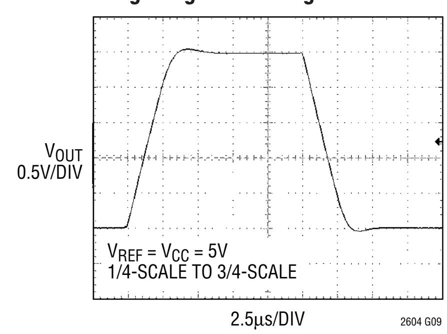
Gain Error vs V_{CC}



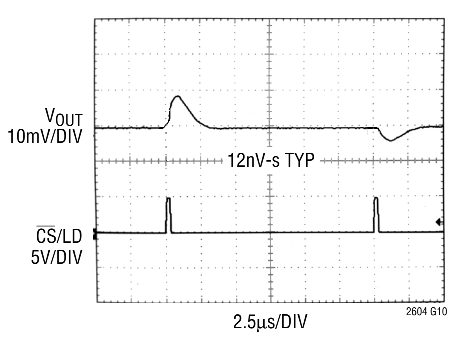
I_{CC} Shutdown vs V_{CC}



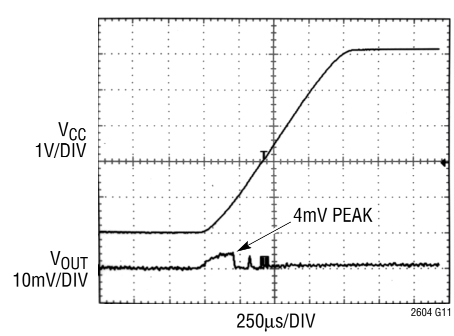
Large-Signal Settling



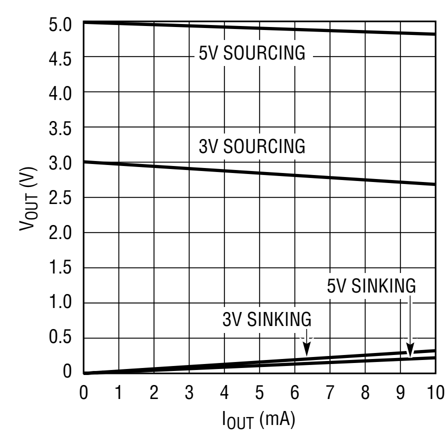
Midscale Glitch Impulse



Power-On Reset Glitch

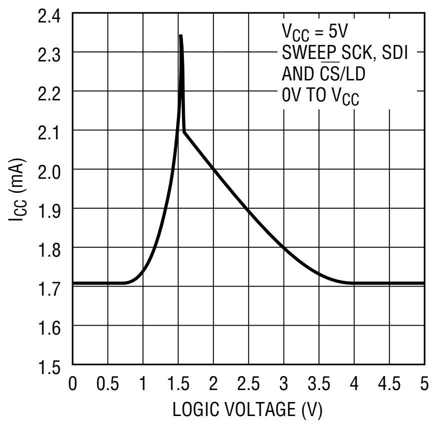


Headroom at Rails vs Output Current



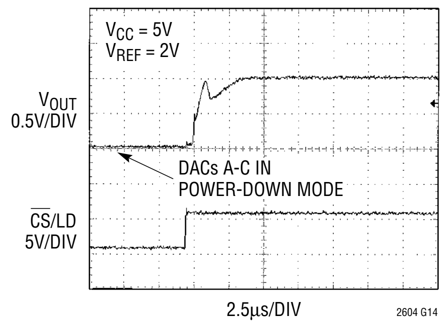
TYPICAL PERFORMANCE CHARACTERISTICS (LTC2604/LTC2614/LTC2624)

Supply Current vs Logic Voltage



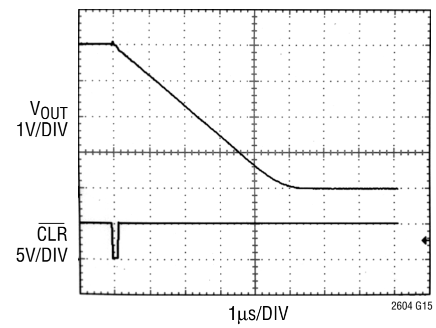
2604 G13

Exiting Power-Down to Midscale



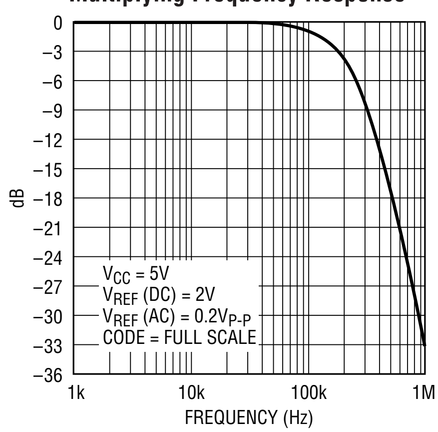
2604 G14

Hardware CLR



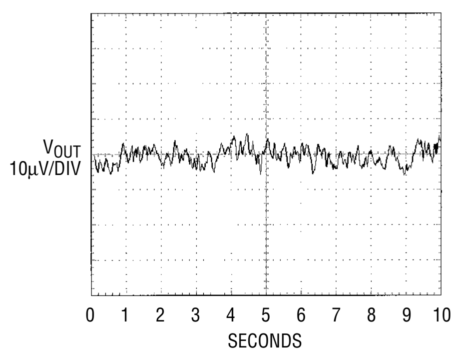
2604 G15

Multiplying Frequency Response



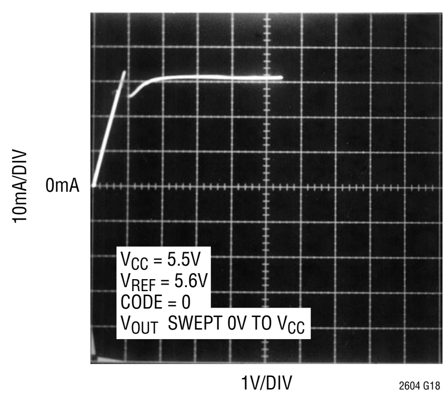
2604 G16

Output Voltage Noise, 0.1Hz to 10Hz



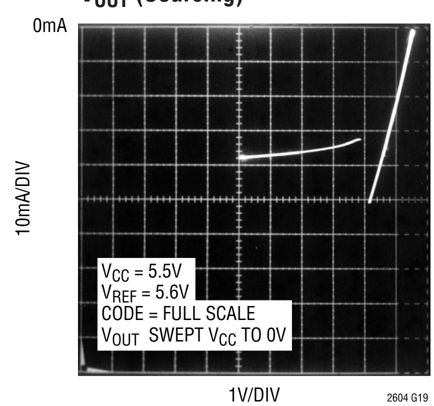
2604 G17

Short-Circuit Output Current vs V_{OUT} (Sinking)



2604 G18

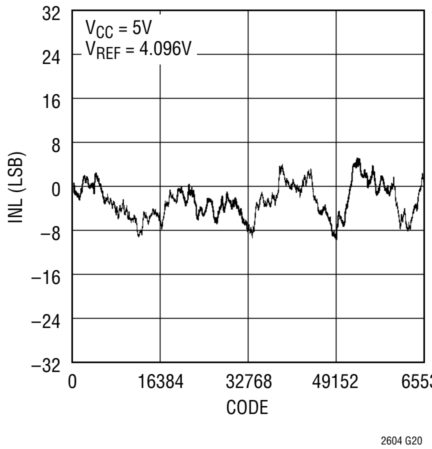
Short-Circuit Output Current vs V_{OUT} (Sourcing)



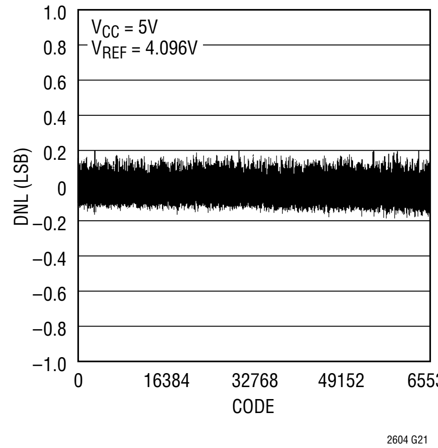
2604 G19

TYPICAL PERFORMANCE CHARACTERISTICS (LTC2604)

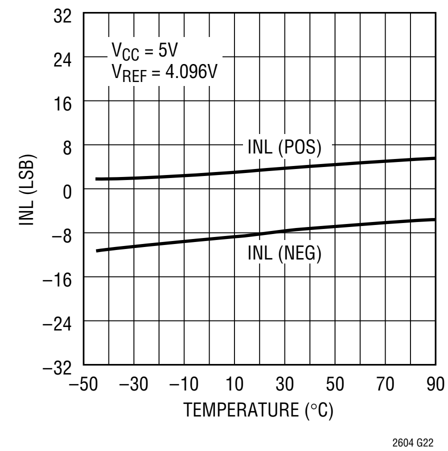
Integral Nonlinearity (INL)



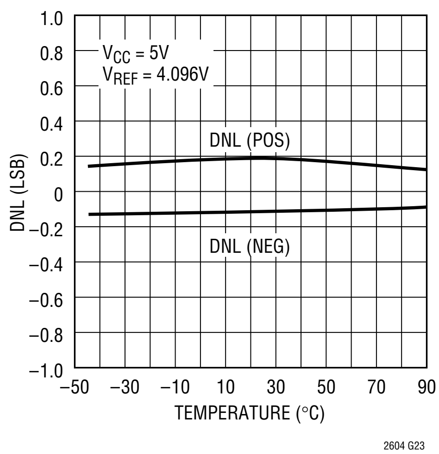
Differential Nonlinearity (DNL)



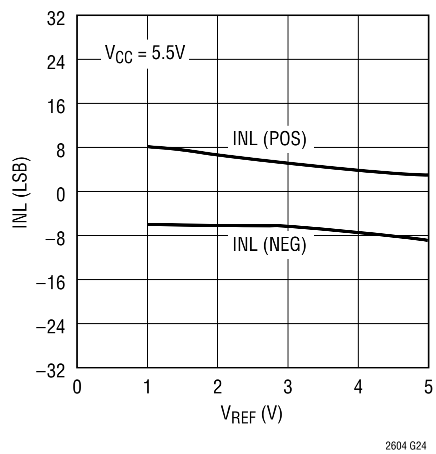
INL vs Temperature



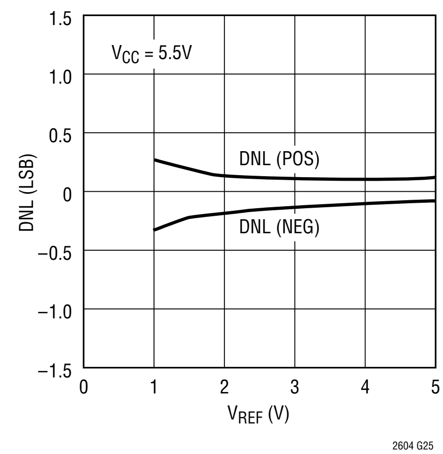
DNL vs Temperature



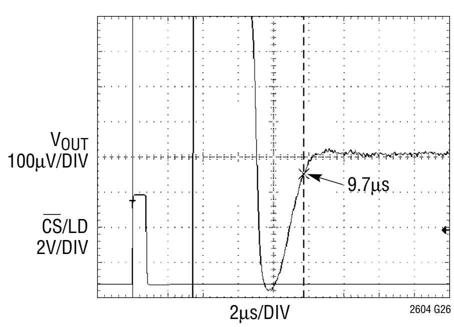
INL vs V_{REF}



DNL vs V_{REF}

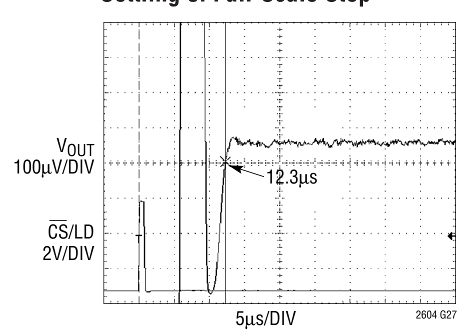


Settling to ±1LSB



V_{CC} = 5V, V_{REF} = 4.096V
1/4-SCALE TO 3/4-SCALE STEP
R_L = 2k, C_L = 200pF
AVERAGE OF 2048 EVENTS

Settling of Full-Scale Step

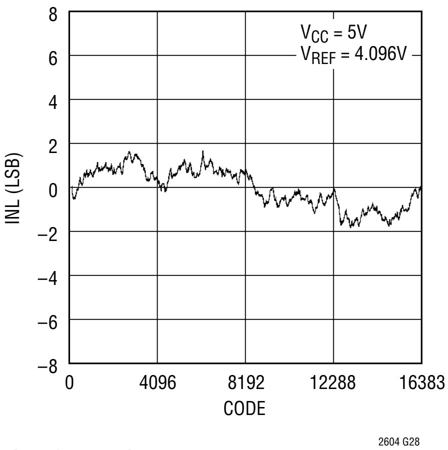


V_{CC} = 5V, V_{REF} = 4.096V
CODE 512 TO 65535 STEP
AVERAGE OF 2048 EVENTS
SETTLING TO ±1LSB

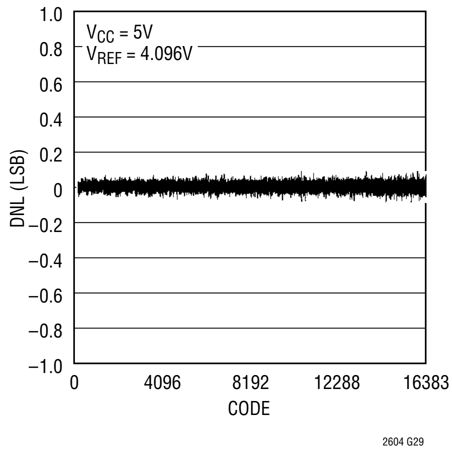
TYPICAL PERFORMANCE CHARACTERISTICS

(LTC2614)

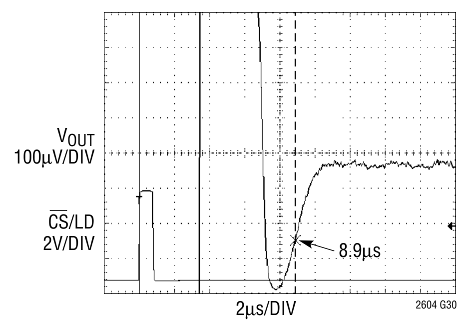
Integral Nonlinearity (INL)



Differential Nonlinearity (DNL)



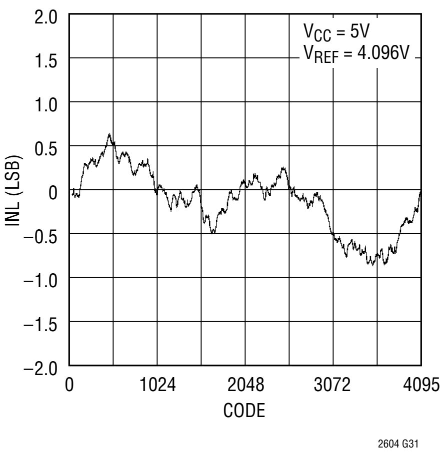
Settling to ±1LSB



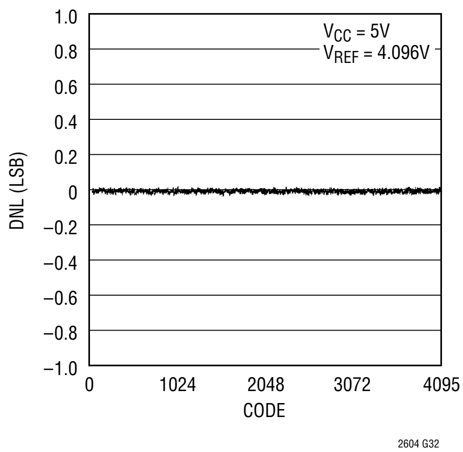
V_{CC} = 5V, V_{REF} = 4.096V
1/4-SCALE TO 3/4-SCALE STEP
R_L = 2k, C_L = 200pF
AVERAGE OF 2048 EVENTS

(LTC2624)

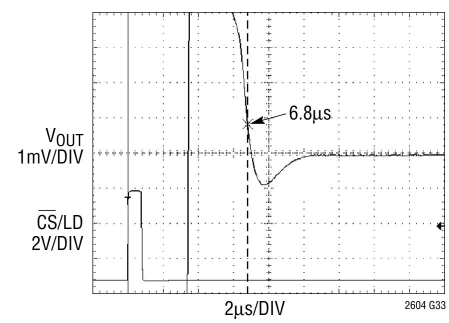
Integral Nonlinearity (INL)



Differential Nonlinearity (DNL)



Settling to ±1LSB



V_{CC} = 5V, V_{REF} = 4.096V
1/4-SCALE TO 3/4-SCALE STEP
R_L = 2k, C_L = 200pF
AVERAGE OF 2048 EVENTS

PIN FUNCTIONS

GND (Pin 1): Analog Ground.

REF LO (Pin 2): Reference Low. The voltage at this pin sets the zero scale (ZS) voltage of all DACs. The voltage range is $0 \le \text{REF LO} \le V_{CC} - 2.5V$.

REF A, REF B, REF C, REF D (Pins 3, 6, 12, 15): Reference Voltage Inputs for each DAC. REF x sets the full scale voltage of the DACs. $0V \le \text{REF x} \le V_{CC}$.

$V_{OUT\ A}$ to $V_{OUT\ D}$ (Pins 4, 5, 13, 14): DAC Analog Voltage Outputs. The output range is from REF LO to REF x.

$\overline{CS}$/LD (Pin 7): Serial Interface Chip Select/Load Input. When $\overline{CS}$/LD is low, SCK is enabled for shifting data on SDI into the register. When $\overline{CS}$/LD is taken high, SCK is disabled and the specified command (see Table 1) is executed.

SCK (Pin 8): Serial Interface Clock Input. CMOS and TTL compatible.

SDI (Pin 9): Serial Interface Data Input. Data is applied to SDI for transfer to the device at the rising edge of SCK. The LTC2604/LTC2614/LTC2624 accepts input word lengths of either 24 or 32 bits.

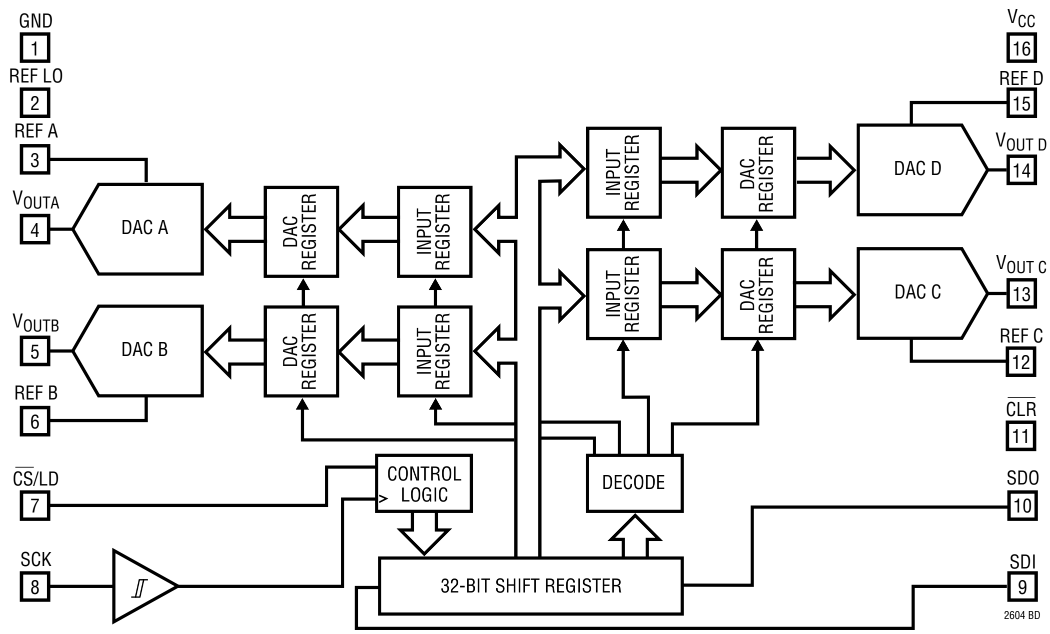
PIN FUNCTIONS

SDO (Pin 10): Serial Interface Data Output. The serial output of the shift register appears at the SDO pin. The data transferred to the device via the SDI pin is delayed 32 SCK rising edges before being output at the next falling edge. This pin is used for daisy-chain operation.

$\overline{\text{CLR}}$ (Pin 11): Asynchronous Clear Input. A logic low at this level-triggered input clears all registers and causes the DAC voltage outputs to drop to 0V. CMOS and TTL-compatible.

V_{CC} (Pin 16): Supply Voltage Input. $2.5V \le V_{CC} \le 5.5V$.

BLOCK DIAGRAM



TIMING DIAGRAM

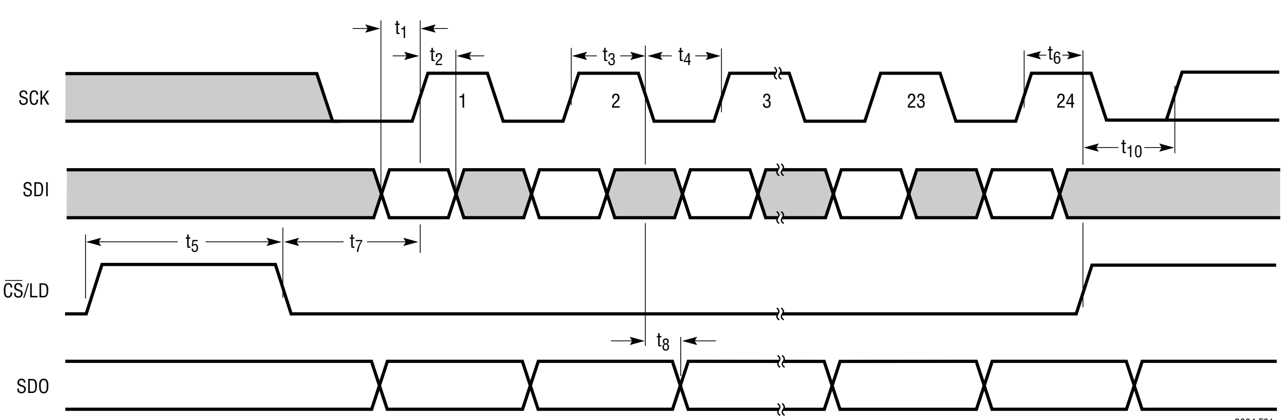


Figure 1

OPERATION

Power-On Reset

The LTC2604/LTC2614/LTC2624 clear the outputs to zero scale when power is first applied, making system initialization consistent and repeatable.

For some applications, downstream circuits are active during DAC power-up, and may be sensitive to nonzero outputs from the DAC during this time. The LTC2604/LTC2614/LTC2624 contain circuitry to reduce the power-on glitch; furthermore, the glitch amplitude can be made arbitrarily small by reducing the ramp rate of the power supply. For example, if the power supply is ramped to 5V in 1ms, the analog outputs rise less than 10mV above ground (typ) during power-on. See Power-On Reset Glitch in the Typical Performance Characteristics section.

Power Supply Sequencing

The voltage at REF (Pins 3, 6, 12 and 15) should be kept within the range $-0.3V \le REF\,x \le V_{CC} + 0.3V$ (see Absolute Maximum Ratings). Particular care should be taken to observe these limits during power supply turn-on and turn-off sequences, when the voltage at V_{CC} (Pin 16) is in transition.

Transfer Function

The digital-to-analog transfer function is

$$V_{OUT(IDEAL)} = \left(\frac{k}{2^N}\right)[REF\,x - REFLO] + REFLO$$

where k is the decimal equivalent of the binary DAC input code, N is the resolution and REF x is the voltage at REF A, REF B, REF C and REF D (Pins 3, 6, 12 and 15).

Serial Interface

The $\overline{CS}$/LD input is level triggered. When this input is taken low, it acts as a chip-select signal, powering-on the SDI and SCK buffers and enabling the input shift register. Data (SDI input) is transferred at the next 24 rising SCK edges. The 4-bit command, C3-C0, is loaded first; then the 4-bit DAC address, A3-A0; and finally the 16-bit data word. The data word comprises the 16-, 14- or 12-bit input code, ordered MSB-to-LSB, followed by 0, 2 or 4 don't-care bits (LTC2604, LTC2614 and LTC2624 respectively). Data can only be transferred to the device when the $\overline{CS}$/LD signal is low.The rising edge of $\overline{CS}$/LD ends the data transfer and causes the device to carry out the action specified in the 24-bit input word. The complete sequence is shown in Figure 2a.

Table 1.

COMMAND*				
C3	**C2**	**C1**	**C0**	
0	0	0	0	Write to Input Register n
0	0	0	1	Update (Power Up) DAC Register n
0	0	1	0	Write to Input Register n, Update (Power Up) All n
0	0	1	1	Write to and Update (Power Up) n
0	1	0	0	Power Down n
1	1	1	1	No Operation
ADDRESS (n)*				
A3	**A2**	**A1**	**A0**	
0	0	0	0	DAC A
0	0	0	1	DAC B
0	0	1	0	DAC C
0	0	1	1	DAC D
1	1	1	1	All DACs

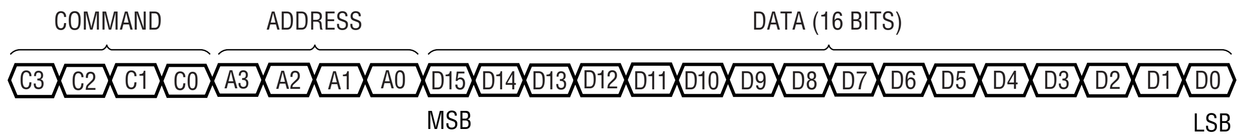
*Command and address codes not shown are reserved and should not be used.

The command (C3-C0) and address (A3-A0) assignments are shown in Table 1. The first four commands in the table consist of write and update operations. A write operation loads a 16-bit data word from the 32-bit shift register into the input register of the selected DAC, n. An update operation copies the data word from the input register to the DAC register. Once copied into the DAC register, the data word becomes the active 16-, 14- or 12-bit input code, and is converted to an analog voltage at the DAC output. The update operation also powers up the selected DAC if it had been in power-down mode. The data path and registers are shown in the block diagram.

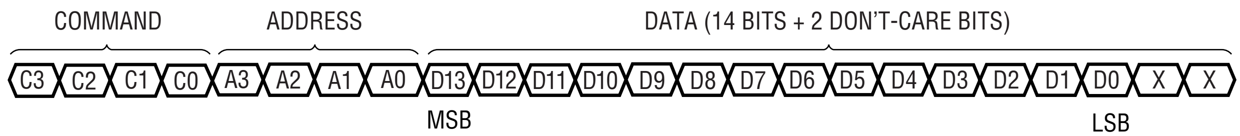
While the minimum input word is 24 bits, it may optionally be extended to 32 bits. To use the 32-bit word width, 8 don't-care bits are transferred to the device first, followed by the 24-bit word as just described. Figure 2b shows the 32-bit sequence. The 32-bit word is required for daisy-chain operation, and is also available to accommodate microprocessors which have a minimum word width of 16 bits (2 bytes).

OPERATION

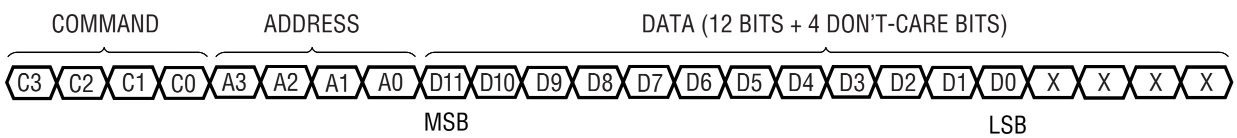
INPUT WORD (LTC2604)



INPUT WORD (LTC2614)



INPUT WORD (LTC2624)



Daisy-Chain Operation

The serial output of the shift register appears at the SDO pin. Data transferred to the device from the SDI input is delayed 32 SCK rising edges before being output at the next SCK falling edge.

The SDO output can be used to facilitate control of multiple serial devices from a single 3-wire serial port (i.e., SCK, SDI and $\overline{CS}$/LD). Such a "daisy chain" series is configured by connecting SDO of each upstream device to SDI of the next device in the chain. The shift registers of the devices are thus connected in series, effectively forming a single input shift register which extends through the entire chain. Because of this, the devices can be addressed and controlled individually by simply concatenating their input words; the first instruction addresses the last device in the chain and so forth. The SCK and $\overline{CS}$/LD signals are common to all devices in the series.

In use, $\overline{CS}$/LD is first taken low. Then the concatenated input data is transferred to the chain, using SDI of the first device as the data input. When the data transfer is complete, $\overline{CS}$/LD is taken high, completing the instruction sequence for all devices simultaneously. A single device can be controlled by using the no-operation command (1111) for the other devices in the chain.

Power-Down Mode

For power-constrained applications, power-down mode can be used to reduce the supply current whenever less than four outputs are needed. When in power-down, the buffer amplifiers, bias circuits and reference inputs are disabled, and draw essentially zero current. The DAC outputs are put into a high-impedance state, and the output pins are passively pulled to ground through individual 90k resistors. Input- and DAC-register contents are not disturbed during power-down.

Any channel or combination of channels can be put into power-down mode by using command 0100_b in combination with the appropriate DAC address, (n). The 16-bit data word is ignored. The supply current is reduced by approximately 1/4 for each DAC powered down. The effective resistance at REF x (pins 3, 6, 12 and 15) are at high-impedance input (typically > 1GΩ) when the corresponding DACs are powered down.

Normal operation can be resumed by executing any command which includes a DAC update, as shown in Table 1. The selected DAC is powered up as its voltage output is updated. When a DAC which is in a powered-down state is powered up and updated, normal settling is delayed. If less than four DACs are in a powered-down state prior to the update command, the power-up delay time is 5µs. If on the

OPERATION

other hand, all four DACs are powered down, then the main bias generation circuit block has been automatically shut down in addition to the individual DAC amplifiers and reference inputs. In this case, the power up delay time is 12µs (for V_{CC} = 5V) or 30µs (for V_{CC} = 3V).

Voltage Outputs

Each of the four rail-to-rail amplifiers contained in these parts has guaranteed load regulation when sourcing or sinking up to 15mA at 5V (7.5mA at 3V).

Load regulation is a measure of the amplifier's ability to maintain the rated voltage accuracy over a wide range of load conditions. The measured change in output voltage per milliampere of forced load current change is expressed in LSB/mA.

DC output impedance is equivalent to load regulation, and may be derived from it by simply calculating a change in units from LSB/mA to Ohms. The amplifiers' DC output impedance is 0.025Ω when driving a load well away from the rails.

When drawing a load current from either rail, the output voltage headroom with respect to that rail is limited by the 30Ω typical channel resistance of the output devices; e.g., when sinking 1mA, the minimum output voltage = 30Ω • 1mA = 25mV. See the graph Headroom at Rails vs Output Current in the Typical Performance Characteristics section.

The amplifiers are stable driving capacitive loads of up to 1000pF.

Board Layout

The excellent load regulation and DC crosstalk performance of these devices is achieved in part by keeping "signal" and "power" grounds separate.

The PC board should have separate areas for the analog and digital sections of the circuit. This keeps digital signals away from sensitive analog signals and facilitates the use of separate digital and analog ground planes which have minimal capacitive and resistive interaction with each other.

Digital and analog ground planes should be joined at only one point, establishing a system star ground as close to the device's ground pin as possible. Ideally, the analog ground plane should be located on the component side of the board, and should be allowed to run under the part to shield it from noise. Analog ground should be a continuous and uninterrupted plane, except for necessary lead pads and vias, with signal traces on another layer.

The GND pin functions as a return path for power supply currents in the device and should be connected to analog ground. Resistance from the GND pin to system star ground should be as low as possible. When a zero scale DAC output voltage of zero is desired, the REFLO pin (pin 2) should be connected to system star ground.

Rail-to-Rail Output Considerations

In any rail-to-rail voltage output device, the output is limited to voltages within the supply range.

Since the analog outputs of the device cannot go below ground, they may limit for the lowest codes as shown in Figure 3b. Similarly, limiting can occur near full scale when the REF pins are tied to V_{CC}. If REF x = V_{CC} and the DAC full-scale error (FSE) is positive, the output for the highest codes limits at V_{CC} as shown in Figure 3c. No full-scale limiting can occur if REF x is less than V_{CC} – FSE.

Offset and linearity are defined and tested over the region of the DAC transfer function where no output limiting can occur.

OPERATION

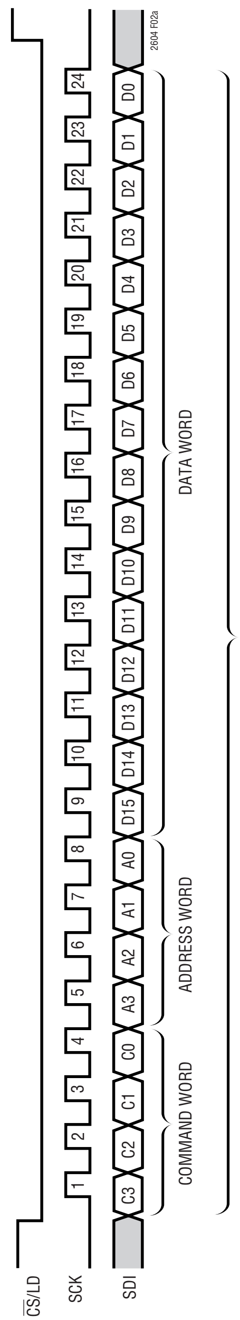


Figure 2a. LTC2604 24-Bit Load Sequence (Minimum Input Word)
LTC2614 SDI Data Word: 14-Bit Input Code + 2 Don't Care Bits
LTC2624 SDI Data Word: 12-Bit Input Code + 4 Don't Care Bits

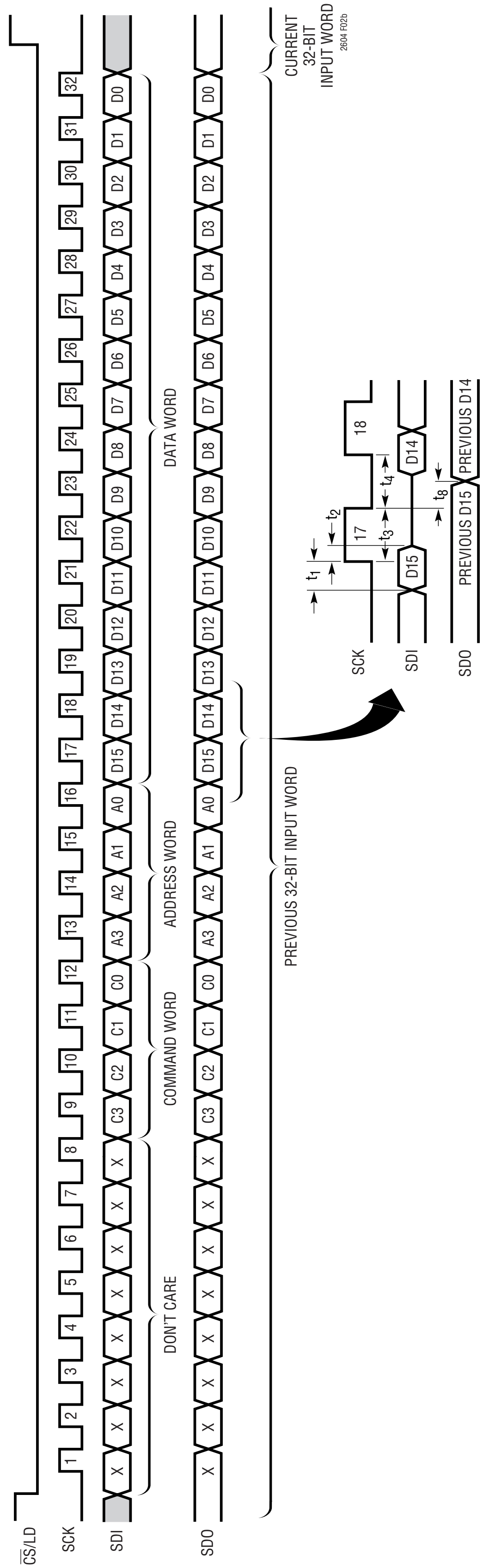


Figure 2b. LTC2604 32-Bit Load Sequence
LTC2614 SDI/SDO Data Word: 14-Bit Input Code + 2 Don't Care Bits
LTC2624 SDI/SDO Data Word: 12-Bit Input Code + 4 Don't Care Bits

OPERATION

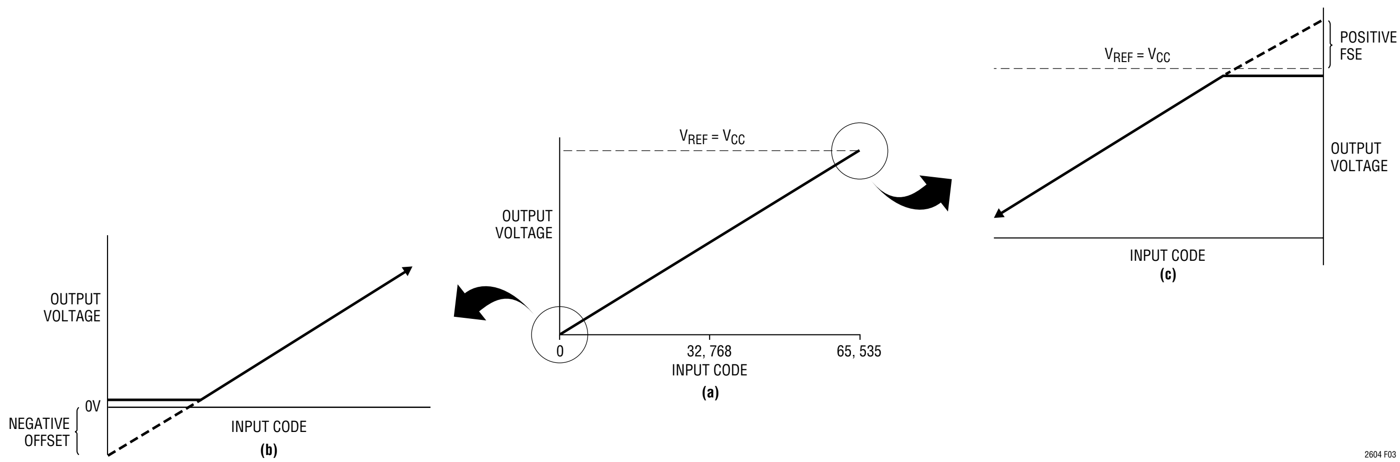
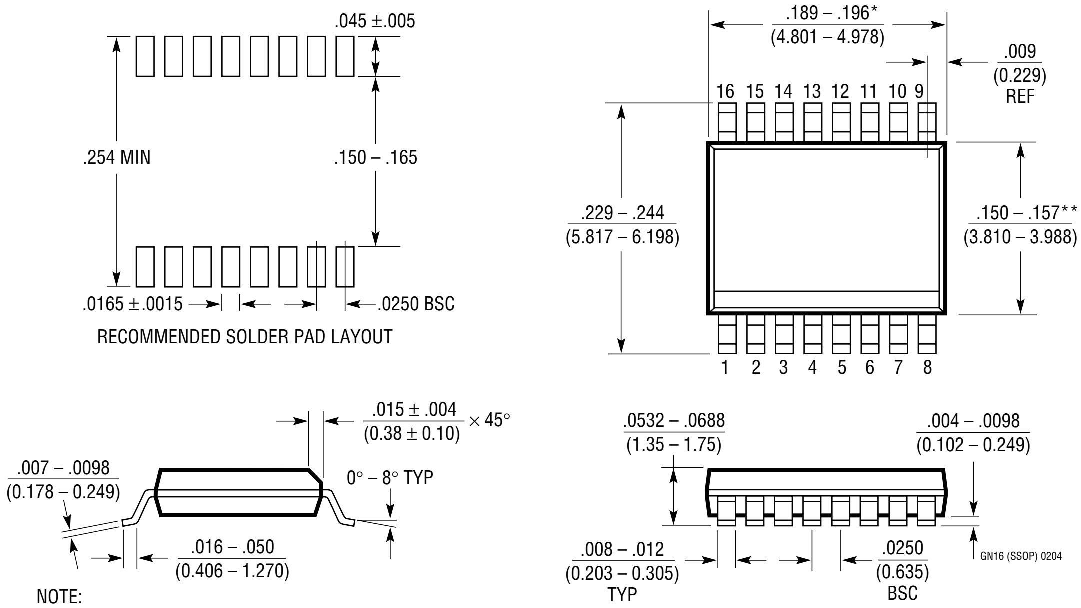


Figure 3. Effects of Rail-to-Rail Operation On a DAC Transfer Curve. (a) Overall Transfer Function (b) Effect of Negative Offset for Codes Near Zero Scale (c) Effect of Positive Full-Scale Error for Codes Near Full Scale

PACKAGE DESCRIPTION

GN Package
16-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641)



NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN $\frac{\text{INCHES}}{\text{(MILLIMETERS)}}$
3. DRAWING NOT TO SCALE

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

TYPICAL APPLICATION

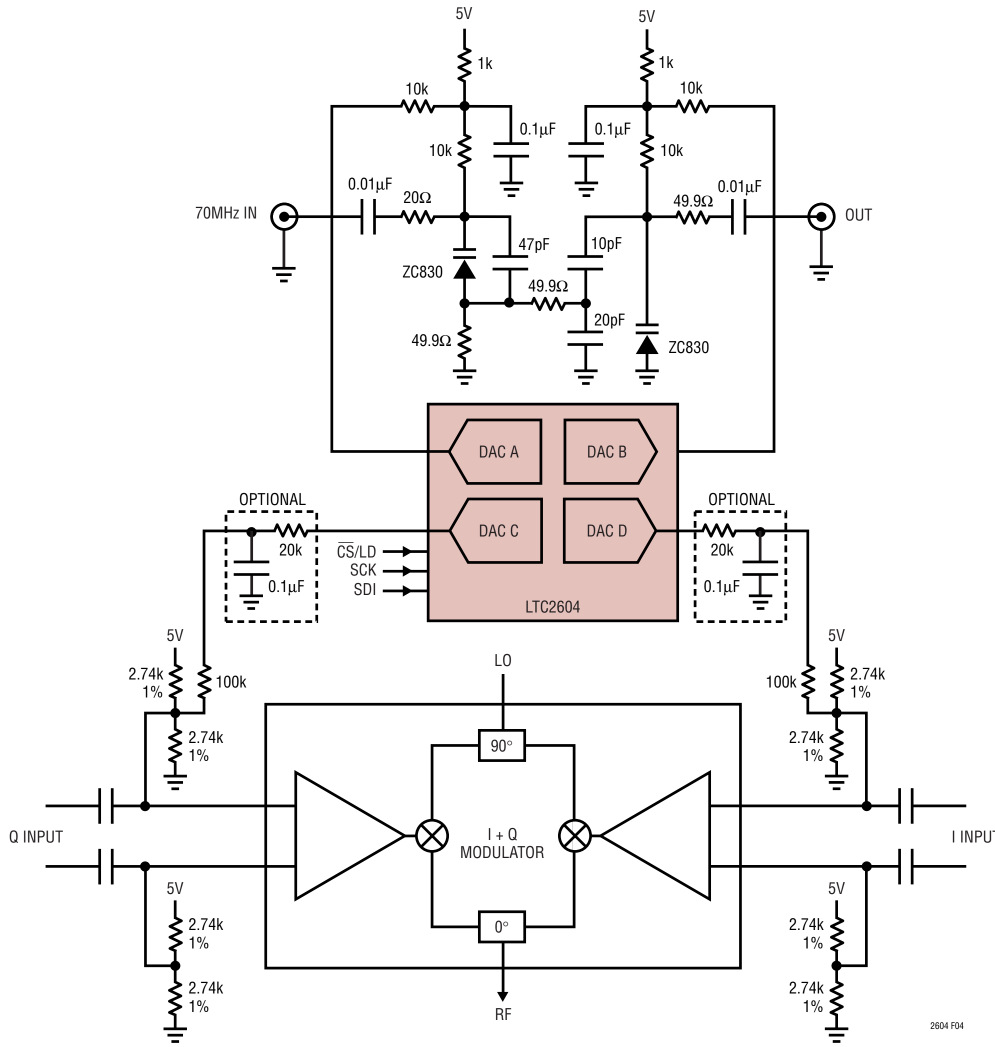


Figure 4. Using DAC A and DAC B for Nearly Continuous Attenuation Control and DAC C and DAC D to Trim for Minimum LO Feedthrough in a Mixer.

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1458/LTC1458L	Quad 12-Bit Rail-to-Rail Output DACs with Added Functionality	LTC1458: V_{CC} = 4.5V to 5.5V, V_{OUT} = 0V to 4.096V LTC1458L: V_{CC} = 2.7V to 5.5V, V_{OUT} = 0V to 2.5V
LTC1654	Dual 14-Bit Rail-to-Rail V_{OUT} DAC	Programmable Speed/Power, 3.5μs/750μA, 8μs/450μA
LTC1655/LTC1655L	Single 16-Bit V_{OUT} DAC with Serial Interface in SO-8	V_{CC} = 5V(3V), Low Power, Deglitched
LTC1657/LTC1657L	Parrallel 5V/3V 16-Bit V_{OUT} DAC	Low Power, Deglitched, Rail-to-Rail V_{OUT}
LTC1660/LTC1665	Octal 8/10-Bit V_{OUT} DAC in 16-Pin Narrow SSOP	V_{CC} = 2.7V to 5.5V, Micropower, Rail-to-Rail Output
LTC1821	Parallel 16-Bit Voltage Output DAC	Precision 16-Bit Settling in 2μs for 10V Step
LTC2600/LTC2610/LTC2620	Octal 16-/14-/12-Bit Rail-to-Rail DACs in 16-Lead SSOP	250μA per DAC, 2.5V to 5.5V Supply Range
LTC2602/LTC2612/LTC2622	Dual 16-/14-/12-Bit Rail-to-Rail DACs in 8-Lead MSOP	300μA per DAC, 2.5V to 5.5V Supply Range

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