

- Member of the Texas Instruments **Widebus™** Family
- **EPIC™** (Enhanced-Performance Implanted CMOS) Submicron Process
- **DOC™** (Dynamic Output Control) Circuit Dynamically Changes Output Impedance, Resulting in Noise Reduction Without Speed Degradation
- Dynamic Drive Capability Is Equivalent to Standard Outputs With  $I_{OH}$  and  $I_{OL}$  of  $\pm 24$  mA at 2.5-V  $V_{CC}$
- Overvoltage-Tolerant Inputs/Outputs Allow Mixed-Voltage-Mode Data Communications
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Ideal for Use in PC133 Registered DIMM Applications
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- Package Options Include Plastic Thin Shrink Small-Outline (DGG) and Thin Very Small-Outline (DGV) Packages

## description

A Dynamic Output Control (DOC) circuit is implemented, which, during the transition, initially lowers the output impedance to effectively drive the load and, subsequently, raises the impedance to reduce noise. Figure 1 shows typical  $V_{OL}$  vs  $I_{OL}$  and  $V_{OH}$  vs  $I_{OH}$  curves to illustrate the output impedance and drive capability of the circuit. At the beginning of the signal transition, the DOC circuit provides a maximum dynamic drive that is equivalent to a high-drive standard-output device. For more information, refer to the TI application reports, *AVC Logic Family Technology and Applications*, literature number SCEA006, and *Dynamic Output Control (DOC™) Circuitry Technology and Applications*, literature number SCEA009.

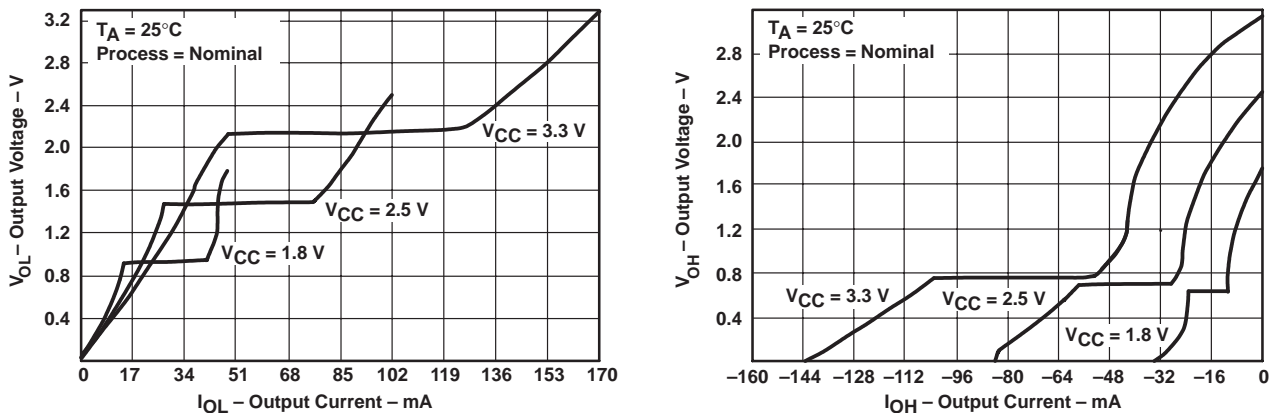


Figure 1. Output Voltage vs Output Current

This 18-bit universal bus driver is operational at 1.2-V to 3.6-V  $V_{CC}$ , but is designed specifically for 1.65-V to 3.6-V  $V_{CC}$  operation.

Data flow from A to Y is controlled by the output-enable ( $\overline{OE}$ ) input. The device operates in the transparent mode when the latch-enable ( $\overline{LE}$ ) input is low. The A data is latched if the clock (CLK) input is held at a high or low logic level. If  $\overline{LE}$  is high, the A data is stored in the latch/flip-flop on the low-to-high transition of CLK. When  $\overline{OE}$  is high, the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.



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SN74AVC16834

18-BIT UNIVERSAL BUS DRIVER

WITH 3-STATE OUTPUTS

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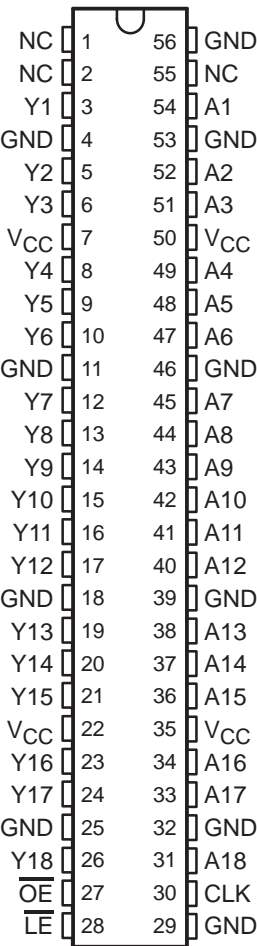
description (continued)

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The SN74AVC16834 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

terminal assignments

DGG OR DGV PACKAGE  
(TOP VIEW)



NC – No internal connection

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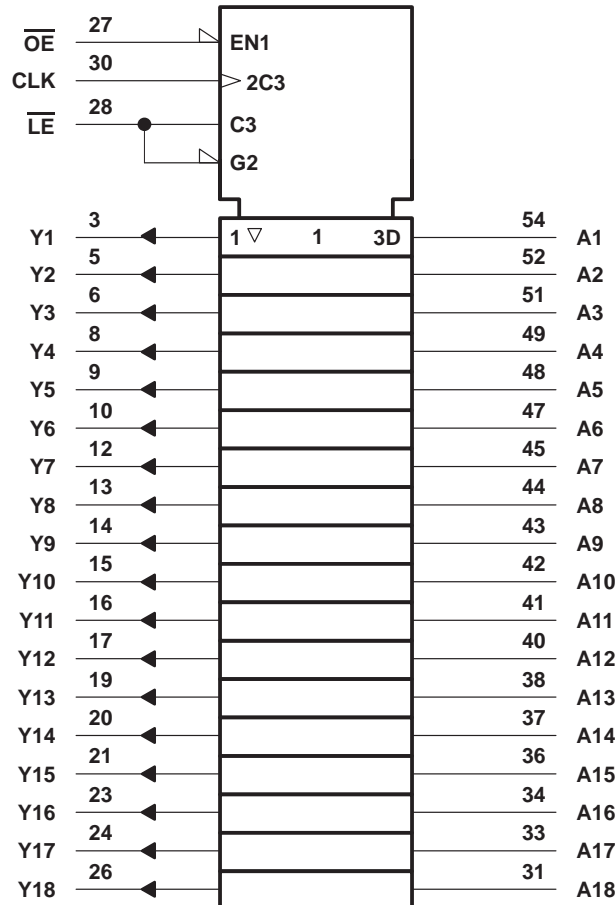
**FUNCTION TABLE**  
 (each universal bus driver)

INPUTS				OUTPUT Y
$\overline{\text{OE}}$	$\overline{\text{LE}}$	CLK	A	
H	X	X	X	Z
L	L	X	L	L
L	L	X	H	H
L	H	↑	L	L
L	H	↑	H	H
L	H	H	X	$Y_0^\dagger$
L	H	L	X	$Y_0^\ddagger$

† Output level before the indicated steady-state input conditions were established, provided that CLK is high before  $\overline{\text{LE}}$  goes high

‡ Output level before the indicated steady-state input conditions were established

**logic symbols**



§ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

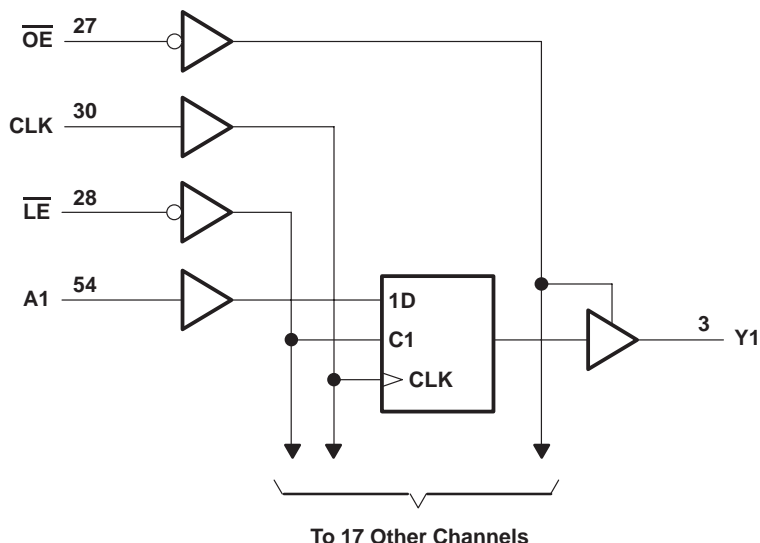
# SN74AVC16834

## 18-BIT UNIVERSAL BUS DRIVER

### WITH 3-STATE OUTPUTS

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#### logic diagram (positive logic)



#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$	–0.5 V to 4.6 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 4.6 V
Voltage range applied to any output in the high-impedance or power-off state, $V_O$ (see Note 1)	–0.5 V to 4.6 V
Voltage range applied to any output in the high or low state, $V_O$ (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ )	–50 mA
Continuous output current, $I_O$	±50 mA
Continuous current through each $V_{CC}$ or GND	±100 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): DGG package	64°C/W
DGV package	48°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.  
 2. The output positive-voltage rating may be exceeded up to 4.6 V maximum if the output current rating is observed.  
 3. The package thermal impedance is calculated in accordance with JESD 51.

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**recommended operating conditions (see Note 4)**

		MIN	MAX	UNIT	
V <sub>CC</sub>	Supply voltage	Operating	1.4	3.6	V
		Data retention only	1.2		
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 1.2 V	V <sub>CC</sub>		V
		V <sub>CC</sub> = 1.4 V to 1.6 V	0.65 × V <sub>CC</sub>		
		V <sub>CC</sub> = 1.65 V to 1.95 V	0.65 × V <sub>CC</sub>		
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7		
		V <sub>CC</sub> = 3 V to 3.6 V	2		
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 1.2 V	GND		V
		V <sub>CC</sub> = 1.4 V to 1.6 V	0.35 × V <sub>CC</sub>		
		V <sub>CC</sub> = 1.65 V to 1.95 V	0.35 × V <sub>CC</sub>		
		V <sub>CC</sub> = 2.3 V to 2.7 V	0.7		
		V <sub>CC</sub> = 3 V to 3.6 V	0.8		
V <sub>I</sub>	Input voltage	0	3.6	V	
V <sub>O</sub>	Output voltage	Active state	0	V <sub>CC</sub>	V
		3-state	0	3.6	
I <sub>OHS</sub>	Static high-level output current†	V <sub>CC</sub> = 1.4 V to 1.6 V	–2		mA
		V <sub>CC</sub> = 1.65 V to 1.95 V	–4		
		V <sub>CC</sub> = 2.3 V to 2.7 V	–8		
		V <sub>CC</sub> = 3 V to 3.6 V	–12		
I <sub>OLS</sub>	Static low-level output current†	V <sub>CC</sub> = 1.4 V to 1.6 V	2		mA
		V <sub>CC</sub> = 1.65 V to 1.95 V	4		
		V <sub>CC</sub> = 2.3 V to 2.7 V	8		
		V <sub>CC</sub> = 3 V to 3.6 V	12		
Δt/Δv	Input transition rise or fall rate	V <sub>CC</sub> = 1.4 V to 3.6 V	5	ns/V	
T <sub>A</sub>	Operating free-air temperature	–40	85	°C	

<sup>†</sup> Dynamic drive capability is equivalent to standard outputs with  $I_{OH}$  and  $I_{OL}$  of  $\pm 24\text{ mA}$  at  $2.5\text{-V }V_{CC}$ . See Figure 1 for  $V_{OL}$  vs  $I_{OL}$  and  $V_{OH}$  vs  $I_{OH}$  characteristics. Refer to the TI application reports, **AVC Logic Family Technology and Applications**, literature number **SCEA006**, and **Dynamic Output Control (DOC™) Circuitry Technology and Applications**, literature number **SCEA009**.

NOTE 4: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP†	MAX	UNIT
V <sub>OH</sub>	I <sub>OHS</sub> = –100 µA		1.4 V to 3.6 V	V <sub>CC</sub> –0.2			V
	I <sub>OHS</sub> = –2 mA,	V <sub>IH</sub> = 0.91 V	1.4 V	1.05			
	I <sub>OHS</sub> = –4 mA,	V <sub>IH</sub> = 1.07 V	1.65 V	1.2			
	I <sub>OHS</sub> = –8 mA,	V <sub>IH</sub> = 1.7 V	2.3 V	1.75			
	I <sub>OHS</sub> = –12 mA,	V <sub>IH</sub> = 2 V	3 V	2.3			
V <sub>OL</sub>	I <sub>OLS</sub> = 100 µA		1.4 V to 3.6 V			0.2	V
	I <sub>OLS</sub> = 2 mA,	V <sub>IL</sub> = 0.49 V	1.4 V			0.4	
	I <sub>OLS</sub> = 4 mA,	V <sub>IL</sub> = 0.57 V	1.65 V			0.45	
	I <sub>OLS</sub> = 8 mA,	V <sub>IL</sub> = 0.7 V	2.3 V			0.55	
	I <sub>OLS</sub> = 12 mA,	V <sub>IL</sub> = 0.8 V	3 V			0.7	
I <sub>I</sub>	Control inputs	V <sub>I</sub> = V <sub>CC</sub> or GND	3.6 V			±2.5	µA
I <sub>off</sub>		V <sub>I</sub> or V <sub>O</sub> = 3.6 V	0			±10	µA
I <sub>OZ</sub>		V <sub>O</sub> = V <sub>CC</sub> or GND	3.6 V			±10	µA
I <sub>CC</sub>		V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	3.6 V			40	µA
C <sub>i</sub>	CLK input	V <sub>I</sub> = V <sub>CC</sub> or GND	2.5 V			4	pF
			3.3 V			4	
	Control inputs	V <sub>I</sub> = V <sub>CC</sub> or GND	2.5 V			4	
			3.3 V			4	
	Data inputs	V <sub>I</sub> = V <sub>CC</sub> or GND	2.5 V			2.5	
			3.3 V			2.5	
C <sub>O</sub>	Outputs	V <sub>O</sub> = V <sub>CC</sub> or GND	2.5 V			6.5	pF
			3.3 V			6.5	

† Typical values are measured at T<sub>A</sub> = 25°C.

**timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 2 through 5)**

			V <sub>CC</sub> = 1.2 V		V <sub>CC</sub> = 1.5 V ± 0.1 V		V <sub>CC</sub> = 1.8 V ± 0.15 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency						150		150		150		MHz
t <sub>w</sub>	Pulse duration	$\overline{\text{LE}}$ low					3.3		3.3		3.3		ns
		CLK high or low						3.3		3.3		3.3	
t <sub>su</sub>	Setup time	Data before CLK↑		1		0.9		0.7		0.7		0.7	ns
		Data before $\overline{\text{LE}}$ ↑	CLK high	1.6		1.5		1		1		1	
			CLK low	3.1		1.7		1.3		1		1	
t <sub>h</sub>	Hold time	Data after CLK↑		1.5		1.3		1		0.9		0.9	ns
		Data after $\overline{\text{LE}}$ ↑	CLK high	2.5		2		1.8		1.5		1.4	
		Data after $\overline{\text{LE}}$ ↑	CLK low	2		1.7		1.5		1.3		1.3	



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**switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 2 through 5)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 1.2 V	V <sub>CC</sub> = 1.5 V ± 0.1 V		V <sub>CC</sub> = 1.8 V ± 0.15 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>max</sub>						150		150		150		MHz
t <sub>pd</sub>	A	Y	5.3	1.2	6.2	1.5	4.9	1	3.2	0.9	2.5	ns
	$\overline{\text{LE}}$		7	2.2	9.7	1.8	7.5	1.5	4.9	0.8	4	
	CLK		6	1.9	7.8	1.6	6	1.1	3.7	1	3.1	
t <sub>en</sub>	$\overline{\text{OE}}$	Y	7.9	2.4	10.2	1.6	8.8	1.5	6.7	1	6.2	ns
t <sub>dis</sub>	$\overline{\text{OE}}$	Y	7.7	2.1	10.3	1.5	8.4	1.2	5.3	1	5.3	ns

**switching characteristics, T<sub>A</sub> = 0°C to 85°C, C<sub>L</sub> = 0 pF†**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 3.3 V ± 0.15 V		UNIT
			MIN	MAX	
t <sub>pd</sub>	A	Y	0.6	1.3	ns
	CLK		0.7	1.5	

† Texas Instruments SPICE simulation data

**operating characteristics, T<sub>A</sub> = 25°C**

PARAMETER			TEST CONDITIONS	V <sub>CC</sub> = 1.8 V	V <sub>CC</sub> = 2.5 V	V <sub>CC</sub> = 3.3 V	UNIT
				TYP	TYP	TYP	
C <sub>pd</sub>	Power dissipation capacitance	Outputs enabled	C <sub>L</sub> = 0, f = 10 MHz	45	48	52	pF
		Outputs disabled		23	25	28	

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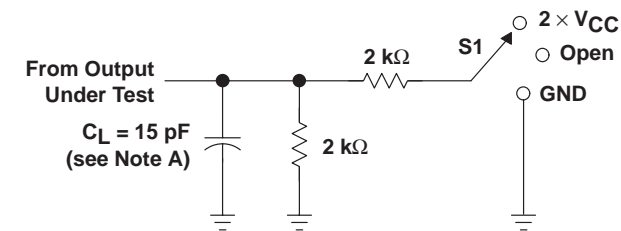
## 18-BIT UNIVERSAL BUS DRIVER

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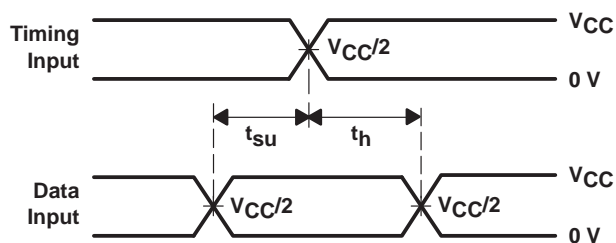
#### PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 1.2\text{ V AND }1.5\text{ V} \pm 0.1\text{ V}$

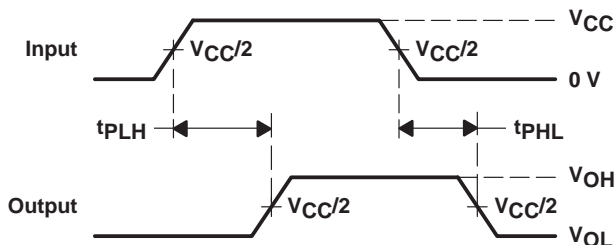


LOAD CIRCUIT

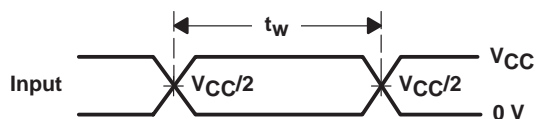
TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	$2 \times V_{CC}$
$t_{PHZ}/t_{PHZ}$	GND



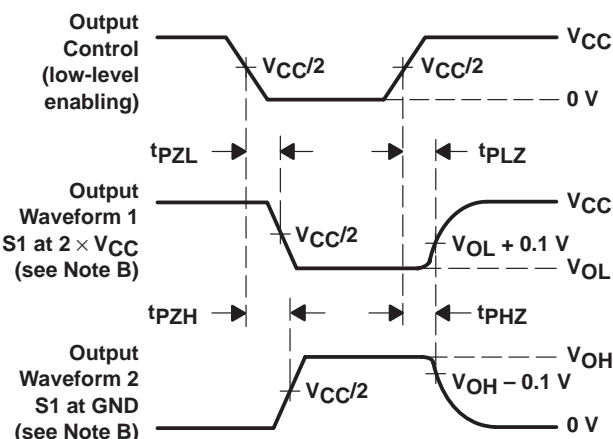
VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES

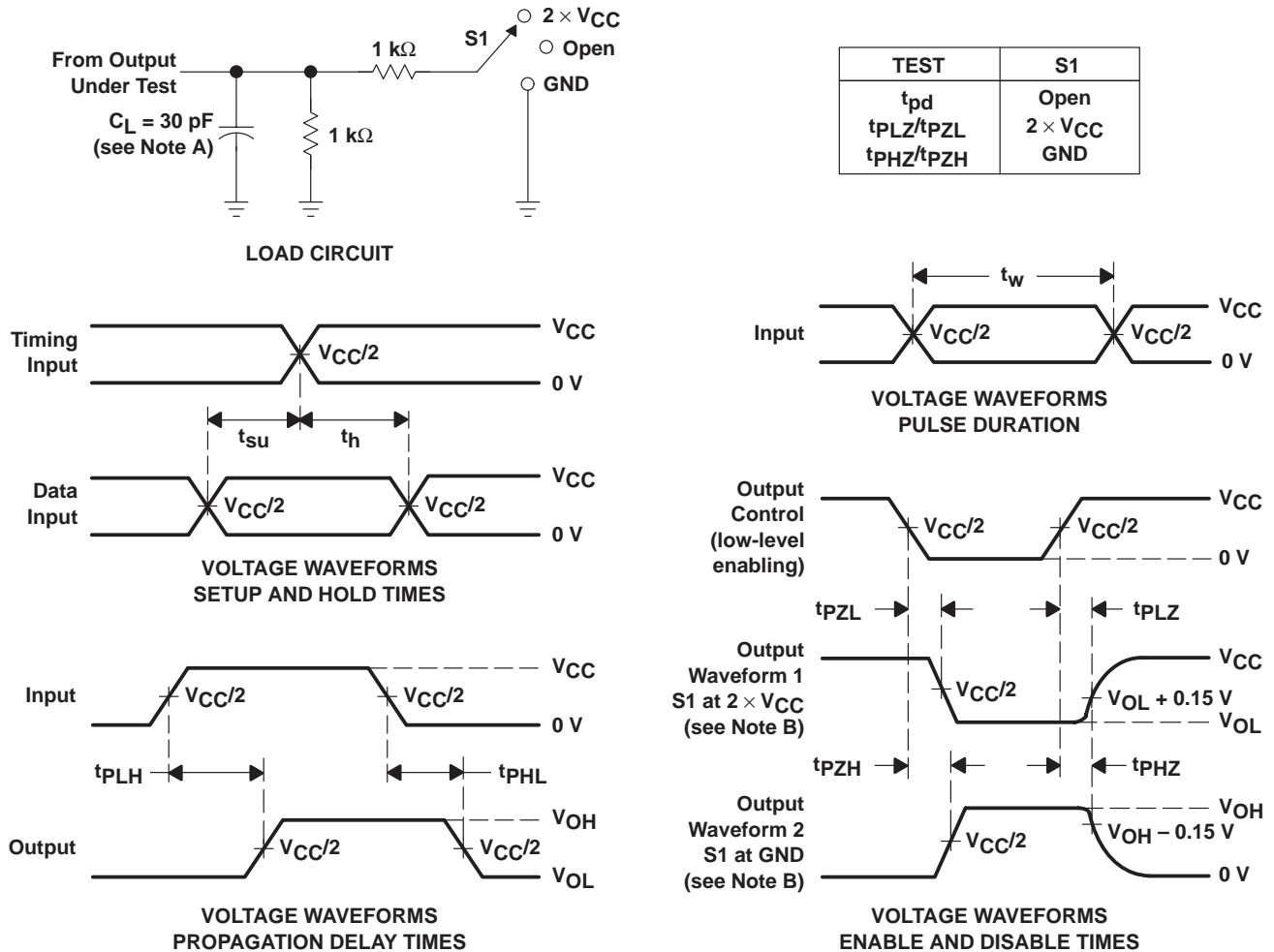
- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2\text{ ns}$ ,  $t_f \leq 2\text{ ns}$ .
  - The outputs are measured one at a time with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 2. Load Circuit and Voltage Waveforms



# PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$$



- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2 \text{ ns}$ ,  $t_f \leq 2 \text{ ns}$ .
  - The outputs are measured one at a time with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 3. Load Circuit and Voltage Waveforms

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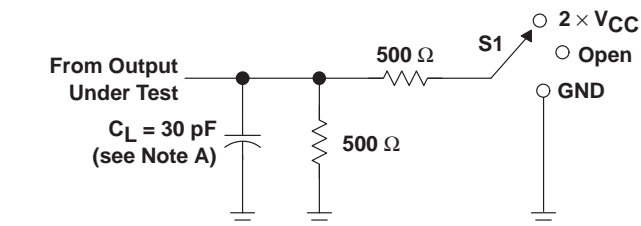
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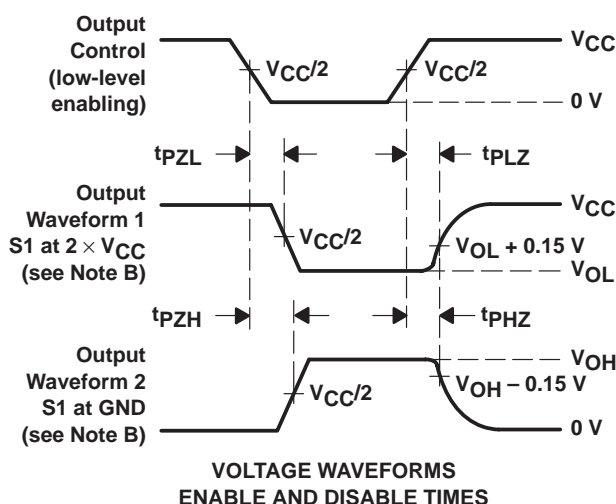
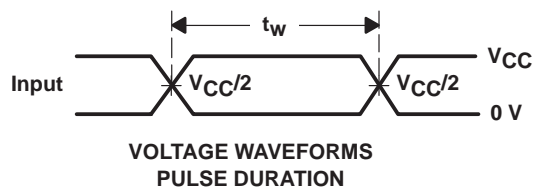
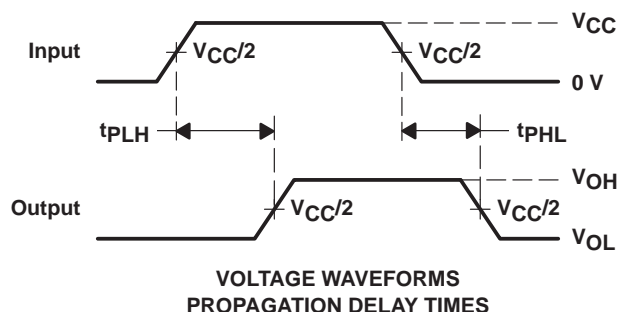
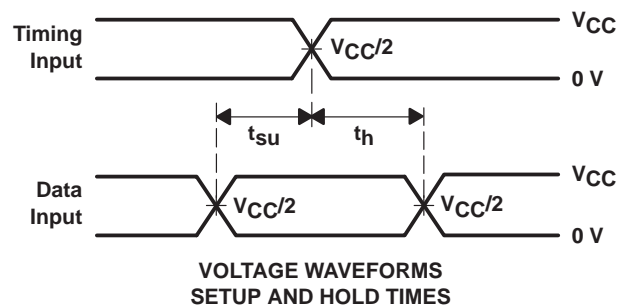
#### PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$



LOAD CIRCUIT

TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	2 $\times V_{CC}$
$t_{PHZ}/t_{PZH}$	GND

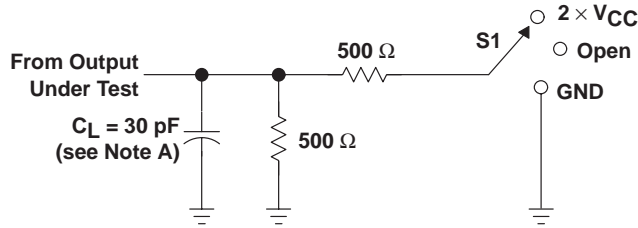


- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2 \text{ ns}$ ,  $t_f \leq 2 \text{ ns}$ .
  - The outputs are measured one at a time with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 4. Load Circuit and Voltage Waveforms

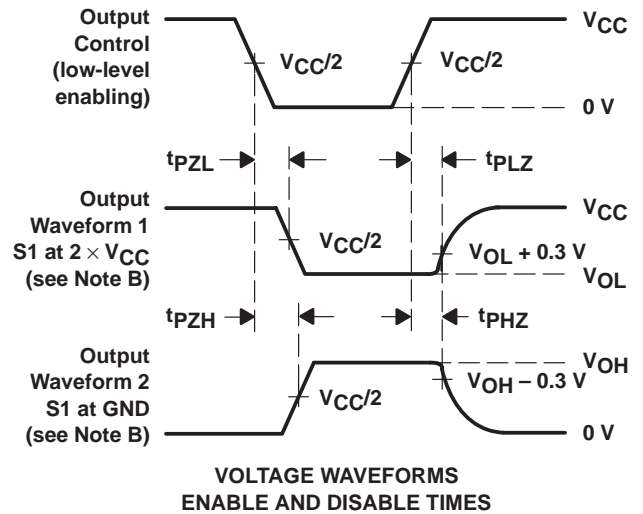
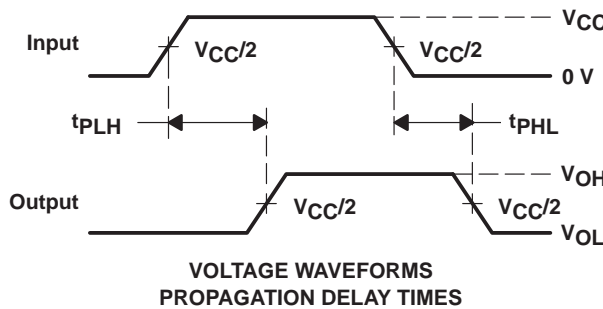
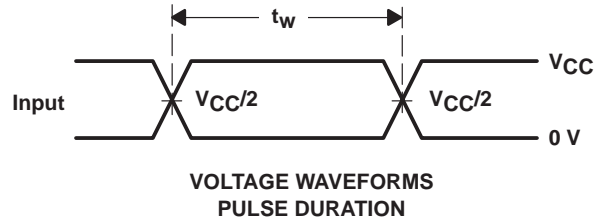
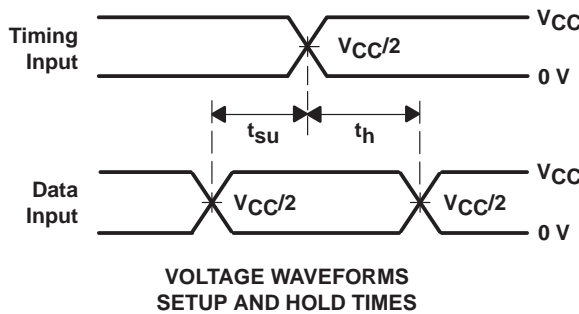
# PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$$



LOAD CIRCUIT

TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	2 $\times V_{CC}$
$t_{PHZ}/t_{PZH}$	GND



- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2 \text{ ns}$ ,  $t_f \leq 2 \text{ ns}$ .
  - The outputs are measured one at a time with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 5. Load Circuit and Voltage Waveforms

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