

SN74CBT16214

12-BIT 1-OF-3 FET MULTIPLEXER/DEMULTIPLEXER

SCDS008I – MAY 1993 – REVISED MAY 1998

- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Input Levels
- Package Options Include Plastic Thin Shrink Small-Outline (DGG) and 300-mil Shrink Small-Outline (DL) Packages

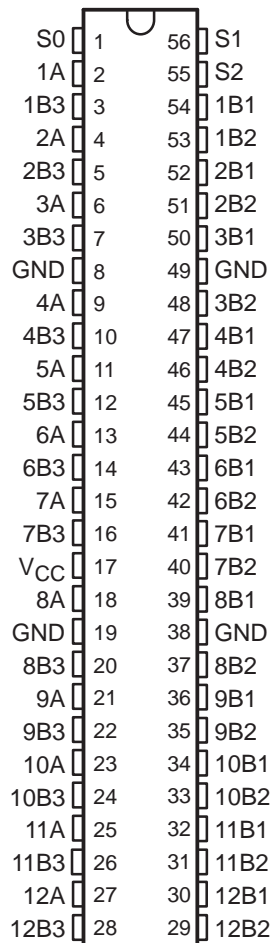
description

The SN74CBT16214 provides 12 bits of high-speed TTL-compatible bus switching between three separate ports. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device operates as a 12-bit bus-select switch via the data-select (S0–S2) terminals.

The SN74CBT16214 is characterized for operation from –40°C to 85°C.

DGG OR DL PACKAGE (TOP VIEW)



FUNCTION TABLE

INPUTS			INPUT/OUTPUT A	FUNCTION
S2	S1	S0		
L	L	L	Z	Disconnect
L	L	H	B1	A port = B1 port
L	H	L	B2	A port = B2 port
L	H	H	Z	Disconnect
H	L	L	Z	Disconnect
H	L	H	B3	A port = B3 port
H	H	L	B1	A port = B1 port
H	H	H	B2	A port = B2 port



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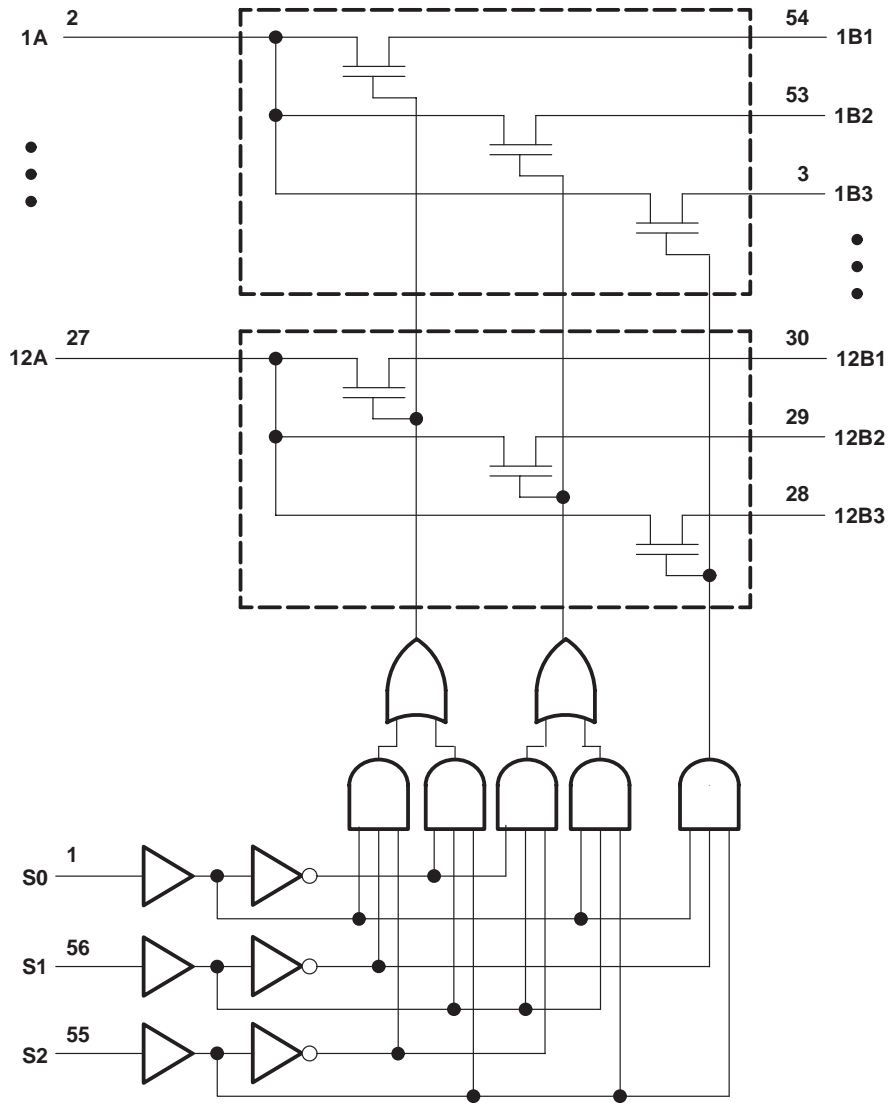
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SCDS0081 – MAY 1993 – REVISED MAY 1998

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Continuous channel current	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Package thermal impedance, θ_{JA} (see Note 2): DGG package	81°C
	DL package	74°C
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. The package thermal impedance is calculated in accordance with JESD 51.



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recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V _{CC}	Supply voltage	4	5.5	V
V _{IH}	High-level control input voltage	2		V
V _{IL}	Low-level control input voltage		0.8	V
T _A	Operating free-air temperature	-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT		
V _{IK}		V _{CC} = 4.5 V,	I _I = -18 mA			-1.2	V		
I _I		V _{CC} = 0,	V _I = 5.5 V			10	μA		
		V _{CC} = 5.5 V,	V _I = 5.5 V or GND			±1			
I _{CC}		V _{CC} = 5.5 V,	I _O = 0, V _I = V _{CC} or GND			3	μA		
ΔI _{CC} ‡	Control inputs	V _{CC} = 5.5 V,	One input at 3.4 V, Other inputs at V _{CC} or GND			2.5	mA		
C _i	Control inputs	V _I = 3 V or 0				4	pF		
C _{io(OFF)}		V _O = 3 V or 0,	A = Z			7.5	pF		
r _{on} §		V _{CC} = 4 V, TYP at V _{CC} = 4 V	V _I = 2.4 V, I _I = 15 mA				Ω		
		V _{CC} = 4.5 V	V _I = 0			4		7	
				I _I = 64 mA				4	7
				I _I = 30 mA				4	7
		V _I = 2.4 V,	I _I = 15 mA			6	12		

† All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4 V		V _{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	
t _{pd} ¶	A or B	B or A	0.35		0.25		ns
t _{pd}	S	B or A	15.3		5.5	13.9	ns
t _{en}	S	A or B	16		5.1	14.5	ns
t _{dis}	S	A or B	12.1		3.6	11.7	ns

¶ The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

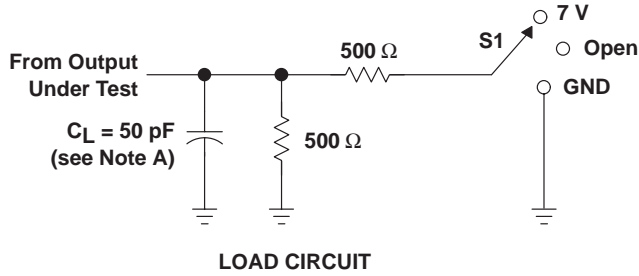


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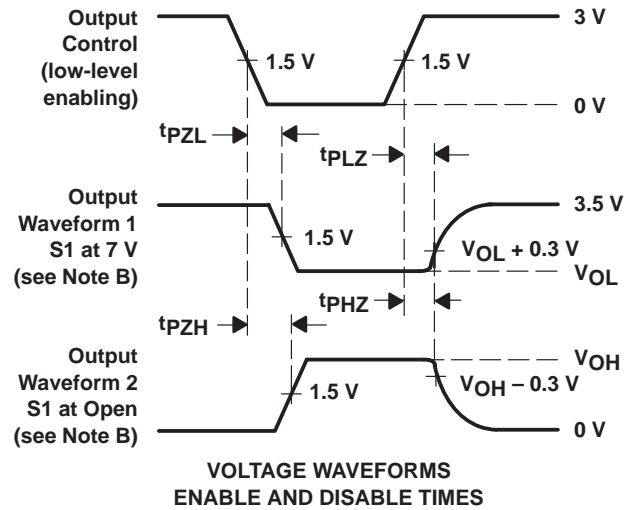
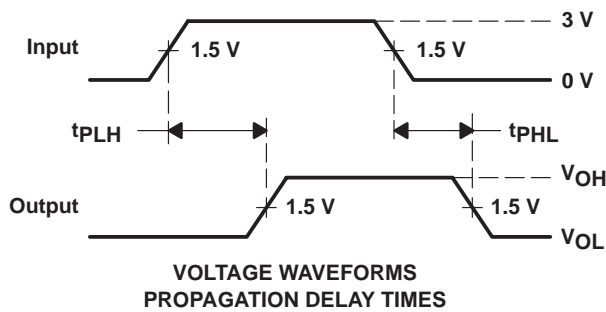
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PARAMETER MEASUREMENT INFORMATION



TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

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