19-1192; Rev 3; 2/98

MAXIM

Single/Dual/Quad, Low-Power, Single-Supply, Rail-to-Rail I/O Op Amps with Shutdown

General Description

The MAX4330–MAX4334 single/dual/quad op amps combine a wide 3MHz bandwidth, low-power operation, and excellent DC accuracy with Rail-to-Rail® inputs and outputs. These devices require only 245µA per amplifier, and operate from either a single +2.3V to +6.5V supply or dual ±1.15V to ±3.25V supplies. The input common-mode voltage range extends 250mV beyond V_{EE} and V_{CC}, and the outputs swing rail-to-rail. The MAX4331/MAX4333 feature a shutdown mode in which the output goes high impedance and the supply current decreases to 9µA per amplifier.

Low-power operation combined with rail-to-rail input common-mode range and output swing makes these amplifiers ideal for portable/battery-powered equipment and other low-voltage, single-supply applications. Although the minimum operating voltage is specified at 2.3V, these devices typically operate down to 2.0V. Low offset voltage and high speed make these amplifiers excellent choices for signal-conditioning stages in precision, low-voltage data-acquisition systems. The MAX4330 is available in the space-saving 5-pin SOT23 package, and the MAX4331/MAX4333 are offered in a µMAX package.

Applications

Portable/Battery-Powered Equipment

Data-Acquisition Systems

Signal Conditioning

Low-Power, Low-Voltage Applications

Selector Guide

PART	NO. OF AMPS PER PACKAGE	SHUTDOWN MODE	PIN-PACKAGE
MAX4330	1	—	5-pin SOT23
MAX4331	1	Yes	8-pin SO/µMAX
MAX4332	2	—	8-pin SO
MAX4333	2	Yes	10-pin µMAX, 14-pin SO
MAX4334	4	—	14-pin SO

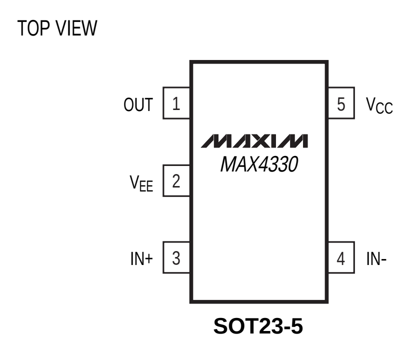
Features

- **3MHz Gain-Bandwidth Product**
- **245µA Quiescent Current per Amplifier**
- **Available in Space-Saving SOT23-5 Package (MAX4330)**
- **+2.3V to +6.5V Single-Supply Operation**
- **Rail-to-Rail Input Common-Mode Voltage Range**
- **Rail-to-Rail Output Voltage Swing**
- **250µV Offset Voltage**
- **Low-Power, 9µA (per amp) Shutdown Mode (MAX4331/MAX4333)**
- **No Phase Reversal for Overdriven Inputs**
- **Capable of Driving 2kΩ Loads**
- **Unity-Gain Stable**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	SOT TOP MARK
MAX4330EUK-T	-40°C to +85°C	5 SOT23-5	ABAJ
MAX4331ESA	-40°C to +85°C	8 SO	—
MAX4331EUA	-40°C to +85°C	8 µMAX	—
MAX4332ESA	-40°C to +85°C	8 SO	—
MAX4333ESD	-40°C to +85°C	14 SO	—
MAX4333EUB	-40°C to +85°C	10 µMAX	—
MAX4334ESD	-40°C to +85°C	14 SO	—

Pin Configurations



Pin Configurations continued at end of data sheet.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} to V_{EE} 7V
IN_+, IN_-, $\overline{SHDN}$ Voltage................(V_{EE} - 0.3V) to (V_{CC} + 0.3V)
Output Short-Circuit Duration................................... Continuous (short to either supply)
Continuous Power Dissipation (T_A = +70°C)
5-Pin SOT23 (derate 7.1mW/°C above +70°C).............571mW
8-Pin SO (derate 5.88mW/°C above +70°C).................471mW
8-Pin µMAX (derate 4.10mW/°C above +70°C) 330mW
10-Pin µMAX (derate 5.60mW/°C above +70°C) 444mW
14-Pin SO (derate 8.33mW/°C above +70°C)...............667mW
Operating Temperature Ranges
MAX433_C/D ....0°C to +70°C
MAX433_E_ _...-40°C to +85°C
Maximum Junction Temperature ....+150°C
Storage Temperature Range ....-65°C to +160°C
Lead Temperature (soldering, 10sec) ....+300°C

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.3V to +6.5V, V_{EE} = 0V, V_{CM} = 0V, V_{OUT} = (V_{CC} / 2), R_L tied to (V_{CC} / 2), $V_{\overline{SHDN}} \geq$ 2V, **T_A = +25°C,** unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	V_{CM} = V_{EE} to V_{CC}		MAX433_EUA/EUB		±0.65	±1.5	mV
				MAX4330EUK		±0.65	±1.5	
				MAX4331ESA		±0.25	±0.6	
				MAX4332ESA/MAX4333ESD		±0.25	±0.9	
				MAX4334ESD		±0.25	±1.0	
Input Bias Current	I_B	$V_{EE} < V_{CM} < V_{CC}$				±25	±65	nA
Input Offset Current	I_{OS}	$V_{EE} < V_{CM} < V_{CC}$				±1	±12	nA
Differential Input Resistance	$R_{IN(DIFF)}$	$\lvert V_{IN+} - V_{IN-} \rvert < 1.4V$				2.3		MΩ
		$\lvert V_{IN+} - V_{IN-} \rvert > 2.5V$				2		kΩ
Common-Mode Input Voltage Range	V_{CM}				-0.25		V_{CC} + 0.25	V
Common-Mode Rejection Ratio	CMRR	-0.25V < V_{CM} < (V_{CC} + 0.25V)	V_{CC} = 5V	MAX433_EUA/EUB	68	88		dB
				MAX4330EUK	67	87		
				MAX4331ESA	74	93		
				MAX4332ESA/ MAX4333ESD	71	93		
				MAX4334ESD	69	92		
			V_{CC} = 2.3V	MAX433_EUA/EUB	65	84		dB
				MAX4330EUK	64	82		
				MAX4331ESA	71	90		
				MAX4332ESA/ MAX4333ESD	69	90		
				MAX4334ESD	66	89		
Power-Supply Rejection Ratio	PSSR	V_{CC} = 2.3V to 6.5V		MAX433_EUA/EUB	76	88		dB
				MAX4330EUK	76	88		
				MAX4331ESA	79	92		
				MAX4332ESA/ MAX4333ESD	77	90		
				MAX4334ESD	75	90		
Output Resistance	R_{OUT}	A_V = 1				0.1		Ω
Off-Leakage Current in Shutdown	$I_{OUT(\overline{SHDN})}$	$V_{\overline{SHDN}}$ < 0.8V, V_{OUT} = 0V to V_{CC}				±0.1	±2	µA

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +2.3V to +6.5V, V_{EE} = 0V, V_{CM} = 0V, V_{OUT} = (V_{CC} / 2), R_L tied to (V_{CC} / 2), $V_{\overline{SHDN}}$ ≥ 2V, **T_A = +25°C,** unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Large-Signal Voltage Gain	A_{VOL}	V_{CC} = 2.3V	V_{OUT} = 0.2V to 2.1V, R_L = 100kΩ	93	112		dB
			V_{OUT} = 0.35V to 1.95V, R_L = 2kΩ	78	90		
		V_{CC} = 5V	V_{OUT} = 0.2V to 4.8V, R_L = 100kΩ	93	120		
			V_{OUT} = 0.35V to 4.65V, R_L = 2kΩ	83	95		
Output Voltage Swing	V_{OUT}	R_L = 100kΩ	V_{CC} - V_{OH}		8	30	mV
			V_{OL}		8	30	
		R_L = 2kΩ	V_{CC} - V_{OH}		100	175	
			V_{OL}		70	150	
Output Short-Circuit Current	I_{SC}				20		mA
$\overline{SHDN}$ Logic Threshold (Note 1)	V_{IL}	Low (shutdown mode)				0.8	V
	V_{IH}	High (normal mode)		2.0			
$\overline{SHDN}$ Input Current		V_{EE} < $V_{\overline{SHDN}}$ < V_{CC}				±2	µA
Operating Supply-Voltage Range	V_{CC}			2.3		6.5	V
Quiescent Supply Current per Amplifier	I_{CC}	V_{CM} = V_{OUT} = V_{CC} / 2	V_{CC} = 5V		275	325	µA
			V_{CC} = 2.3V		245	290	
Shutdown Supply Current per Amplifier	$I_{CC(\overline{SHDN})}$	$V_{\overline{SHDN}}$ < 0.8V	V_{CC} = 5V		17	25	µA
			V_{CC} = 2.3V		9	14	

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.3V to +6.5V, V_{EE} = 0V, V_{CM} = 0V, V_{OUT} = (V_{CC} / 2), R_L tied to (V_{CC} / 2), $V_{\overline{SHDN}}$ ≥ 2V, **T_A = -40°C to +85°C,** unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	V_{CM} = V_{EE} to V_{CC}	MAX433_EUA			±3.2	mV
			MAX433_EUK/EUB			±3.8	
			MAX4331ESA			±0.7	
			MAX4332ESA/MAX4333ESD			±1	
			MAX4334ESD			±1	
Offset-Voltage Tempco	$\Delta V_{OS}/\Delta T$				±3		µV/°C
Input Bias Current	I_B	V_{EE} < V_{CM} < V_{CC}				±115	nA
Input Offset Current	I_{OS}	V_{EE} < V_{CM} < V_{CC}				±15	nA
Power-Supply Rejection Ratio	PSRR	V_{CC} = 2.3V to 6.5V	MAX433_EUA	72			dB
			MAX433_EUK/EUB	71			
			MAX4331ESA	76			
			MAX4332ESA/ MAX4333ESD	73			
			MAX4334ESD	71			
Common-Mode Input Voltage Range	V_{CM}			-0.15		V_{CC} + 0.15	V

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +2.3V to +6.5V, V_{EE} = 0V, V_{CM} = 0V, V_{OUT} = (V_{CC} / 2), R_L tied to (V_{CC} / 2), $V_{\overline{SHDN}} \geq$ 2V, **T_A = -40°C to +85°C,** unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
Common-Mode Rejection Ratio	CMRR	-0.25V < V_{CM} < (V_{CC} + 0.25V)	V_{CC} = 5V	MAX433_EUA/EUB	63			dB
				MAX4330EUK	62			
				MAX4331ESA	72			
				MAX4332ESA/ MAX4333ESD	69			
				MAX4334ESD	67			
			V_{CC} = 2.3V	MAX433_EUA/EUB	58			
				MAX4330EUK	57			
				MAX4331ESA	68			
				MAX4332ESA/ MAX4333ESD	66			
				MAX4334ESD	65			
Off-Leakage Current in Shutdown	$I_{OUT(\overline{SHDN})}$	$V_{\overline{SHDN}}$ < 0.8V, V_{OUT} = 0V to V_{CC}					±5	µA
Large-Signal Voltage Gain	A_{VOL}	V_{CC} = 2.3V	V_{OUT} = 0.2V to 2.1V, R_L = 100kΩ		90			dB
			V_{OUT} = 0.35V to 1.95V, R_L = 2kΩ		70			
		V_{CC} = 5V	V_{OUT} = 0.2V to 4.8V, R_L = 100kΩ		90			
			V_{OUT} = 0.35V to 4.65V, R_L = 2kΩ		74			
Output Voltage Swing	V_{OUT}	R_L = 100kΩ	V_{CC} - V_{OH}				40	mV
			V_{OL}				40	
		R_L = 2kΩ	V_{CC} - V_{OH}				200	
			V_{OL}				180	
$\overline{SHDN}$ Logic Threshold (Note 1)	V_{IL}	Low (shutdown mode)					0.8	V
	V_{IH}	High (normal mode)			2.0			
$\overline{SHDN}$ Input Current		V_{EE} < $V_{\overline{SHDN}}$ < V_{CC}					±2	µA
Operating Supply-Voltage Range	V_{CC}	T_A = -40°C to +85°C			2.3		6.5	V
Quiescent Supply Current per Amplifier	I_{CC}	V_{CM} = V_{OUT} = V_{CC} / 2	V_{CC} = 5V				350	µA
			V_{CC} = 2.3V				330	
Shutdown Supply Current per Amplifier	$I_{CC(\overline{SHDN})}$	$V_{\overline{SHDN}}$ < 0.8V	V_{CC} = 5V				30	µA
			V_{CC} = 2.3V				17	

Note 1: $\overline{SHDN}$ logic thresholds are referenced to V_{EE}.

Note 2: The MAX4330EUK is 100% tested at T_A = +25°C. All temperature limits are guaranteed by design.

AC ELECTRICAL CHARACTERISTICS

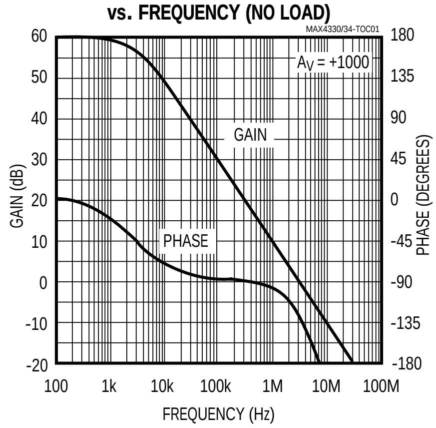
(V_{CC} = +5V, V_{EE} = 0V, V_{CM} = 0V, V_{OUT} = (V_{CC} / 2), R_L = 10kΩ to (V_{CC} / 2), $V_{\overline{SHDN}}$ ≥ 2V, C_L = 15pF, **T_A = +25°C,** unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Gain-Bandwidth Product	GBWP			3		MHz
Full-Power Bandwidth	FPBW	V_{OUT} = 4Vp-p		190		kHz
Slew Rate	SR			1.5		V/µs
Phase Margin	PM			55		degrees
Gain Margin	GM			10		dB
Total Harmonic Distortion	THD	f = 10kHz, V_{OUT} = 2Vp-p, A_{VCL} = +1V/V		0.012		%
Settling Time to 0.01%	t_S	A_V = +1V/V, 2V step		4		µs
Input Capacitance	C_{IN}			3		pF
Input Noise Voltage Density	V_{NOISE}	f = 10kHz		28		nV/√Hz
Input Current Noise Density	I_{NOISE}	f = 10kHz		0.26		pA/√Hz
Crosstalk		f = 10kHz, MAX4332/MAX4333/MAX4334		-124		dB
Capacitive Load Stability		A_V = 1, no sustained oscillations		150		pF
Shutdown Time	$t_{\overline{SHDN}}$			0.8		µs
Enable Time from Shutdown	t_{ENABLE}			1		µs
Power-Up Time	t_{ON}			5		µs

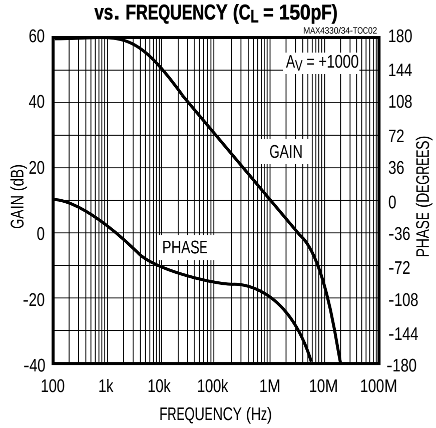
Typical Operating Characteristics

(V_{CC} = +5V, V_{EE} = 0V, V_{CM} = V_{CC} / 2, $V_{\overline{SHDN}}$ > 2V, T_A = +25°C, unless otherwise noted.)

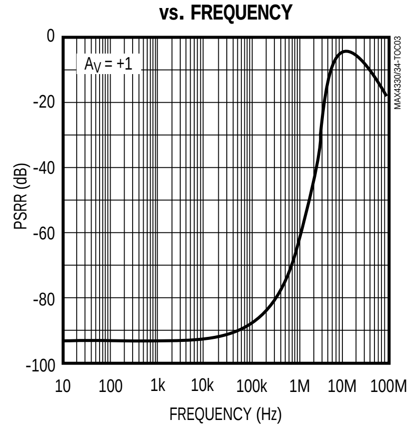
GAIN AND PHASE vs. FREQUENCY (NO LOAD)



GAIN AND PHASE vs. FREQUENCY (C_L = 150pF)



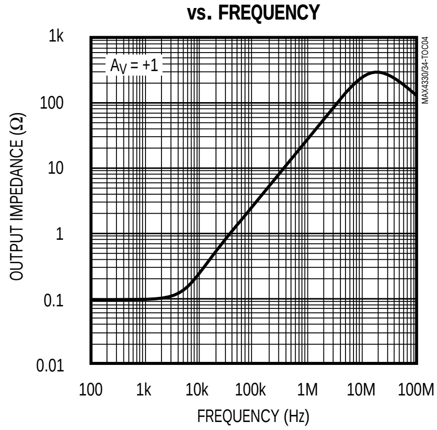
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



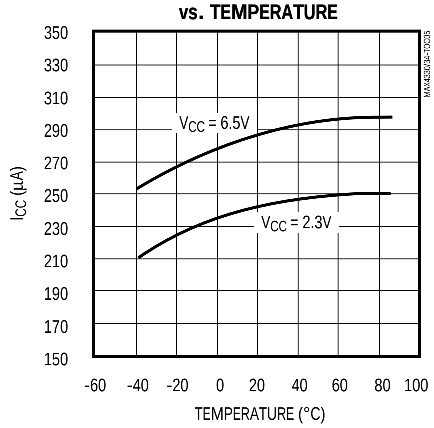
Typical Operating Characteristics (continued)

(V_{CC} = +5V, V_{EE} = 0V, V_{CM} = V_{CC} / 2, $V_{\overline{SHDN}}$ > 2V, T_A = +25°C, unless otherwise noted.)

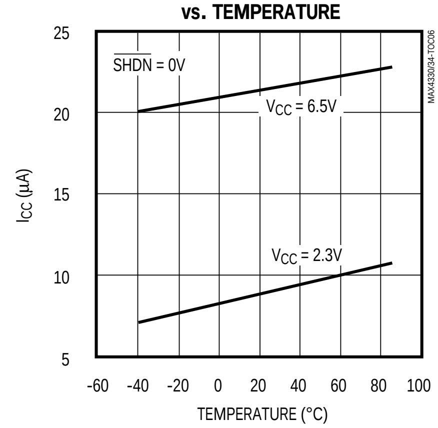
OUTPUT IMPEDANCE vs. FREQUENCY



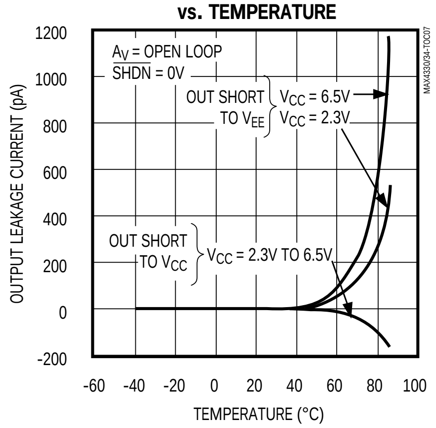
SUPPLY CURRENT vs. TEMPERATURE



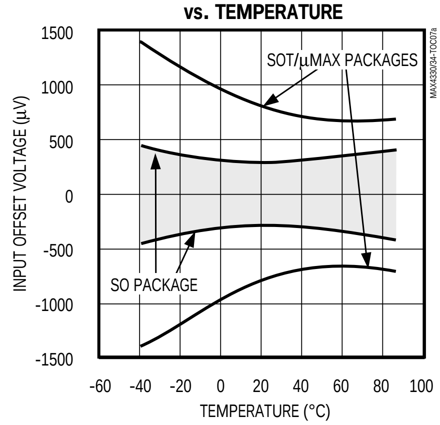
SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



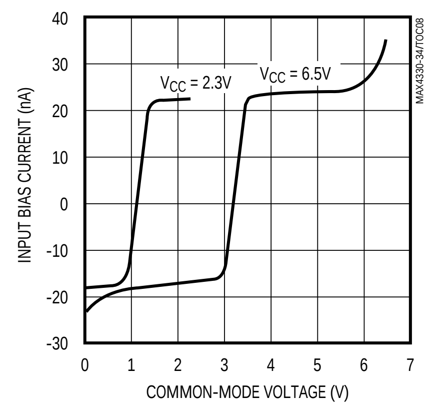
OUTPUT LEAKAGE CURRENT vs. TEMPERATURE



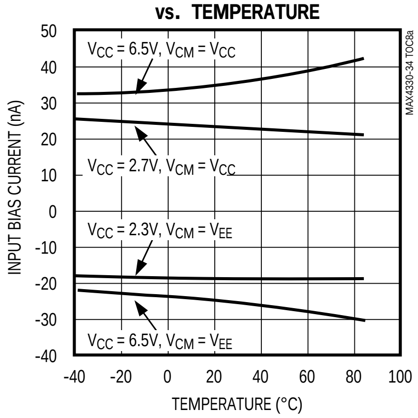
INPUT OFFSET VOLTAGE vs. TEMPERATURE



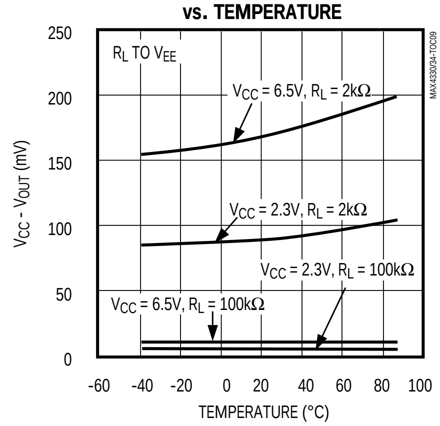
INPUT BIAS CURRENT vs. COMMON-MODE VOLTAGE



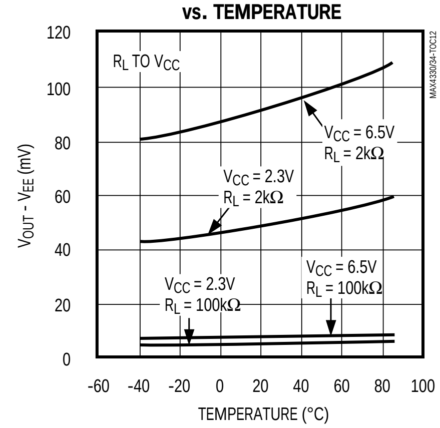
INPUT BIAS CURRENT vs. TEMPERATURE



OUTPUT SWING HIGH vs. TEMPERATURE



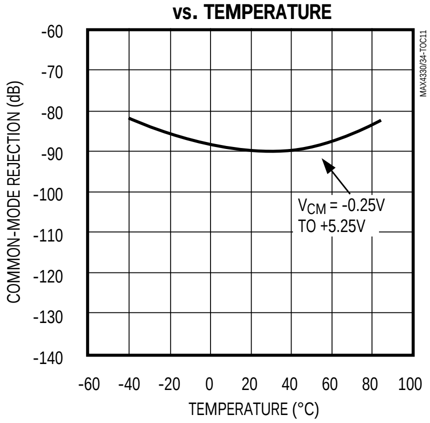
OUTPUT SWING LOW vs. TEMPERATURE



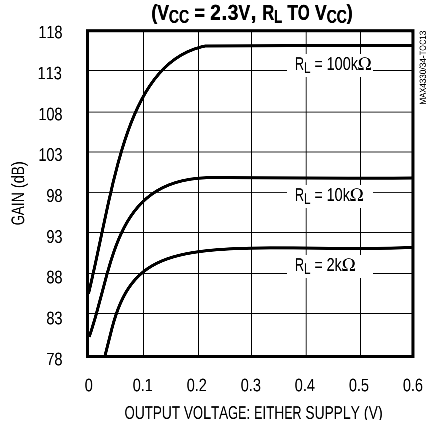
Typical Operating Characteristics (continued)

(V_{CC} = +5V, V_{EE} = 0V, V_{CM} = V_{CC} / 2, $V_{\overline{SHDN}}$ > 2V, T_A = +25°C, unless otherwise noted.)

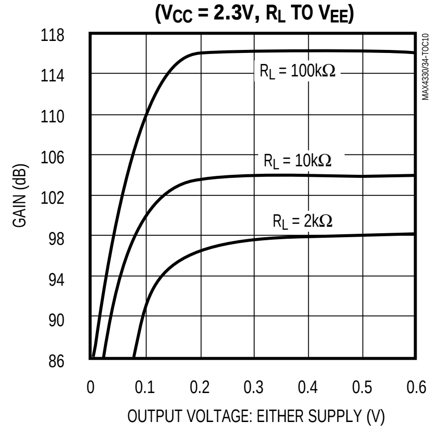
COMMON-MODE REJECTION vs. TEMPERATURE



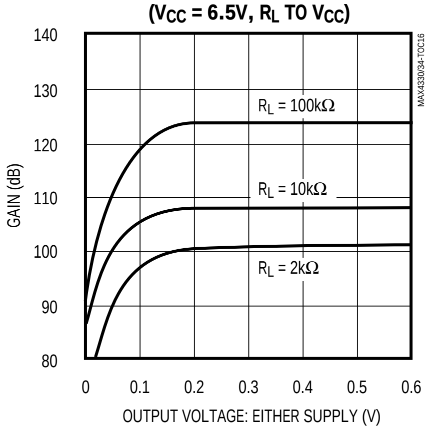
LARGE-SIGNAL GAIN vs. OUTPUT VOLTAGE (V_{CC} = 2.3V, R_L TO V_{CC})



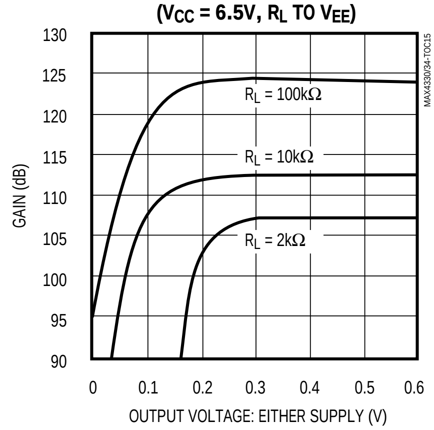
LARGE-SIGNAL GAIN vs. OUTPUT VOLTAGE (V_{CC} = 2.3V, R_L TO V_{EE})



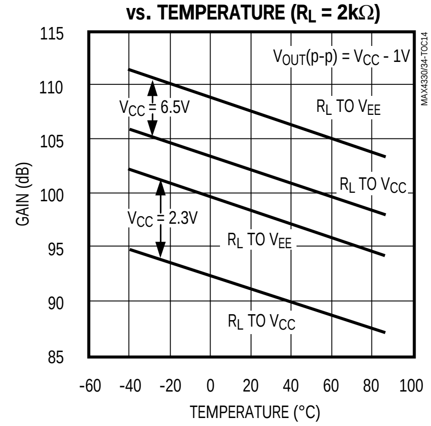
LARGE-SIGNAL GAIN vs. OUTPUT VOLTAGE (V_{CC} = 6.5V, R_L TO V_{CC})



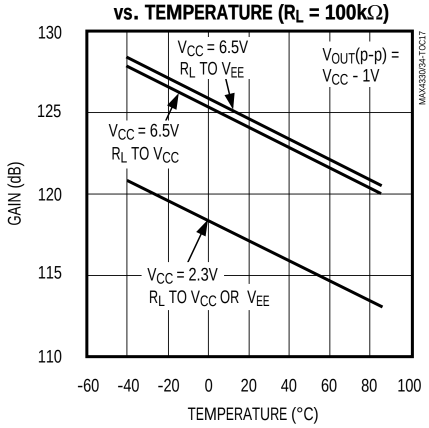
LARGE-SIGNAL GAIN vs. OUTPUT VOLTAGE (V_{CC} = 6.5V, R_L TO V_{EE})



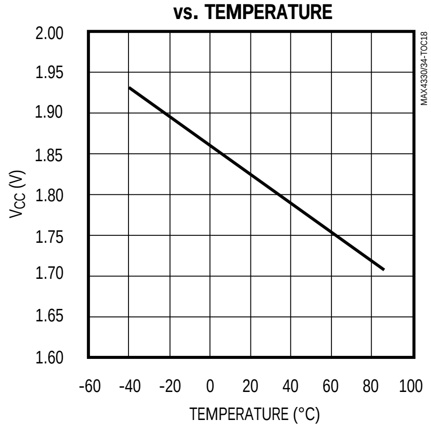
LARGE-SIGNAL GAIN vs. TEMPERATURE (R_L = 2kΩ)



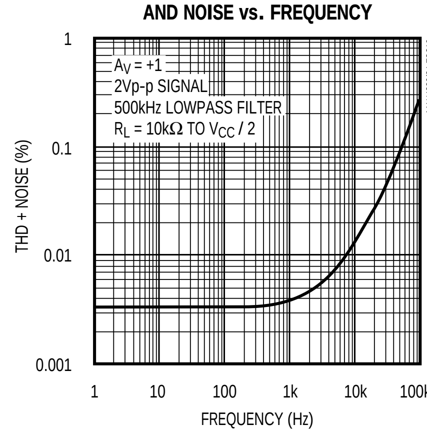
LARGE-SIGNAL GAIN vs. TEMPERATURE (R_L = 100kΩ)



MINIMUM OPERATING VOLTAGE vs. TEMPERATURE



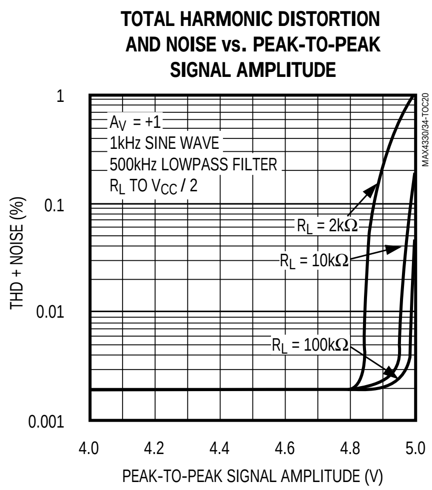
TOTAL HARMONIC DISTORTION AND NOISE vs. FREQUENCY

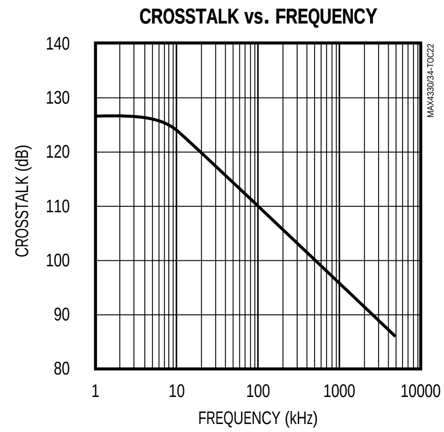


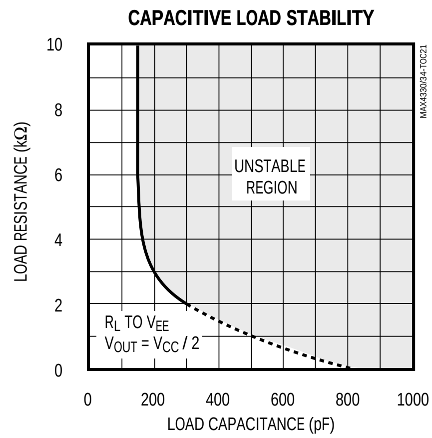
Single/Dual/Quad, Low-Power, Single-Supply, Rail-to-Rail I/O Op Amps with Shutdown

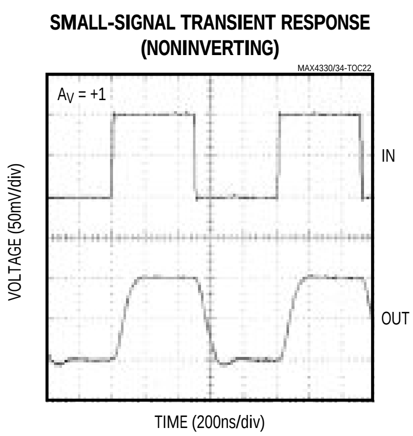
Typical Operating Characteristics (continued)

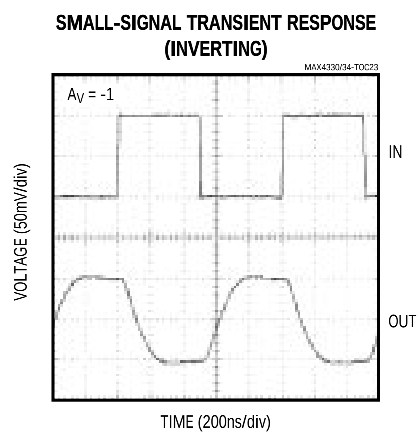
(V_{CC} = +5V, V_{EE} = 0V, V_{CM} = V_{CC} / 2, $V_{\overline{SHDN}}$ > 2V, T_A = +25°C, unless otherwise noted.)

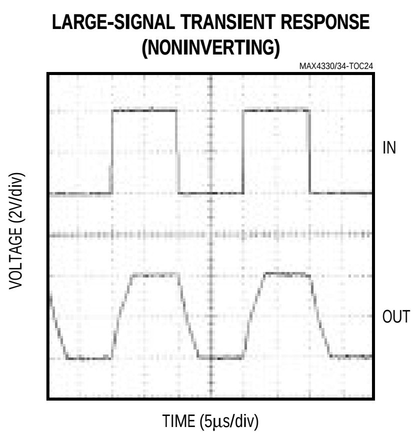


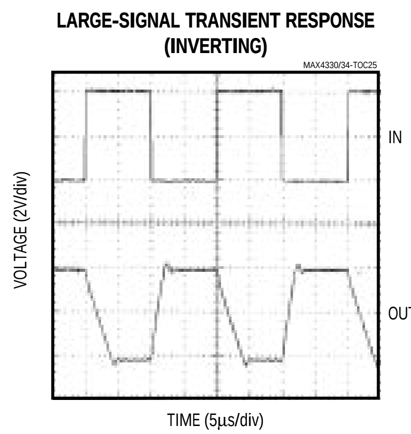












Pin Description

PIN						NAME	FUNCTION
MAX4330	MAX4331	MAX4332	MAX4333		MAX4334		
			10-Pin µMAX	14-Pin SO			
1	6	—	—	—	—	OUT	Output
2	4	4	4	4	11	V_{EE}	Negative Supply. Ground for single-supply operation.
3	3	—	—	—	—	IN+	Noninverting Input
4	2	—	—	—	—	IN-	Inverting Input
5	7	8	10	14	4	V_{CC}	Positive Supply
—	1, 5	—	—	5, 7, 8, 10	—	N.C.	No Connection. Not internally connected.
—	—	1, 7	1, 9	1, 13	1, 7	OUT1, OUT2	Outputs for Amplifiers 1 and 2
—	—	3, 5	3, 7	3, 11	3, 5	IN1+, IN2+	Noninverting Inputs to Amplifiers 1 and 2
—	—	2, 6	2, 8	2, 12	2, 6	IN1-, IN2-	Inverting Inputs to Amplifiers 1 and 2
—	8	—	—	—	—	$\overline{SHDN}$	Shutdown Input for Amplifier. Drive low for shutdown mode. Drive high or connect to V_{CC} for normal operation.
—	—	—	5, 6	6, 9	—	$\overline{SHDN1}$, $\overline{SHDN2}$	Shutdown for Amplifiers 1 and 2. Drive low for shutdown mode. Drive high or connect to V_{CC} for normal operation.
—	—	—	—	—	8, 14	OUT3, OUT4	Outputs for Amplifiers 3 and 4
—	—	—	—	—	9, 13	IN3-, IN4-	Inverting Inputs for Amplifiers 3 and 4
—	—	—	—	—	10, 12	IN3+, IN4+	Noninverting Inputs for Amplifiers 3 and 4

Detailed Description

Rail-to-Rail Input Stage

The MAX4330–MAX4334 have rail-to-rail input and output stages that are specifically designed for low-voltage, single-supply operation. The input stage consists of separate NPN and PNP differential stages, which operate together to provide a common-mode range extending to 0.25V beyond both supply rails. The crossover region, which occurs halfway between V_{CC} and V_{EE}, is extended to minimize degradation in CMRR caused by mismatched input pairs. The input offset voltage is typically 250µV. Low offset voltage, high bandwidth, rail-to-rail common-mode input range, and rail-to-rail outputs make this family of op amps an excellent choice for precision, low-voltage data-acquisition systems.

Since the input stage consists of NPN and PNP pairs, the input bias current changes polarity as the input voltage passes through the crossover region. Match the effective impedance seen by each input to reduce the offset error due to input bias currents flowing through external source impedances (Figures 1a and 1b). The combination of high source impedance with input capacitance (amplifier input capacitance plus stray capacitance) creates a parasitic pole that produces an underdamped signal response. Reducing input capacitance or placing a small capacitor across the feedback resistor improves response.

The MAX4330–MAX4334's inputs are protected from large differential input voltages by internal 1kΩ series resistors and back-to-back triple diode stacks across the inputs (Figure 2). For differential input voltages (much less than 1.8V), input resistance is typically 2.3MΩ. For differential input voltages greater than 1.8V, input resistance is around 2kΩ, and the input bias current can be approximated by the following equation:

$$I_{BIAS} = (V_{DIFF} - 1.8V) / 2k\Omega$$

In the region where the differential input voltage approaches 1.8V, input resistance decreases exponentially from 2.3MΩ to 2kΩ as the diode block begins conducting. Inversely, the bias current increases with the same curve.

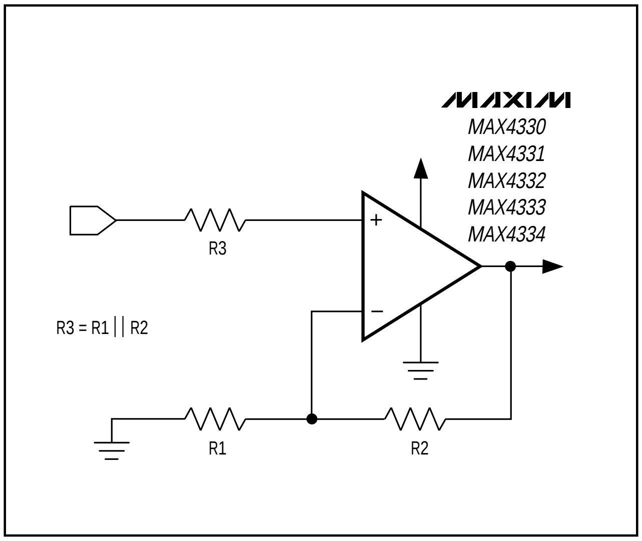


Figure 1a. Reducing Offset Error Due to Bias Current (Noninverting)

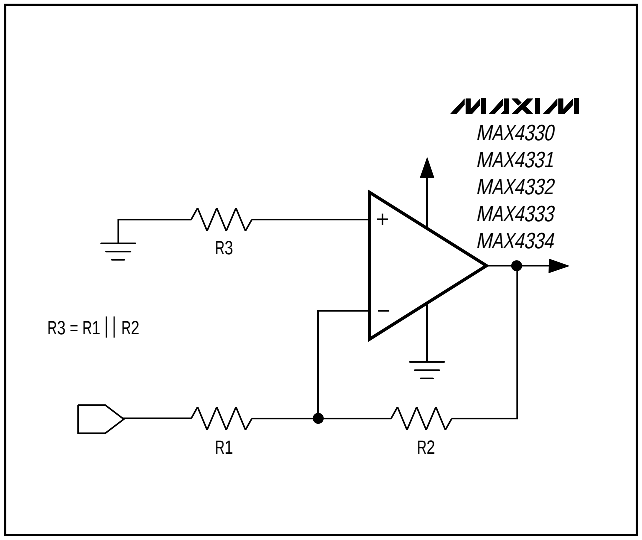


Figure 1b. Reducing Offset Error Due to Bias Current (Inverting)

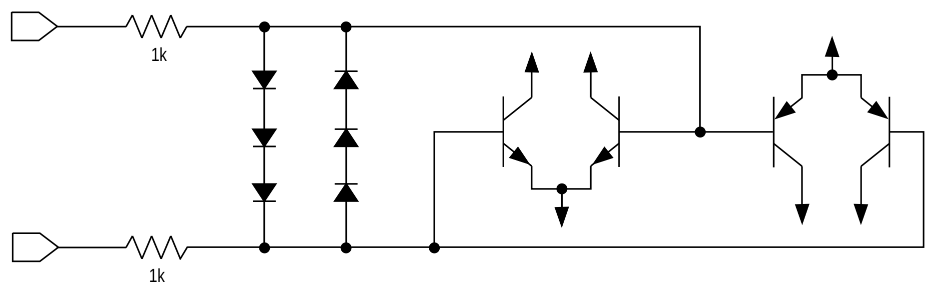


Figure 2. Input Protection Circuit

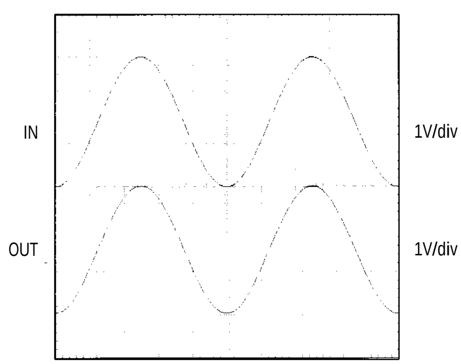


Figure 3. Rail-to-Rail Input/Output Voltage Range

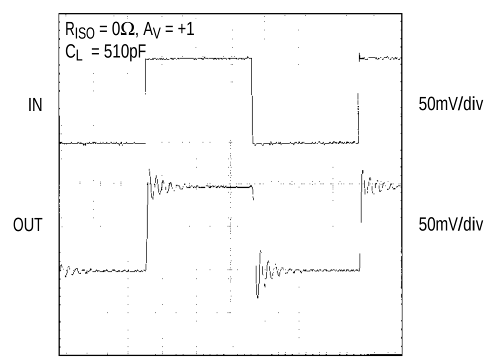


Figure 4. Small-Signal Transient Response with Excessive Capacitive Load

Rail-to-Rail Output Stage

The MAX4330–MAX4334 output stage can drive up to a 2kΩ load and still typically swing within 125mV of the rails. Figure 3 shows the output voltage swing of a MAX4331 configured as a unity-gain buffer. The operating voltage is a single +3V supply, and the input voltage is 3Vp-p. The output swings to within 70mV of V_{EE} and 100mV of V_{CC}, even with the maximum load applied (2kΩ to mid-supply).

Driving a capacitive load can cause instability in many op amps, especially those with low quiescent current. The MAX4330–MAX4334 are stable for capacitive loads up to 150pF. The Capacitive Load Stability graph in the *Typical Operating Characteristics* gives the stable operating region for capacitive vs. resistive loads. Figures 4 and 5 show the response of the MAX4331 with an excessive capacitive load, compared with the response when a series resistor is added between the output and the capacitive load. The resistor improves the circuit's response by isolating the load capacitance from the op amp's output (Figure 6).

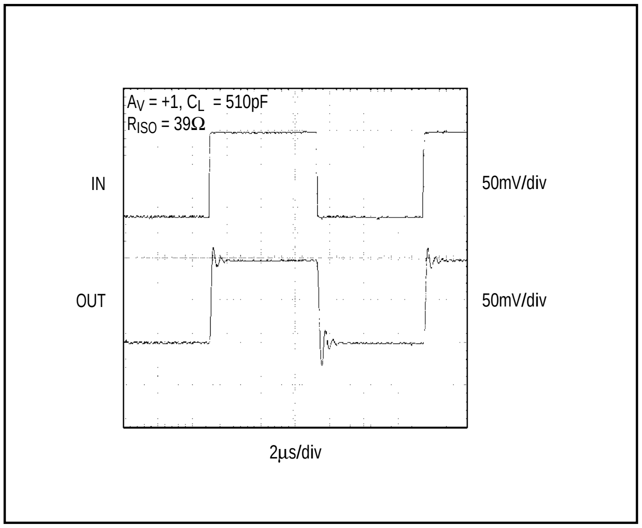


Figure 5. Small-Signal Transient Response with Excessive Capacitive Load and Isolation Resistor

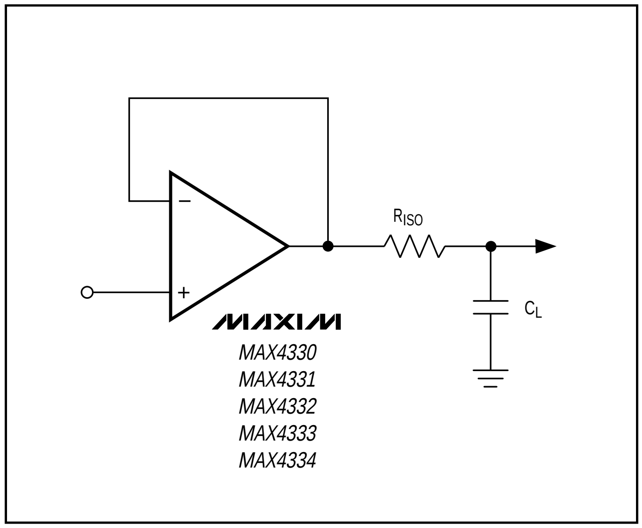


Figure 6. Capacitive-Load-Driving Circuit

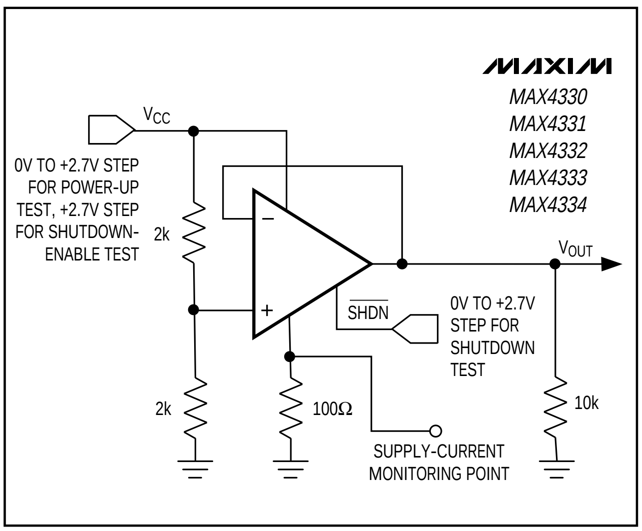


Figure 7. Power-Up/Shutdown Test Circuit

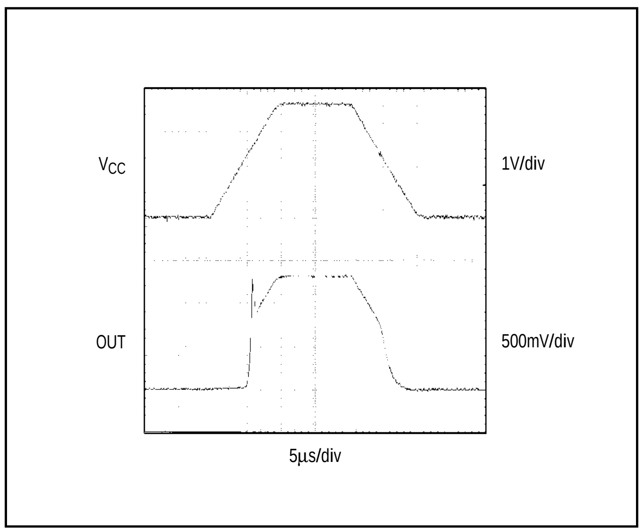


Figure 8. Power-Up/Down Output Voltage

Applications Information

Power-Up

The MAX4330–MAX4334 outputs typically settle within 5µs after power-up. Using the test circuit of Figure 7, Figures 8 and 9 show the output voltage and supply current on power-up and power-down.

Shutdown Mode

The MAX4331/MAX4333 feature a low-power shutdown mode. When the shutdown pin ($\overline{SHDN}$) is pulled low, the supply current drops to 9µA per amplifier (typical), the amplifier is disabled, and the outputs enter a high-impedance state. Pulling $\overline{SHDN}$ high or leaving it floating enables the amplifier. Figures 10 and 11 show the MAX4331/MAX4333's output voltage and supply-current responses to a shutdown pulse.

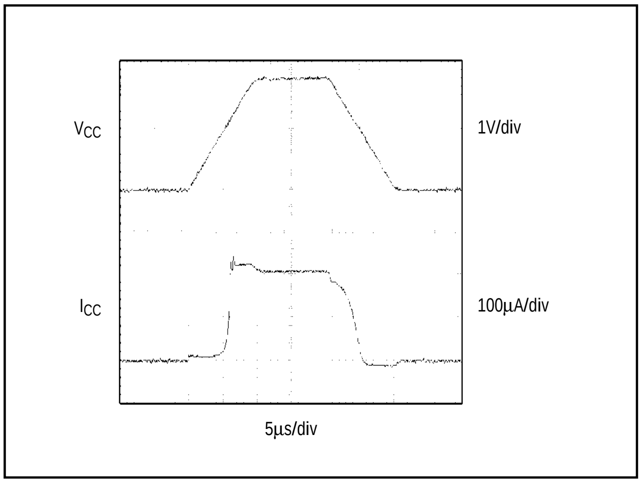


Figure 9. Power-Up/Down Supply Current

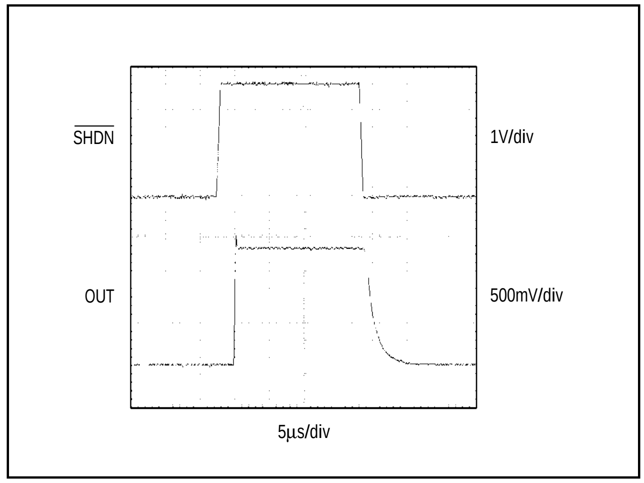


Figure 10. Shutdown Output Voltage Enable/Disable

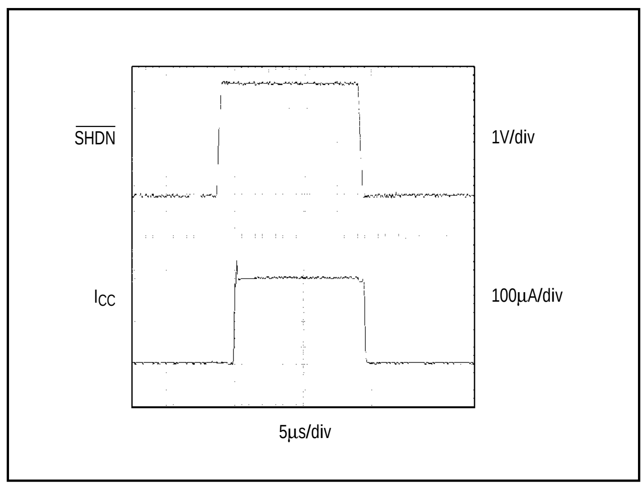


Figure 11. Shutdown Enable/Disable Supply Current

Do not three-state $\overline{SHDN}$. Due to the output leakage currents of three-state devices and the small internal pull-up current for $\overline{SHDN}$, three-stating this pin could result in indeterminate logic levels, and could adversely affect op-amp operation.

The logic threshold for $\overline{SHDN}$ is always referred to V_{EE}, **not** GND. When using dual supplies, pull $\overline{SHDN}$ to V_{EE} to place the op amp in shutdown mode.

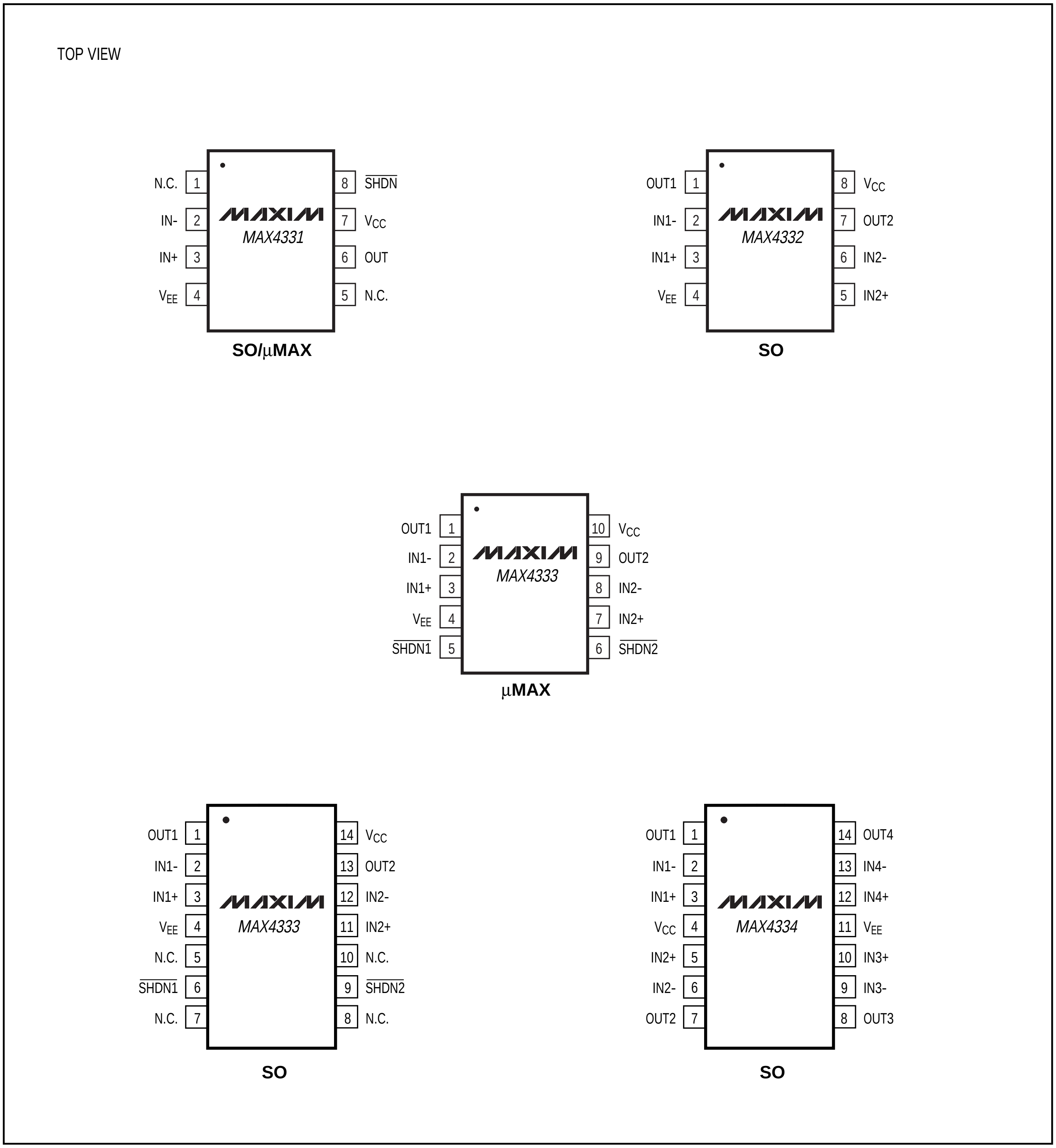
Power Supplies and Layout

The MAX4330–MAX4334 operate from a single +2.3V to +6.5V power supply, or from dual ±1.15V to ±3.25V supplies. For single-supply operation, bypass the power supply with a 0.1µF capacitor to ground (V_{EE}). For dual supplies, bypass both V_{CC} and V_{EE} with their own set of capacitors to ground.

Good layout technique helps optimize performance by decreasing the amount of stray capacitance at the op amp's inputs and outputs. To decrease stray capacitance, minimize trace lengths by placing external components close to the op amp's pins.

Single/Dual/Quad, Low-Power, Single-Supply, Rail-to-Rail I/O Op Amps with Shutdown

Pin Configurations (continued)



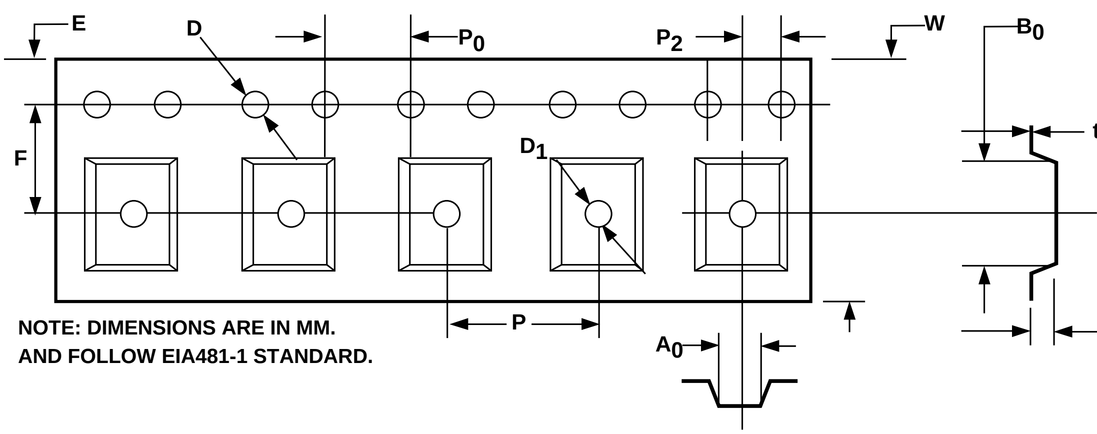
Chip Information

MAX4330/MAX4331
TRANSISTOR COUNT: 199
SUBSTRATE CONNECTED TO V_{EE}

MAX4332/MAX4333
TRANSISTOR COUNT: 398
SUBSTRATE CONNECTED TO V_{EE}

MAX4334
TRANSISTOR COUNT: 796
SUBSTRATE CONNECTED TO V_{EE}

Tape-and-Reel Information



NOTE: DIMENSIONS ARE IN MM. AND FOLLOW EIA481-1 STANDARD.

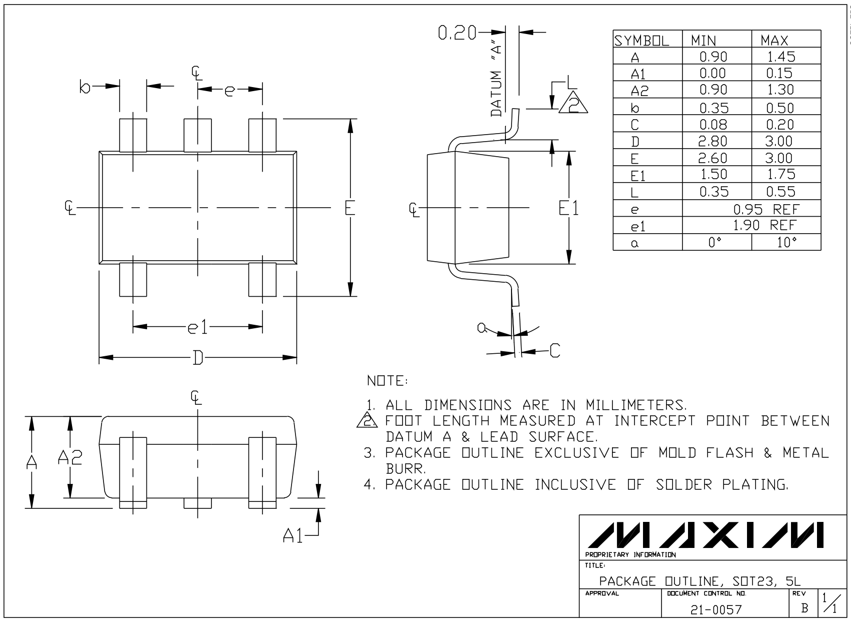
A_0	3.200	±0.102
B_0	3.099	±0.102
D	1.499	+0.102 +0.000
D_1	0.991	+0.254 +0.000

E	1.753	±0.102
F	3.505	±0.051
K_0	1.397	±0.102
P	3.988	±0.102

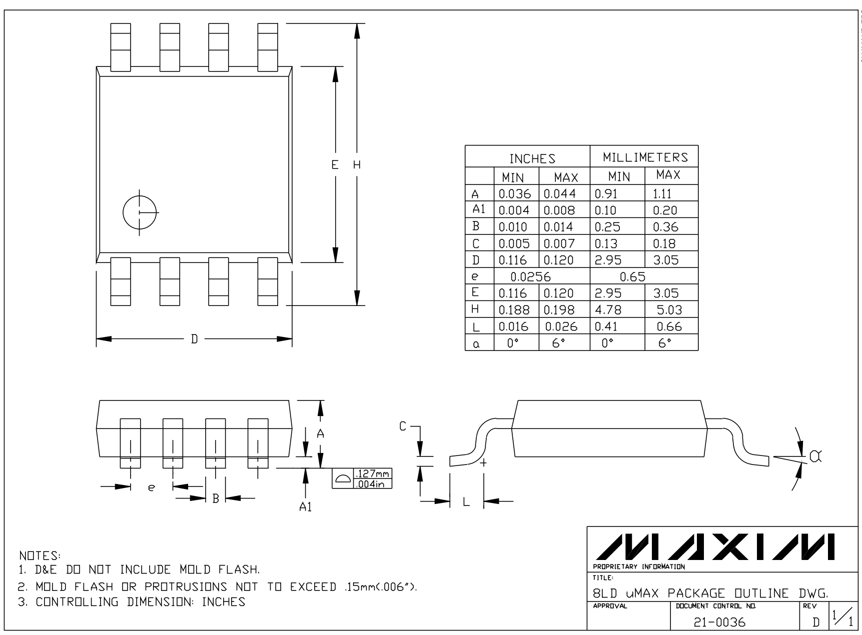
P_0	3.988	±0.102
$P_0$10	40.005	±0.203
P_2	2.007	±0.051
t	0.254	±0.127
W	8.001	+0.305 -0.102

5 SOT23-5

Package Information



SYMBOL	MIN	MAX
A	0.90	1.45
A1	0.00	0.15
A2	0.90	1.30
b	0.35	0.50
C	0.08	0.20
D	2.80	3.00
E	2.60	3.00
E1	1.50	1.75
L	0.35	0.55
e	0.95 REF	
e1	1.90 REF	
α	0°	10°



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.036	0.044	0.91	1.11
A1	0.004	0.008	0.10	0.20
B	0.010	0.014	0.25	0.36
C	0.005	0.007	0.13	0.18
D	0.116	0.120	2.95	3.05
e	0.0256		0.65	
E	0.116	0.120	2.95	3.05
H	0.188	0.198	4.78	5.03
L	0.016	0.026	0.41	0.66
α	0°	6°	0°	6°