INTEGRATED CIRCUITS

DATA SHEET

74F640

Octal bus transceiver, inverting (3-State)

Product specification

1989 Nov 27

IC15 Data Handbook





Octal bus transceiver, inverting (3-State)

74F640

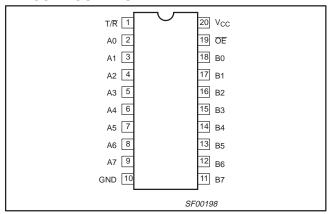
FEATURES

- High-impedance NPN base inputs for reduced loading (70μA in High and Low states)
- Ideal for applications which require high-output drive and minimal bus loading
- Inverting version of 74F245
- Octal bidirectional bus interface
- 3-State outputs sink 64mA and source 15mA

DESCRIPTION

The 74F640 is an octal transceiver featuring inverting 3-State bus compatible outputs in both transmit and receive directions. The B port outputs are capable of sinking 64mA and sourcing 15mA, providing very good capacitive drive characteristics. The device features an Output Enable ($\overline{\text{OE}}$) input for easy cascading and Transmit/Receiver ($\overline{\text{T/R}}$) input for direction control. The 3-State outputs, B0–B7, have been designed to prevent output bus loading if the power is removed from the device.

PIN CONFIGURATION



TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)					
74F640	3.5ns	78mA					

ORDERING INFORMATION

DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V $\pm 10\%$, T_{amb} = 0°C to +70°C	PKG DWG #		
20-pin plastic DIP	N74F640N	SOT146-1		
20-pin plastic SOL	N74F640D	SOT163-1		

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

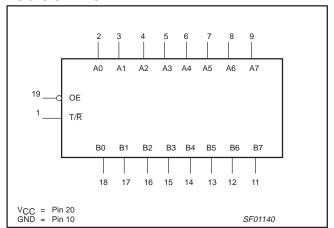
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A0 - A7, B0 - B7	Data inputs	3.5/0.115	70μΑ/70μΑ
ŌĒ	Output Enable input (active Low)	2.0/0.067	40μΑ/40μΑ
T/R	Transmit/Receive input	2.0/0.067	40μΑ/40μΑ
A0 - A7	A port outputs	150/40	3.0mA/24mA
B0 - B7	B port outputs	750/106.7	15mA/64mA

NOTE: One (1.0) FAST unit load is defined as: $20\mu A$ in the High state and 0.6mA in the Low state.

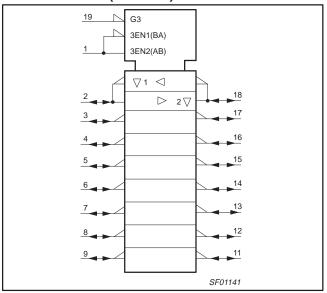
Octal bus transceiver, inverting (3-State)

74F640

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



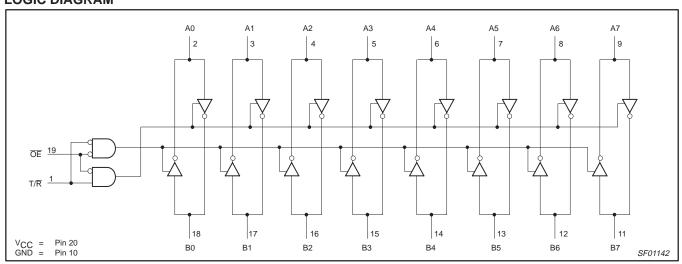
FUNCTION TABLE

INP	JTS	OUTPUTS
ŌĒ	T/R	0017013
L	L	Bus B data to Bus A
L	Н	Bus A data to Bus B
Н	X	z

High voltage level Low voltage level Н

X = Don't care Z = High impedance "off" state

LOGIC DIAGRAM



Octal bus transceiver, inverting (3-State)

74F640

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT	
V _{CC}	Supply voltage	upply voltage			
V _{IN}	Input voltage	-0.5 to +7.0	V		
I _{IN}	Input current		-30 to +5	mA	
V _{OUT}	Voltage applied to output in High output state		–0.5 to +V _{CC}	V	
	Command applied to sustaint in Lancautaut atom	A0-A7	48	mA	
lout	Current applied to output in Low output state	B0-B7	128	mA	
T _{amb}	Operating free-air temperature range	0 to +70	°C		
T _{stg}	Storage temperature range		-65 to +150	°C	

RECOMMENDED OPERATING CONDITIONS

OVMDOL	DADAA		LIMITS				
SYMBOL	PARAM	METER	MIN	NOM	MAX	UNIT	
V _{CC}	Supply voltage		4.5	5.0	5.5	V	
V _{IH}	High-level input voltage		2.0			V	
V _{IL}	Low-level input voltage			0.8	V		
I _{IK}	Input clamp current				-18	mA	
	High level even avenue	A0-A7			-3	mA	
IOH	High-level output current	B0-B7			-15	mA	
	l and land and and an extended	A0-A7			24	mA	
I _{OL}	Low-level output current	B0-B7			64	mA	
T _{amb}	Operating free-air temperature range	0		70	°C		

Octal bus transceiver, inverting (3-State)

74F640

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

				LIMITS					
SYMBOL	PARAMETER		TES1	TEST CONDITIONS ^{NO TAG}				MAX	UNIT
		A0-A7			±10%V _{CC}	2.4			V
M	Link lavel autout valtage	B0-B7	$V_{CC} = MIN,$ $V_{IL} = MAX,$	$I_{OH} = -3mA$	±5%V _{CC}	2.7	3.3		V
V _{OH}	High-level output voltage	B0-B7	$V_{IH} = MIN$	J 15mA	±10%V _{CC}	2.0			V
		BU-B7		$I_{OH} = -15 \text{mA}$	±5%V _{CC}	2.0			V
		A0-A7		I _{OL} = 24mA	±10%V _{CC}		0.35	0.50	V
V	Low lovel output voltage	AU-A7	$V_{CC} = MIN,$ $V_{IL} = MAX,$		±5%V _{CC}		0.35	0.50	V
V_{OL}	Low-level output voltage	B0-B7	$V_{IH} = MIN$		±10%V _{CC}			0.55	V
		B0-B7		IOL = IVIAX	±5%V _{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage	_	$V_{CC} = MIN, I_I$	= I _{IK}			-0.73	-1.2	V
l ₁	Input current at maximum	ŌĒ, T/R	V _{CC} = 0.0V, V	_I = 7.0V				100	μА
η	input voltage	A0–A7, B0–B7	V _{CC} = 5.5V, V _I = 5.5V					1.0	mA
I _{IH}	High-level input current	ŌĒ, T/R	V _{CC} = MAX, V	′ _I = 2.7V				40	μΑ
I _{IL}	Low-level input current	only	V _{CC} = MAX, V	′ _I = 0.5V				-40	μА
I _{OZH} +I _{IH}	Off-state output current, High level of voltage applied	•	V _{CC} = MAX, V	′ _I = 2.7V				70	μА
I _{OZL} +I _{IL}	Off-state output current, Low level of voltage applied		V _{CC} = MAX, V	' _I = 0.5V				-70	μΑ
	Short-circuit output cur-	A0-A7	V MAY	, , , , , , , , , , , , , , , , , , , ,		-60		-150	mA
los	rent ^{NO TAG}	B0–B7 V _{CC} = MAX			-100		-225	μΑ	
		I _{CCH}	$T/\overline{R} = An = 4.5V,$ $\overline{OE} = GND$			66	85	mA	
I _{CC}	Supply current (total)	I _{CCL}	$V_{CC} = MAX$	$V_{CC} = MAX$ $T/\overline{R} = Bn = \overline{OE} = GND$			91	120	mA
		I _{CCZ}		$T/\overline{R} = Bn = GND,$ $\overline{OE} = 4.5V$			78	102	mA

^{1.} For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.

All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
 Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Octal bus transceiver, inverting (3-State)

74F640

AC ELECTRICAL CHARACTERISTICS

					LIM	ITS		
SYMBOL	PARAMETER	TEST CONDITION	$V_{CC} = +5V$ $T_{amb} = +25^{\circ}C$ $C_{L} = 50pF, R_{L} = 500\Omega$			V _{CC} = +5 T _{amb} = 0°C C _L = 50pF,	UNIT	
			MIN	TYP	MAX	MIN	MAX	
t _{PLH} t _{PHL}	Propagation delay An to Bn, Bn to An	Waveform NO TAG	2.0 1.0	4.5 2.5	7.0 5.0	2.0 1.0	8.0 5.5	ns
t _{PZH} t _{PZL}	Output Enable time to High or Low level	Waveform 3 Waveform 2	5.5 5.5	6.5 7.0	10.5 10.5	5.0 5.0	12.0 11.0	ns
t _{PHZ}	Output Disable time from High or Low level	Waveform 3 Waveform 2	2.0 2.0	3.5 4.5	6.5 7.0	1.5 2.0	8.0 7.5	ns

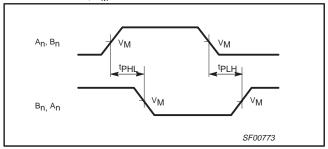
1989 Nov 27 6

Octal bus transceiver, inverting (3-State)

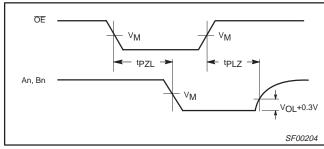
74F640

AC WAVEFORMS

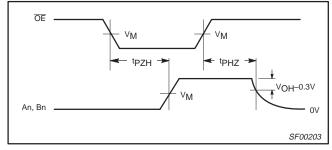
For all waveforms, $V_M = 1.5V$.



Waveform 1. Propagation Delay for Inverting Outputs

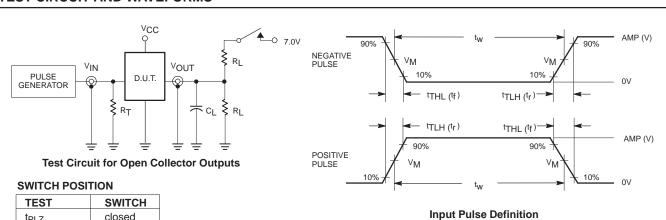


Waveform 2. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level



Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level

TEST CIRCUIT AND WAVEFORMS



TEST	SWITCH
t _{PLZ}	closed
t _{PZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor;

see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

fa!!	INP	UT PU	LSE REQU	REMEN	TS	
family	amplitude	V _M rep. rate		t _w	t _{TLH}	t _{THL}
74F 3.0V		1.5V	1MHz	500ns	2.5ns	2.5ns

SF00128

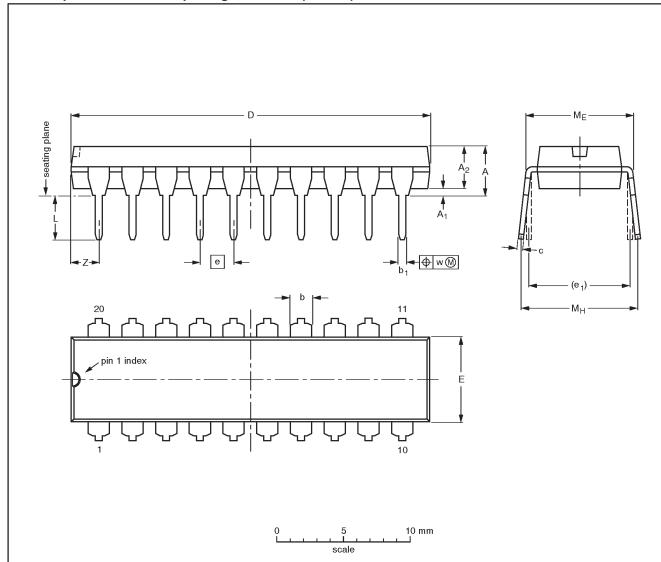
1989 Nov 27 7

Octal bus transceiver, inverting (3-State)

74F640

DIP20: plastic dual in-line package; 20 leads (300 mil)

SOT146-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	С	D ⁽¹⁾	E ⁽¹⁾	е	e ₁	L	ME	Мн	w	Z ⁽¹⁾ max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

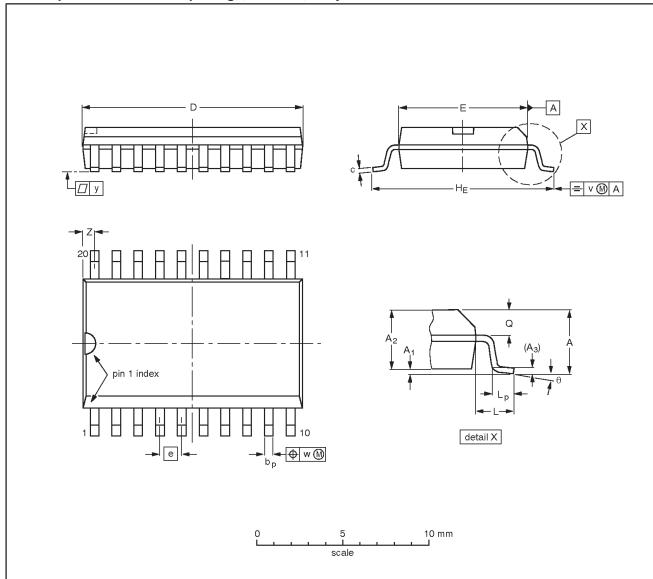
OUTLINE		REFER	RENCES	EUROPEAN	ISSUE DATE			
	VERSION	IEC	IEC JEDEC EIAJ				ISSUE DATE	
	SOT146-1			SC603			92-11-17 95-05-24	

Octal bus transceiver, inverting (3-State)

74F640

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	bр	С	D ⁽¹⁾	E ⁽¹⁾	е	HE	L	Lp	Q	v	w	у	z ⁽¹⁾	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016		0.01	0.01	0.004	0.035 0.016	0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE		REFER	EUROPEAN	ISSUE DATE		
VERSION	IEC	JEDEC	EIAJ		PROJECTION	ISSUE DATE
SOT163-1	075E04	MS-013AC				-95-01-24 97-05-22

Octal bus transceiver, inverting (3-State)

74F640

NOTES

1989 Nov 27 10

Octal bus transceiver, inverting (3-State)

74F640

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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