DATA SHEET

~~74F655A*~~
~~Octal buffer/driver with parity, inverting (3-State)~~
74F656A
Octal buffer/driver with parity, non-inverting (3-State)

** Discontinued part. Please see the Discontinued Product List.*

Product specification

1991 Jul 17

IC15 Data Handbook

Philips Semiconductors

PHILIPS

Buffers/drivers

~~74F655A~~*
74F656A

74F655A Octal buffer/driver with parity, inverting (3-State)
74F656A Octal buffer/driver with parity, non-inverting (3-State)

FEATURES

- Significantly improved AC performance over 74F655 and 74F656
- High impedance NPN base input for reduced loading (40µA in High and Low states)
- Ideal in applications where high output drive and light bus loading are required (I_{IL} is 40µA vs. FAST std of 600µA)
- 74F655A combines 74F240 and 74F280A functions in one package
- 74F656A combines 74F244 and 74F280A functions in one package
- 74F655A Inverting
- 74F656A Non-inverting
- 3-State outputs sink 64mA and source 15mA
- 24-pin plastic Slim DIP (300mil) package
- Inputs on one side and outputs on the other side simplifies PC board layout
- Combined functions reduce part count and enhance system performance
- Industrial temperature range available (–40°C to +85°C)

DESCRIPTION

The 74F655A and 74F656A are octal buffers and line drivers with parity generation/checking designed to be employed as memory address drivers, clock drivers and bus-oriented transmitters/receivers. These parts include parity generator/checker to improve PC board density.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F655A	6.5ns	64mA
74F656A	6.5ns	64mA

ORDERING INFORMATION

DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	INDUSTRIAL RANGE V_{CC} = 5V ±10%, T_{amb} = –40°C to +85°C	PKG DWG #
24-pin Plastic Slim DIP (300mil)	N74F656AN	I74F656AN	SOT222-1
24-pin Plastic SOL	N74F656AD	I74F656AD	SOT137-1

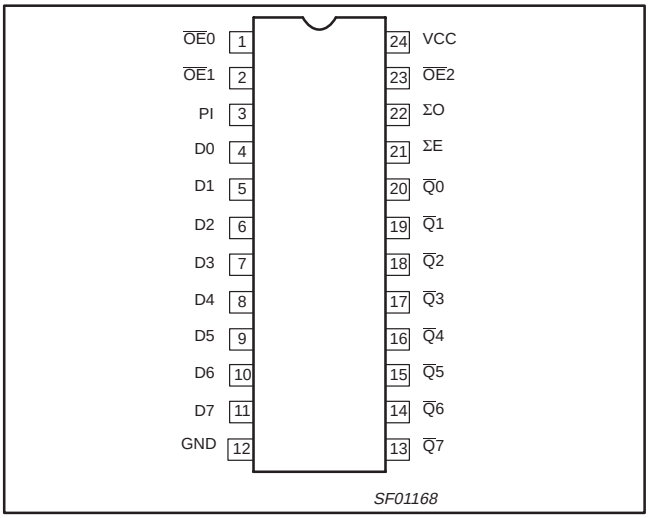
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0–D7	Data inputs	2.0/0.066	40µA/40µA
PI	Parity input	1.0/0.033	20µA/20µA
$\overline{OE}$0, $\overline{OE}$1, $\overline{OE}$2	Output Enable Inputs (active Low)	1.0/0.033	20µA/20µA
ΣE, ΣO	Parity outputs	750/106.7	15mA/64mA
$\overline{Q}$0–$\overline{Q}$7	Data outputs (74F655A)	750/106.7	15mA/64mA
Q0–Q7	Data outputs (74F656A)	750/106.7	15mA/64mA

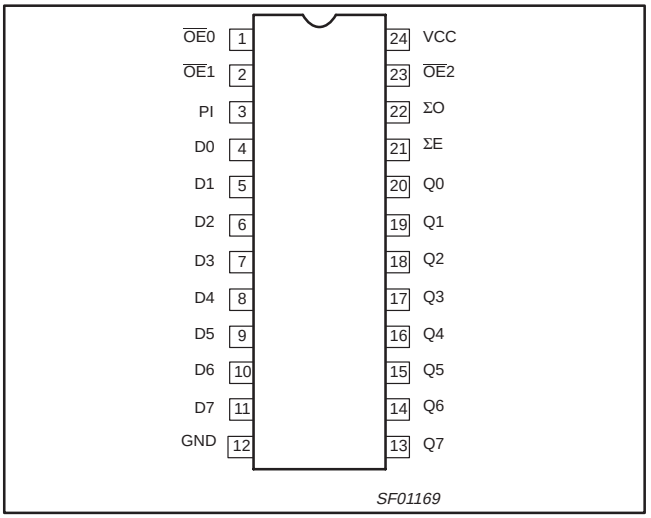
NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20µA in the High state and 0.6mA in the Low state.

** Discontinued part. Please see the Discontinued Products List.*

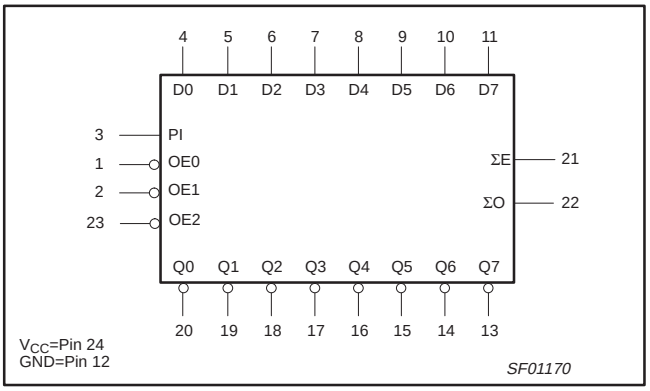
PIN CONFIGURATION – 74F655A



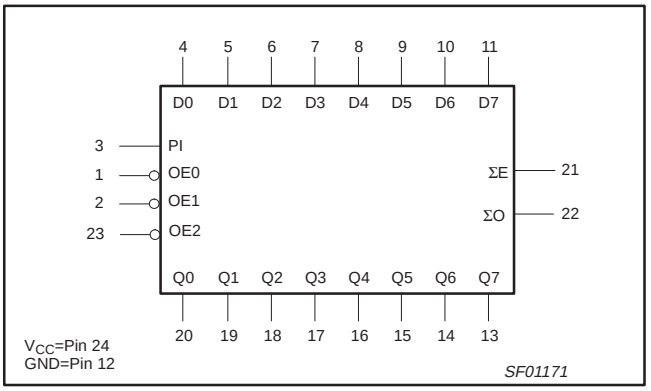
PIN CONFIGURATION – 74F656A



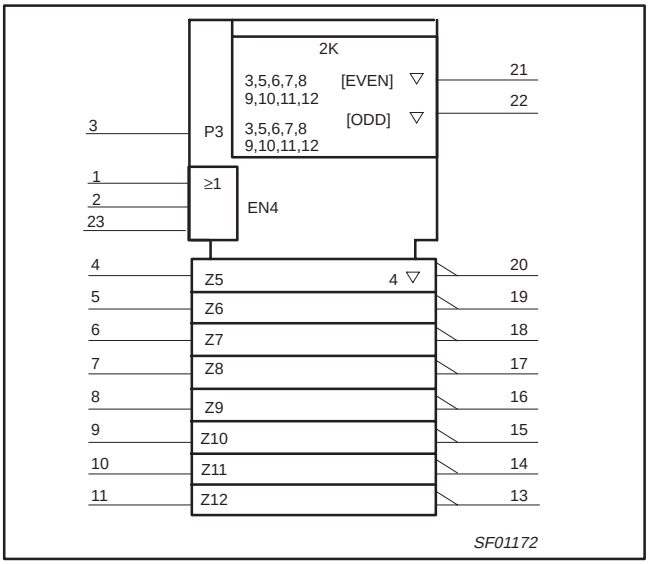
LOGIC SYMBOL – 74F655A



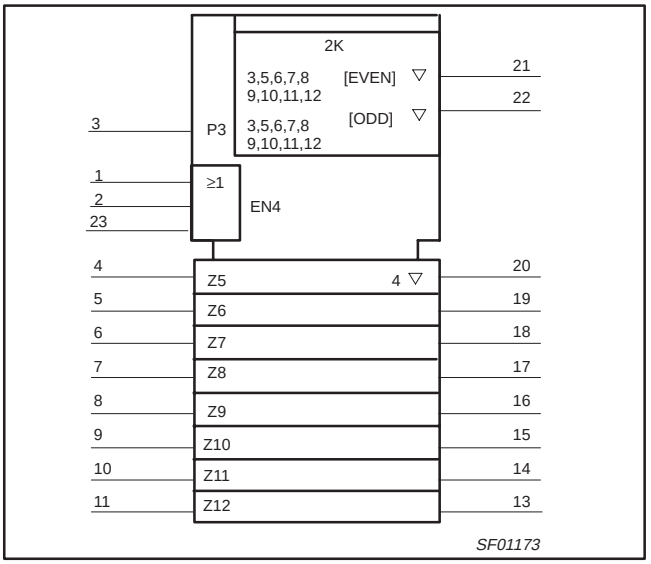
LOGIC SYMBOL – 74F656A



IEEE/IEC SYMBOL – 74F655A

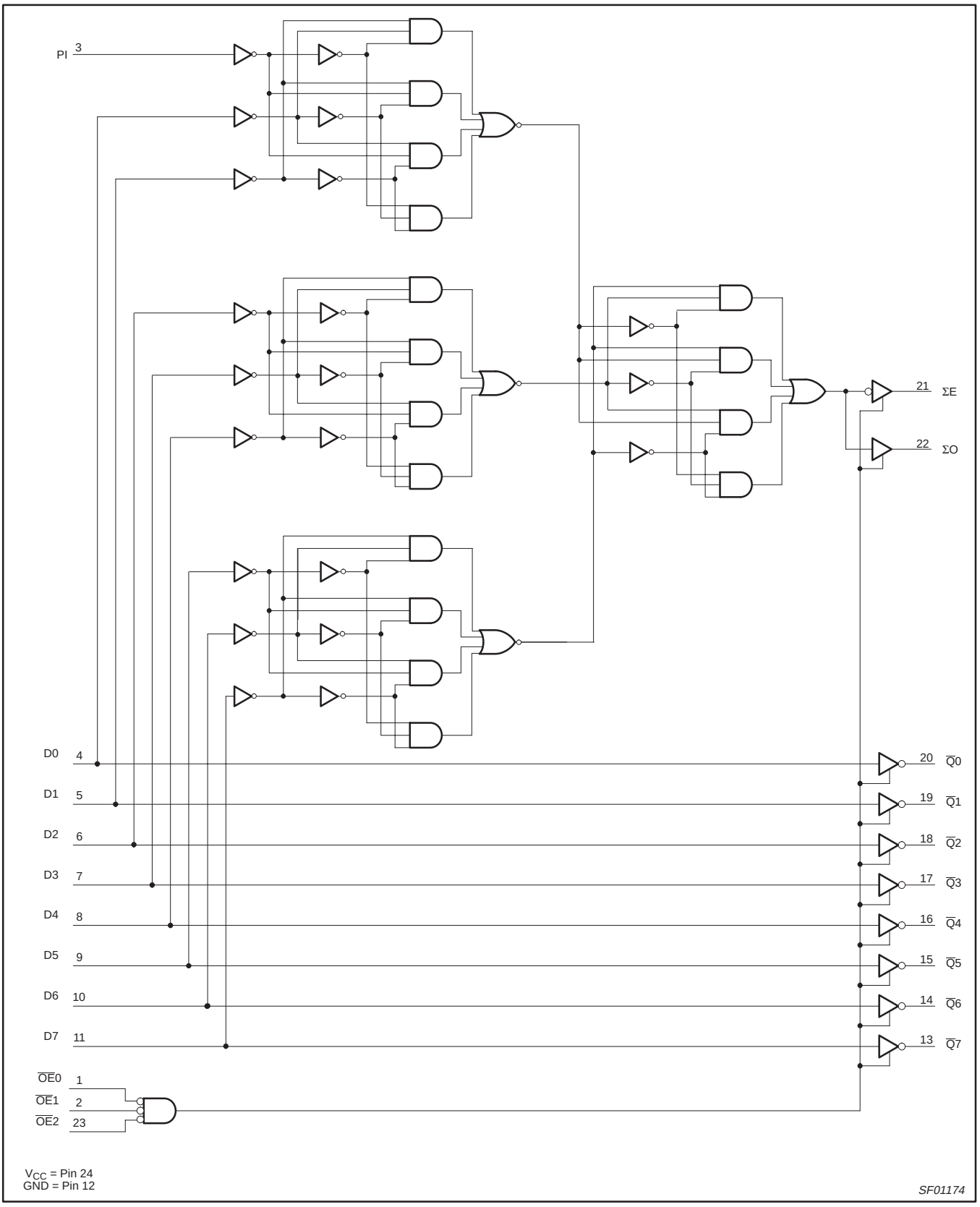


LOGIC SYMBOL (IEEE/IEC) – 74F656A



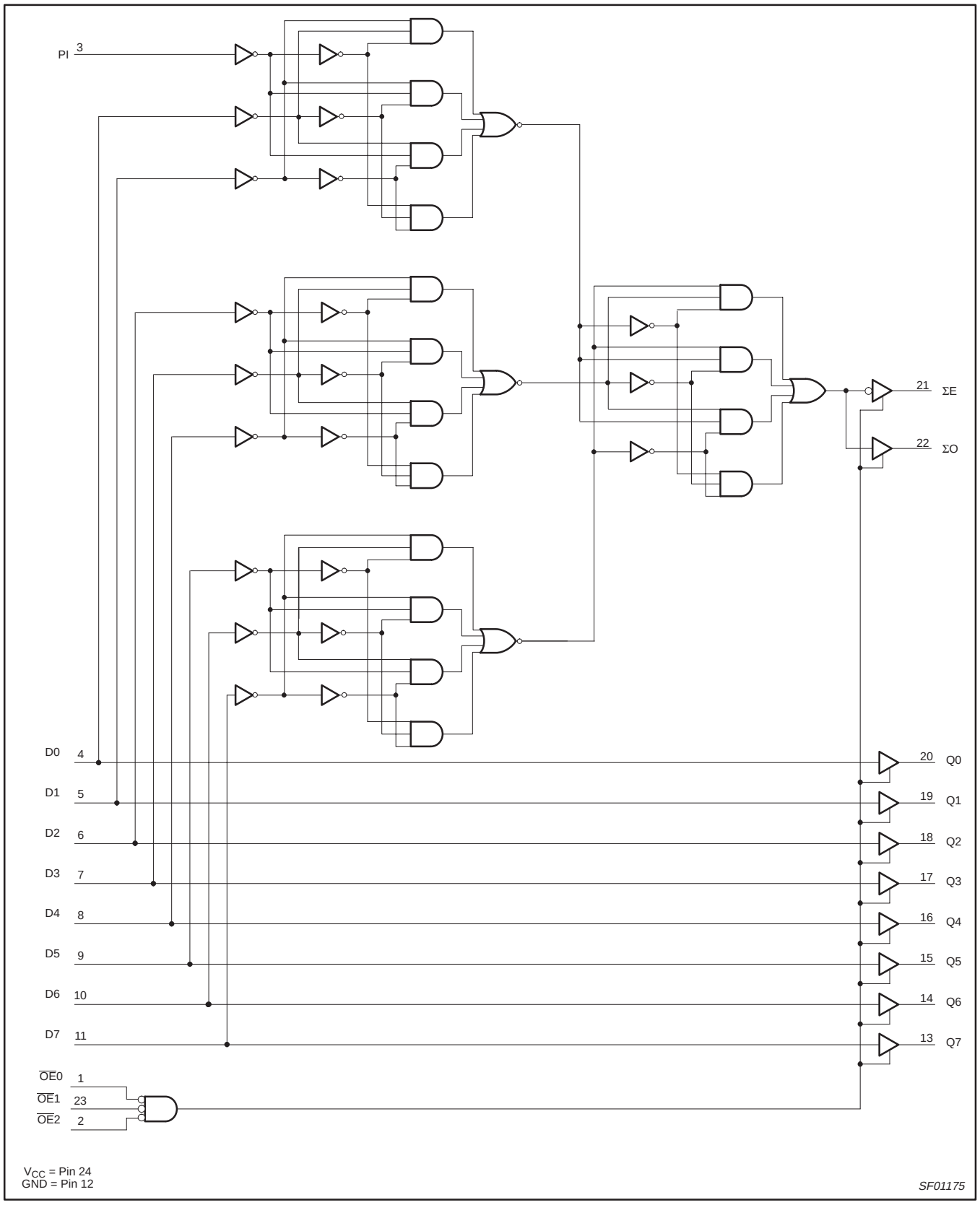
** Discontinued part. Please see the Discontinued Products List.*

LOGIC DIAGRAM – 74F655A



** Discontinued part. Please see the Discontinued Products List.*

LOGIC DIAGRAM – 74F656A



** Discontinued part. Please see the Discontinued Products List.*

FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{OE}0$	$\overline{OE}1$	$\overline{OE}2$	Dn	74F655A	74F656A
				$\overline{Q}n$	Qn
L	L	L	L	H	L
L	L	L	H	L	H
H	X	X	X	Z	Z
X	H	X	X	Z	Z
X	X	H	X	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

FUNCTION TABLE for PARITY OUTPUTS

INPUTS	PARITY OUTPUTS	
Number of inputs, High (PI, D0–D7)	ΣE	Σ0
Even - 0, 2, 4, 6, 8	H	L
Odd - 1, 3, 5, 7, 9	L	H
Any $\overline{OE}$n = High	Z	Z

H = High voltage level
L = Low voltage level
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IN}	Input voltage		–0.5 to +7.0	V
I_{IN}	Input current		–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		–0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state		128	mA
T_{amb}	Operating free-air temperature range	Commercial range	0 to +70	°C
		Industrial range	–40 to +85	°C
T_{stg}	Storage temperature range		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current				–15	mA
I_{OL}	Low-level output current				64	mA
T_{amb}	Operating free-air temperature range	Commercial range	0		70	°C
		Industrial range	–40		85	°C

** Discontinued part. Please see the Discontinued Products List.*

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[NO TAG]			LIMITS MIN	LIMITS TYP NO TAG	LIMITS MAX	UNIT
V_{OH}	High-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –3mA	±10%V_{CC}	2.4			V
						±5%V_{CC}	2.7	3.3		V
					I_{OH} = –15mA	±10%V_{CC}	2.0			V
V_{OL}	Low-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 64mA	±10%V_{CC}			0.55	V
						±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, I_I = I_{IK}				–0.73	–1.2	V
I_I	Input current at maximum input voltage			V_{CC} = 0.0, V_I = 7.0V					100	µA
I_{IH}	High-level input current	Commercial range	Dn	V_{CC} = MAX, V_I = 2.7V					40	µA
			PI, $\overline{OE}$n						20	µA
		Industrial range	Dn						80	µA
			PI, $\overline{OE}$n						40	µA
I_{IL}	Low-level input current		Dn	V_{CC} = MAX, V_I = 0.5V					–40	µA
			PI, $\overline{OE}$n						–20	µA
I_{OZH}	Off-state current High-level voltage applied			V_{CC} = MAX, V_O = 2.7V					50	µA
I_{OZL}	Off-state current Low-level voltage applied			V_{CC} = MAX, V_O = 0.5V					–50	µA
I_{OS}	Short-circuit output current[3]			V_{CC} = MAX			–100		–225	mA
I_{CC}	Supply current (total)		I_{CCH}	V_{CC} = MAX				50	80	mA
			I_{CCL}					78	110	mA
			I_{CCZ}					83	90	mA

NOTES:

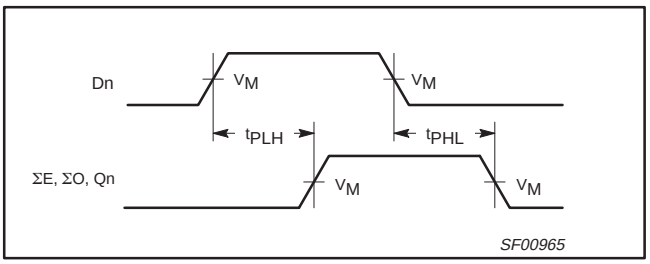
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

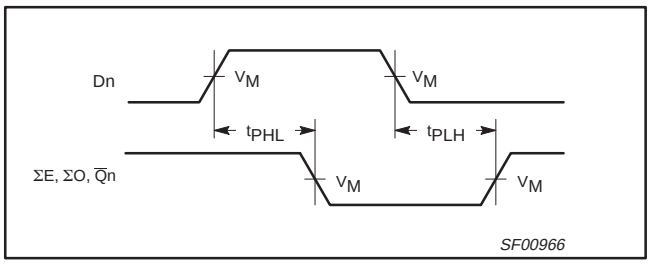
SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS: T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			LIMITS: T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		LIMITS: T_{amb} = –40°C to +85°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Dn to $\overline{Q}$n	74F655A	Waveform 2	2.0 1.0	4.5 2.5	6.5 4.0	2.0 1.0	7.5 4.5	2.0 1.0	8.5 5.5	ns ns
t_{PLH} t_{PHL}	Propagation delay Dn to Qn	74F656A	Waveform 1	2.0 2.5	4.0 5.5	6.5 7.0	2.0 2.5	7.0 7.5	2.0 2.5	8.0 9.0	ns ns
t_{PLH} t_{PHL}	Propagation delay Dn to ΣE, ΣO		Waveform 1, 2	5.5 5.5	10.0 11.0	13.0 14.5	5.5 5.5	14.0 16.5	4.5 5.5	16.5 18.0	ns ns
t_{PZH} t_{PZL}	Output enable time to High or Low level		Waveform 3 Waveform 4	3.5 4.0	7.0 8.0	10.5 11.0	3.5 4.5	11.5 12.0	3.0 4.0	13.0 13.5	ns ns
t_{PHZ} t_{PLZ}	Output disable time from High or Low level		Waveform 3 Waveform 4	1.5 2.0	4.5 5.0	8.0 8.0	1.5 2.0	9.0 9.0	1.5 1.5	10.0 10.0	ns ns

** Discontinued part. Please see the Discontinued Products List.*

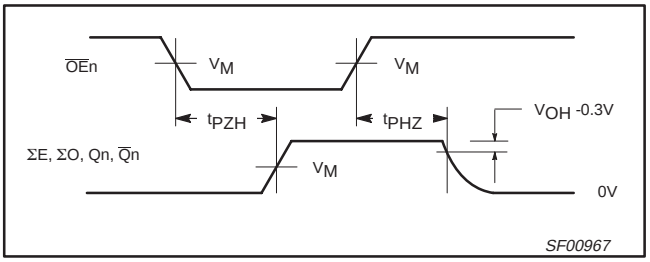
AC WAVEFORMS



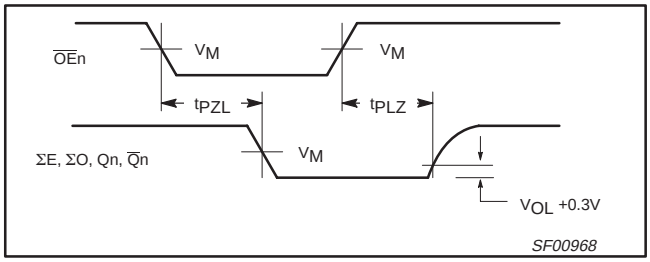
Waveform 1. Propagation Delay, Non-Inverting Outputs



Waveform 2. Propagation Delay, Inverting Outputs

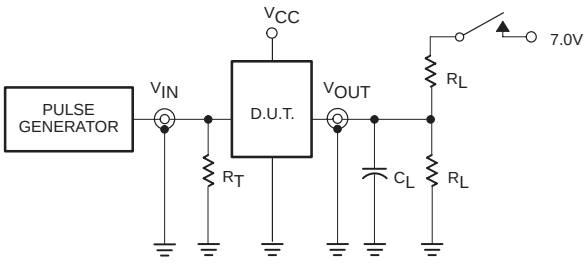


Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level

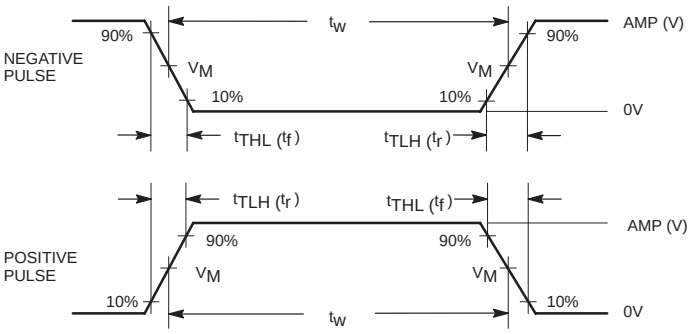


Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

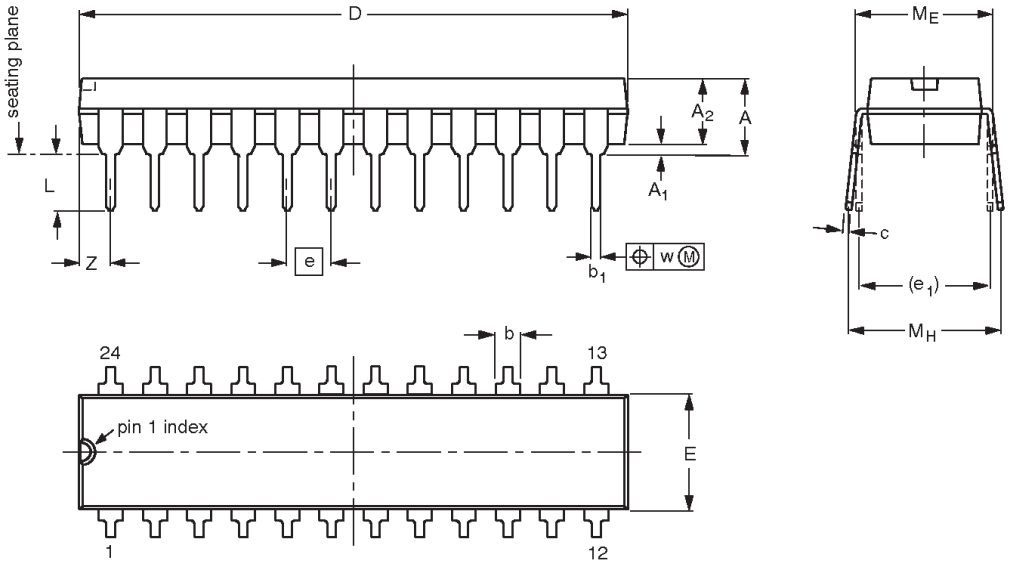
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

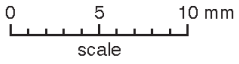
family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00777

* *Discontinued part. Please see the Discontinued Products List.*

DIP24: plastic dual in-line package; 24 leads (300 mil) **SOT222-1**





DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.70	0.38	3.94	1.63 1.14	0.56 0.43	0.36 0.25	31.9 31.5	6.73 6.48	2.54	7.62	3.51 3.05	8.13 7.62	10.03 7.62	0.25	2.05
inches	0.185	0.015	0.155	0.064 0.045	0.022 0.017	0.014 0.010	1.256 1.240	0.265 0.255	0.100	0.300	0.138 0.120	0.32 0.30	0.395 0.300	0.01	0.081

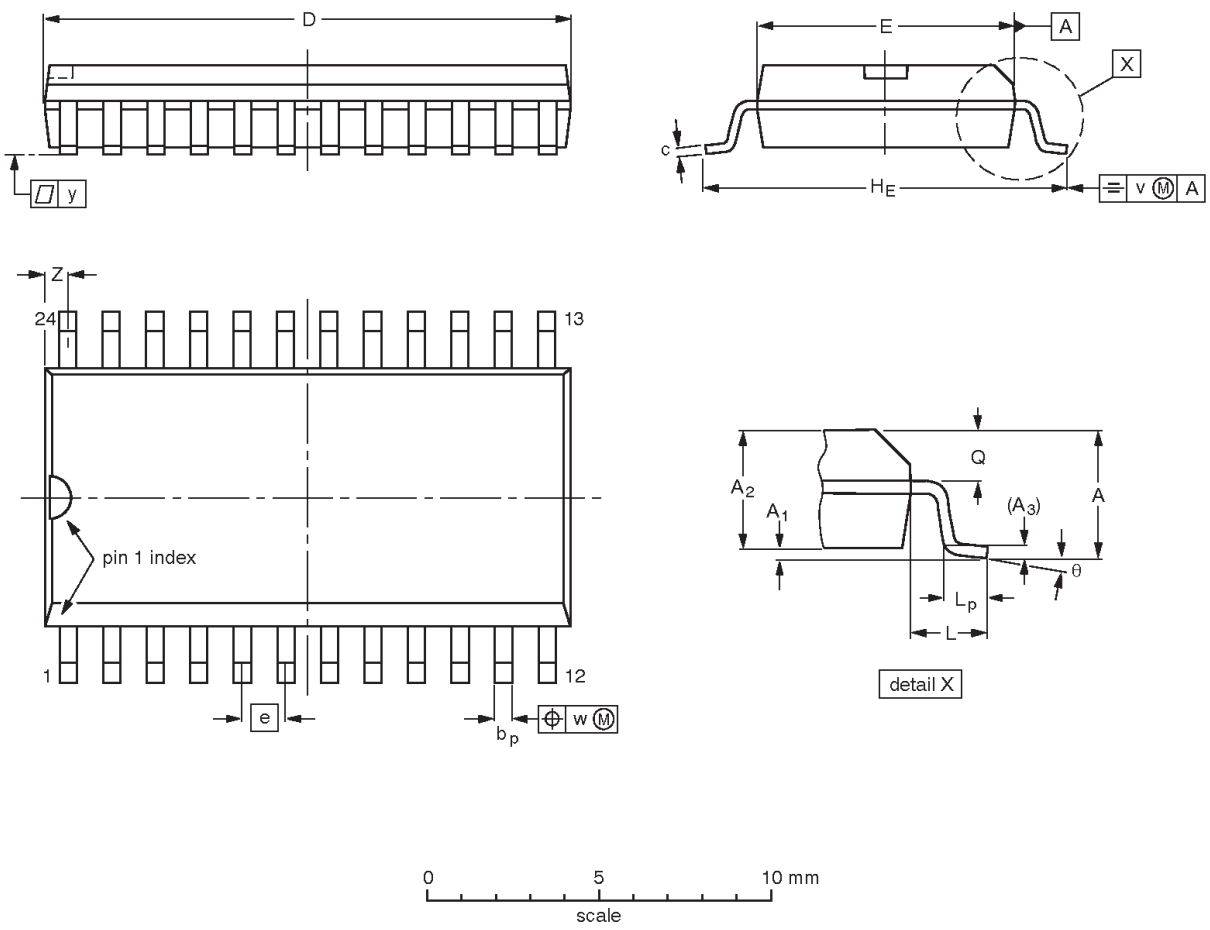
Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT222-1		MS-001AF				95-03-11

** Discontinued part. Please see the Discontinued Product List.*

SO24: plastic small outline package; 24 leads; body width 7.5 mm **SOT137-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT137-1	075E05	MS-013AD				~~95-01-24~~ 97-05-22

* *Discontinued part. Please see the Discontinued Product List.*

NOTES

** Discontinued part. Please see the Discontinued Product List.*

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make chages at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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print code Date of release: 10-98

Document order number: 9397-750-05169

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