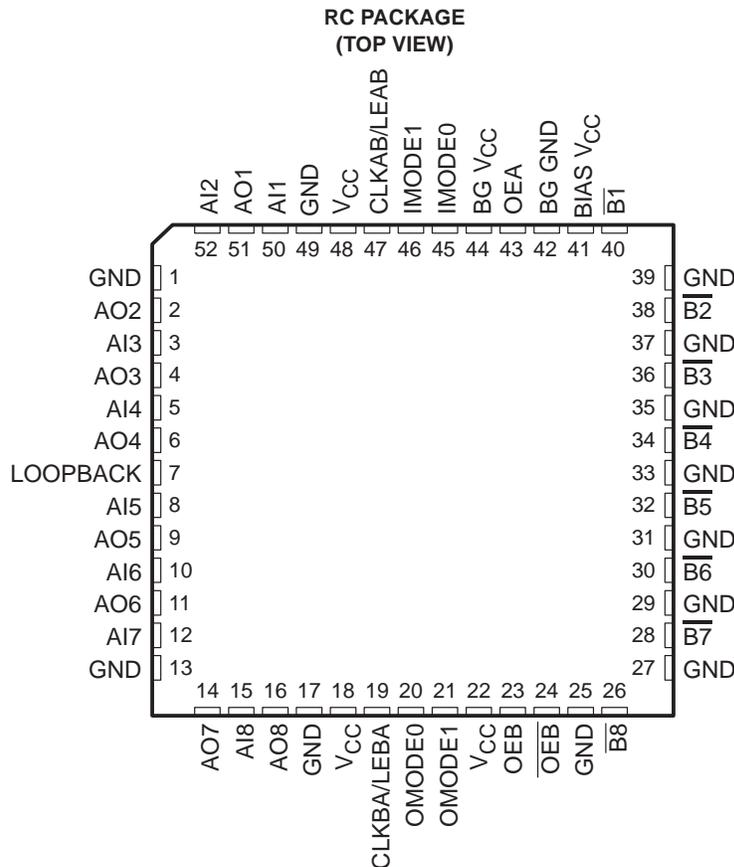


# SN74FB2033A 8-BIT TTL/BTL REGISTERED TRANSCEIVER

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- **Compatible With IEEE Std 1194.1-1991 (BTL)**
- **TTL A Port, Backplane Transceiver Logic (BTL)  $\bar{B}$  Port**
- **Open-Collector  $\bar{B}$ -Port Outputs Sink 100 mA**
- **Isolated Logic-Ground and Bus-Ground Pins Reduce Noise**
- **BIAS  $V_{CC}$  Pin Minimizes Signal Distortion During Live Insertion or Withdrawal**
- **High-Impedance State During Power Up and Power Down**
- **$\bar{B}$ -Port Biasing Network Preconditions the Connector and PC Trace to the BTL High-Level Voltage**
- **TTL-Input Structures Incorporate Active Clamping Networks to Aid in Line Termination**
- **Packaged in Plastic Quad Flatpack**



## description

The SN74FB2033A is an 8-bit transceiver featuring a split input (AI) and output (AO) bus on the TTL-level A port. The common-I/O, open-collector  $\bar{B}$  port operates at backplane transceiver logic (BTL) signal levels.

The logic element for data flow in each direction is configured by two mode inputs (IMODE1 and IMODE0 for B-to-A, OMODE1 and OMODE0 for A-to-B) as a buffer, a D-type flip-flop, or a D-type latch. When configured in the buffer mode, the inverted input data appears at the output port. In the flip-flop mode, data is stored on the rising edge of the appropriate clock input (CLKAB/LEAB or CLKBA/LEBA). In the latch mode, the clock inputs serve as active-high transparent latch enables.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

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### description (continued)

Data flow in the B-to-A direction, regardless of the logic element selected, is further controlled by the LOOPBACK input. When LOOPBACK is low,  $\overline{B}$ -port data is the B-to-A input. When LOOPBACK is high, the output of the selected A-to-B logic element (prior to inversion) is the B-to-A input.

The AO port-enable/-disable control is provided by OEA. When OEA is low or when  $V_{CC}$  is less than 2.5 V, the AO port is in the high-impedance state. When OEA is high, the AO port is active (high or low logic levels).

The  $\overline{B}$  port is controlled by OEB and  $\overline{OEB}$ . If OEB is low,  $\overline{OEB}$  is high, or  $V_{CC}$  is less than 2.5 V, the  $\overline{B}$  port is inactive. If OEB is high and  $\overline{OEB}$  is low, the  $\overline{B}$  port is active.

BG  $V_{CC}$  and BG GND are the bias-generator reference inputs.

The A-to-B and B-to-A logic elements are active, regardless of the state of their associated outputs. The logic elements can enter new data (in flip-flop and latch modes) or retain previously stored data while the associated outputs are in the high-impedance (AO port) or inactive ( $\overline{B}$  port) states.

Output clamps are provided on the BTL outputs to reduce switching noise. One clamp reduces inductive ringing effects on  $V_{OH}$  during a low-to-high transition. The other clamps out ringing below the BTL  $V_{OL}$  voltage of 0.75 V. Both clamps are active only during ac switching and do not affect the BTL outputs during steady-state conditions.

BIAS  $V_{CC}$  establishes a voltage between 1.62 V and 2.1 V on the BTL outputs when  $V_{CC}$  is not connected.

The SN74FB2033A is characterized for operation from 0°C to 70°C.

### Function Tables

FUNCTION/MODE								FUNCTION/MODE
INPUTS								
OEA	OEB	$\overline{OEB}$	OMODE1	OMODE0	IMODE1	IMODE0	LOOPBACK	
L	L	X	X	X	X	X	X	Isolation
L	X	H	X	X	X	X	X	
X	H	L	L	L	X	X	X	AI to $\overline{B}$ , buffer mode
X	H	L	L	H	X	X	X	AI to $\overline{B}$ , flip-flop mode
X	H	L	H	X	X	X	X	AI to $\overline{B}$ , latch mode
H	L	X	X	X	L	L	L	$\overline{B}$ to AO, buffer mode
H	X	H	X	X	L	L	L	
H	L	X	X	X	L	H	L	$\overline{B}$ to AO, flip-flop mode
H	X	H	X	X	L	H	L	
H	L	X	X	X	H	X	L	$\overline{B}$ to AO, latch mode
H	X	H	X	X	H	X	L	
H	L	X	X	X	L	L	H	AI to AO, buffer mode
H	X	H	X	X	L	L	H	
H	L	X	X	X	L	H	H	AI to AO, flip-flop mode
H	X	H	X	X	L	H	H	
H	L	X	X	X	H	X	H	AI to AO, latch mode
H	X	H	X	X	H	X	H	
H	H	L	X	X	X	X	L	AI to $\overline{B}$ , $\overline{B}$ to AO



**Function Tables (Continued)**

**ENABLE/DISABLE**

INPUTS			OUTPUTS	
OEA	OEB	$\overline{\text{OEB}}$	AO	$\overline{\text{B}}$
L	X	X	Hi Z	
H	X	X	Active	
X	L	L		Inactive (H)
X	L	H		Inactive (H)
X	H	L		Active
X	H	H		Inactive (H)

**BUFFER**

INPUT	OUTPUT
L	H
H	L

**LATCH**

INPUTS		OUTPUT
CLK/LE	DATA	
H	L	H
H	H	L
L	X	$Q_0$

**LOOPBACK**

LOOPBACK	$Q^\dagger$
L	$\overline{\text{B}}$ port
H	Point $P^\ddagger$

$^\dagger Q$  is the input to the B-to-A logic element.

$^\ddagger P$  is the output of the A-to-B logic element (see functional block diagram).

**SELECT**

INPUTS		SELECTED LOGIC ELEMENT
MODE1	MODE0	
L	L	Buffer
L	H	Flip-flop
H	X	Latch

**FLIP-FLOP**

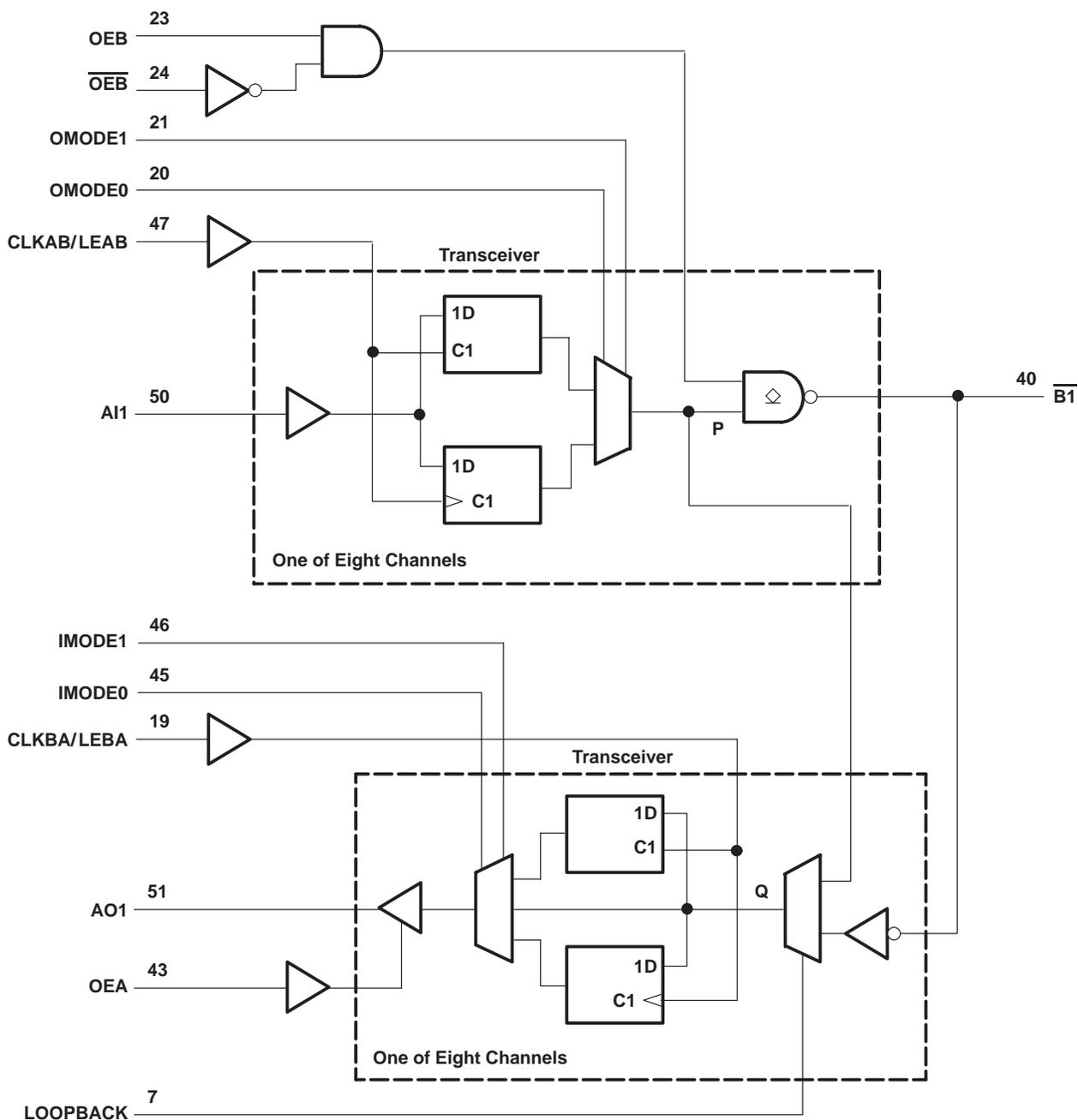
INPUTS		OUTPUT
CLK/LE	DATA	
L	X	$Q_0$
$\uparrow$	L	H
$\uparrow$	H	L

# SN74FB2033A

## 8-BIT TTL/BTL REGISTERED TRANSCEIVER

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### functional block diagram



# SN74FB2033A

## 8-BIT TTL/BTL REGISTERED TRANSCEIVER

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### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ .....	–0.5 V to 7 V
Input clamp current, $V_I$ : Except $\overline{B}$ port .....	–1.2V to 7V
$\overline{B}$ port .....	–1.2V to 3.5V
Voltage range applied to any $\overline{B}$ output in the disabled or power-off state, $V_O$ .....	–0.5 V to 3.5 V
Voltage range applied to any output in the high state, $V_O$ : A port .....	–0.5 V to $V_{CC}$
Input clamp current, $I_{IK}$ : Except $\overline{B}$ port .....	–40 mA
$\overline{B}$ port .....	–18 mA
Current applied to any single output in the low state, $I_O$ : A port .....	48 mA
Package thermal impedance, $\theta_{JA}$ (see Note 1) .....	44°C/W
Storage temperature range, $T_{stg}$ .....	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51.

### recommended operating conditions (see Note 2)

		MIN	NOM	MAX	UNIT
$V_{CC}$ , BG $V_{CC}$	Supply voltage	4.75	5	5.25	V
BIAS $V_{CC}$	Supply voltage	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	$\overline{B}$ port	1.62	2.3	V
		Except $\overline{B}$ port	2		
$V_{IL}$	Low-level input voltage	$\overline{B}$ port	0.75	1.47	V
		Except $\overline{B}$ port	0.8		
$I_{OH}$	High-level output current	AO port		–3	mA
$I_{OL}$	Low-level output current	AO port		24	mA
		$\overline{B}$ port		100	
$\Delta t/\Delta v$	Input transition rise or fall rate	Except $\overline{B}$ port		10	ns/V
$T_A$	Operating free-air temperature	0	70		°C

NOTE 2: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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## 8-BIT TTL/BTL REGISTERED TRANSCEIVER

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### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
$V_{IK}$		$V_{CC} = 4.75\text{ V}$	$I_I = -18\text{ mA}$			-1.2	V
$V_{OH}$	AO port	$V_{CC} = 4.75\text{ V to } 5.25\text{ V}$	$I_{OH} = -10\text{ }\mu\text{A}$			$V_{CC}-1.1$	V
		$V_{CC} = 4.75\text{ V}$	$I_{OH} = -3\text{ mA}$	2.5	2.85	3.4	
$V_{OL}$	AO port	$V_{CC} = 4.75\text{ V}$	$I_{OL} = 20\text{ mA}$		0.33	0.5	V
			$I_{OL} = 55\text{ mA}$			0.8	
	$\bar{B}$ port	$V_{CC} = 4.75\text{ V}$	$I_{OL} = 100\text{ mA}$	0.75		1.1	
			$I_{OL} = 4\text{ mA}$	0.5			
$I_I$	Except $\bar{B}$ port	$V_{CC} = 0,$	$V_I = 5.25\text{ V}$			100	$\mu\text{A}$
$I_{IH}$	Except $\bar{B}$ port	$V_{CC} = 5.25\text{ V},$	$V_I = 2.7\text{ V}$			50	$\mu\text{A}$
	$\bar{B}$ port‡	$V_{CC} = 0\text{ to } 5.25\text{ V},$	$V_I = 2.1\text{ V}$			100	
$I_{IL}$	Except $\bar{B}$ port	$V_{CC} = 5.25\text{ V},$	$V_I = 0.5\text{ V}$			-50	$\mu\text{A}$
	$\bar{B}$ port‡	$V_{CC} = 5.25\text{ V},$	$V_I = 0.75\text{ V}$			-100	
$I_{OH}$	$\bar{B}$ port	$V_{CC} = 0\text{ to } 5.25\text{ V},$	$V_O = 2.1\text{ V}$			100	$\mu\text{A}$
$I_{OZPU}$		$V_{CC} = 0\text{ to } 2.1\text{ V},$	$V_O = 0.5\text{ V to } 2.7\text{ V}$			50	$\mu\text{A}$
$I_{OZPD}$		$V_{CC} = 2.1\text{ V to } 0,$	$V_O = 0.5\text{ V to } 2.7\text{ V}$			-50	$\mu\text{A}$
$I_{OZH}$	AO port	$V_{CC} = 5.25\text{ V},$	$V_O = 2.7\text{ V}$			50	$\mu\text{A}$
$I_{OZL}$	AO port	$V_{CC} = 5.25\text{ V},$	$V_O = 0.5\text{ V}$			-50	$\mu\text{A}$
$I_{OS}^{\S}$	AO port	$V_{CC} = 5.25\text{ V},$	$V_O = 0$	-40	-80	-150	mA
$I_{CC}$	All outputs on	$V_{CC} = 5.25\text{ V},$	$I_O = 0$		45	70	mA
$C_i$	AI port and control inputs	$V_I = 0.5\text{ V or } 2.5\text{ V}$			5		pF
$C_o$	AO port	$V_O = 0.5\text{ V or } 2.5\text{ V}$			5		pF
$C_{io}$	$\bar{B}$ port per IEEE Std 1194.1-1991	$V_{CC} = 0\text{ to } 4.75\text{ V}$				6	pF
		$V_{CC} = 4.75\text{ V to } 5.25\text{ V}$				6	

† All typical values are at  $V_{CC} = 5\text{ V}$ .

‡ For I/O ports, the parameters  $I_{IH}$  and  $I_{IL}$  include the off-state output current.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

### live-insertion characteristics over recommended operating free-air temperature range (see Note 3)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT	
$I_{CC}$ (BIAS $V_{CC}$ )	$V_{CC} = 0\text{ to } 4.5\text{ V}$	$V_B = 0\text{ to } 2\text{ V},$	$V_I$ (BIAS $V_{CC}) = 4.5\text{ V to } 5.5\text{ V}$	10		$\mu\text{A}$	
	$V_{CC} = 4.5\text{ V to } 5.5\text{ V}$			10			
$V_O$	$\bar{B}$ port	$V_{CC} = 0,$	$V_I$ (BIAS $V_{CC}) = 4.5\text{ V to } 5.5\text{ V}$	1.62	2.1	V	
$I_O$	$\bar{B}$ port	$V_{CC} = 0,$	$V_B = 1\text{ V},$	$V_I$ (BIAS $V_{CC}) = 4.5\text{ V to } 5.5\text{ V}$		-1	$\mu\text{A}$
		$V_{CC} = 0\text{ to } 5.5\text{ V},$	$OEB = 0\text{ to } 0.8\text{ V}$			100	
		$V_{CC} = 0\text{ to } 2.2\text{ V},$	$OEB = 0\text{ to } 5\text{ V}$			100	

NOTE 3: The power-up sequence is: GND, BIAS  $V_{CC}$ ,  $V_{CC}$ .



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**timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 2)**

			V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C		MIN	MAX	UNIT
			MIN	MAX			
f <sub>clock</sub>	Clock frequency		150		150		MHz
t <sub>w</sub>	Pulse duration	CLKAB/LEAB or CLKBA/LEBA	3.3		3.3		ns
t <sub>su</sub>	Setup time	Data before CLKAB/LEAB or CLKBA/LEBA↑	2.7		2.7		ns
t <sub>h</sub>	Hold time	Data after CLKAB/LEAB or CLKBA/LEBA↑	0.7		0.7		ns



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## 8-BIT TTL/BTL REGISTERED TRANSCEIVER

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f <sub>max</sub>			150			150		MHz
t <sub>PLH</sub>	AI (through mode)	$\bar{B}$	2.3	3.6	4.6	2.3	5.6	ns
t <sub>PHL</sub>			1.9	3	4.2	1.9	4.5	
t <sub>PLH</sub>	$\bar{B}$ (through mode)	AO	2.5	4.2	5.5	2.5	6.1	ns
t <sub>PHL</sub>			3	4.2	5.6	3	5.7	
t <sub>PLH</sub>	AI (transparent)	$\bar{B}$	2.3	3.6	4.6	2.3	5.6	ns
t <sub>PHL</sub>			1.9	3	4.1	1.9	4.5	
t <sub>PLH</sub>	$\bar{B}$ (transparent)	AO	2.5	4.2	5.5	2.5	6.1	ns
t <sub>PHL</sub>			3	4.2	5.6	3	5.7	
t <sub>PLH</sub>	OEB	$\bar{B}$	2.4	3.7	4.7	2.4	5.8	ns
t <sub>PHL</sub>			1.8	3	4.1	1.8	4.4	
t <sub>PLH</sub>	$\overline{OEB}$	$\bar{B}$	2	3.4	4.3	2	5.2	ns
t <sub>PHL</sub>			2	3.3	4.4	2	4.8	
t <sub>PZH</sub>	OEA	AO	2	3.5	4.6	2	5.1	ns
t <sub>PZL</sub>			2.7	4.2	5.1	2.7	5.4	
t <sub>PHZ</sub>	OEA	AO	2.1	4	5	2.1	5.5	ns
t <sub>PLZ</sub>			1.6	2.8	3.9	1.6	4.3	
t <sub>PLH</sub>	CLKAB/LEAB	$\bar{B}$	3	4.7	5.8	3	6.9	ns
t <sub>PHL</sub>			2.8	4.3	5.6	2.8	6.1	
t <sub>PLH</sub>	CLKBA/LEBA	AO	2	3.6	4.9	2	5.4	ns
t <sub>PHL</sub>			2.2	3.5	4.7	2.2	5.1	
t <sub>PLH</sub>	OMODE	$\bar{B}$	2.4	5	6.1	2.4	7.2	ns
t <sub>PHL</sub>			2.4	4.5	6	2.4	6.7	
t <sub>PLH</sub>	IMODE	AO	1.8	4	5.3	1.8	5.9	ns
t <sub>PHL</sub>			2.3	4.1	5.2	2.3	5.4	
t <sub>PLH</sub>	LOOPBACK	AO	2.4	5	7	2.4	8	ns
t <sub>PHL</sub>			3.1	4.6	5.7	3.1	5.9	
t <sub>PLH</sub>	AI	AO	1.9	3.7	5.5	1.9	6.1	ns
t <sub>PHL</sub>			2.6	4.2	5.6	2.6	5.8	
t <sub>r</sub>	Rise time, 1.3 V to 1.8 V, $\bar{B}$ port		0.5	1.2	2.1	0.5	3	ns
t <sub>f</sub>	Fall time, 1.8 V to 1.3 V, $\bar{B}$ port		0.5	1.4	2.3	0.5	3	
t <sub>r</sub>	Rise time, 10% to 90%, AO		2	3.3	4.2	2	5	ns
t <sub>f</sub>	Fall time, 90% to 10%, AO		1	2.5	3.4	1	5	
$\bar{B}$ -port input pulse rejection						1		ns

### output-voltage characteristics

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V <sub>OHP</sub>	Peak output voltage during turnoff of 100 mA into 40 nH	$\bar{B}$ port	See Figure 1		4.5	V
V <sub>OHV</sub>	Minimum output voltage during turnoff of 100 mA into 40 nH	$\bar{B}$ port	See Figure 1	1.62		V
V <sub>OLV</sub>	Minimum output voltage during high-to-low switch	$\bar{B}$ port	I <sub>OL</sub> = -50 mA	0.3		V



PARAMETER MEASUREMENT INFORMATION

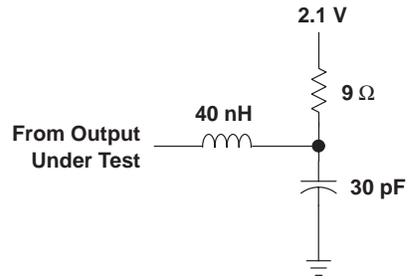
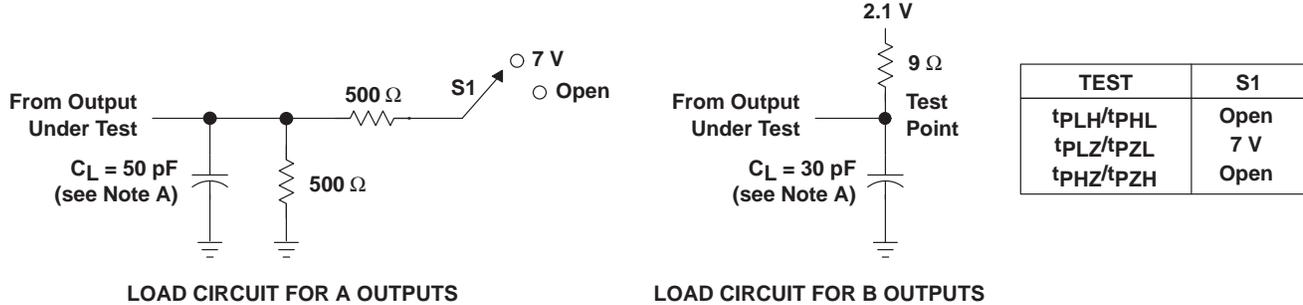


Figure 1. Load Circuit for  $V_{OHP}$  and  $V_{OHV}$

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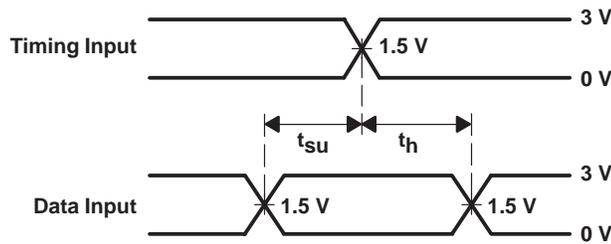
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## PARAMETER MEASUREMENT INFORMATION

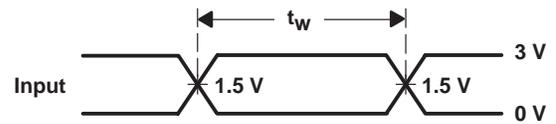


LOAD CIRCUIT FOR A OUTPUTS

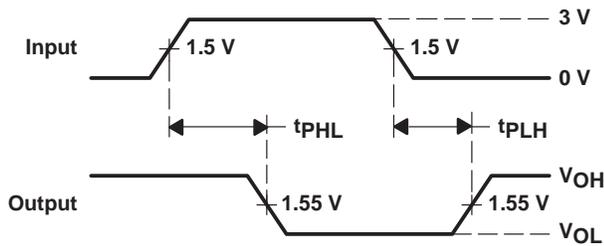
LOAD CIRCUIT FOR B OUTPUTS



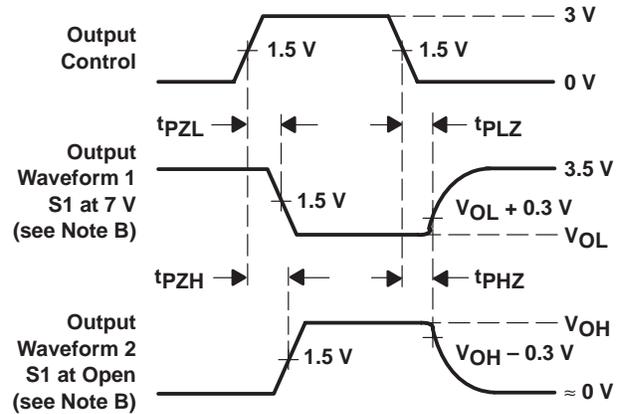
VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



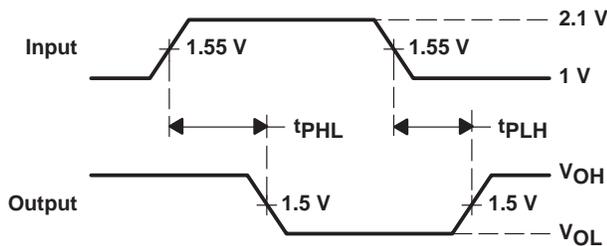
VOLTAGE WAVEFORMS  
PULSE DURATION



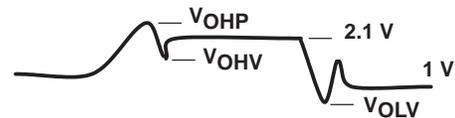
VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES (A TO B)



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES (A PORT)



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES (B TO A)



VOLTAGE WAVEFORMS

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics: TTL inputs:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_f \leq 2.5$  ns; BTL inputs:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_f \leq 2.5$  ns.  
 D. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuits and Voltage Waveforms



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