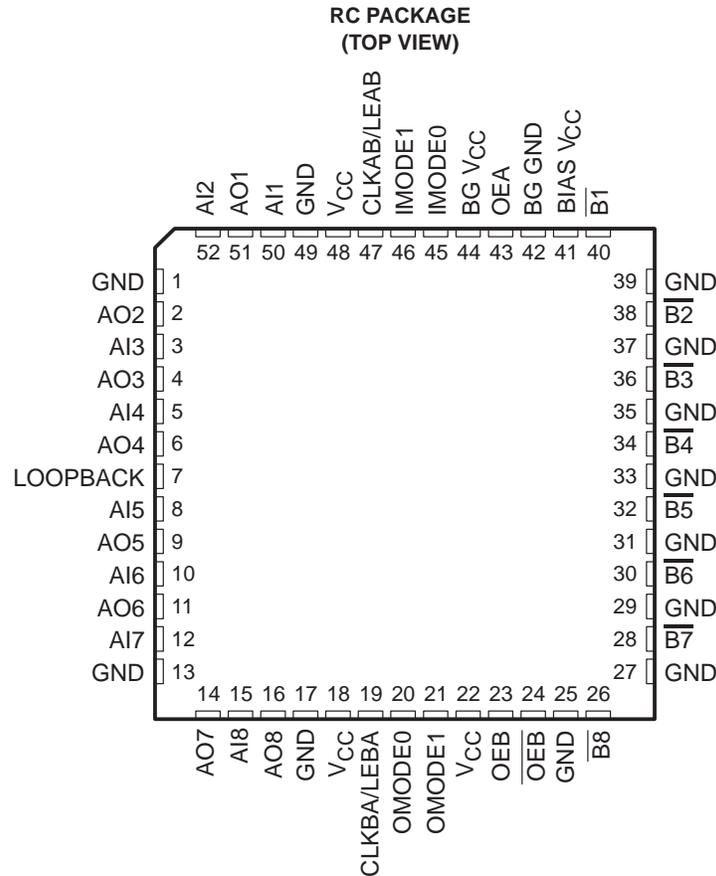


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- Compatible With IEEE Std 1194.1-1991 (BTL)
- TTL A Port, Backplane Transceiver Logic (BTL) \bar{B} Port
- Open-Collector \bar{B} -Port Outputs Sink 100 mA
- BIAS V_{CC} Pin Minimizes Signal Distortion During Live Insertion/Withdrawal
- High-Impedance State During Power Up and Power Down
- \bar{B} -Port Biasing Network Preconditions the Connector and PC Trace to the BTL High-Level Voltage
- TTL-Input Structures Incorporate Active Clamping Networks to Aid in Line Termination
- Packaged in Plastic Quad Flatpack



description

The SN74FB2033K is an 8-bit transceiver featuring a split input (AI) and output (AO) bus on the TTL-level A port. The common I/O, open-collector \bar{B} port operates at backplane transceiver logic (BTL) signal levels. The SN74FB2033K is specifically designed to be compatible with IEEE Std 1194.1-1991.

The logic element for data flow in each direction is configured by two mode inputs (IMODE1 and IMODE0 for B-to-A, OMODE1 and OMODE0 for A-to-B) as a buffer, a D-type flip-flop, or a D-type latch. When configured in the buffer mode, the inverted input data appears at the output port. In the flip-flop mode, data is stored on the rising edge of the appropriate clock input (CLKAB/LEAB or CLKBA/LEBA). In the latch mode, the clock inputs serve as active-high transparent latch enables.



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description (continued)

Data flow in the B-to-A direction, regardless of the logic element selected, is further controlled by the LOOPBACK input. When LOOPBACK is low, \overline{B} -port data is the B-to-A input. When LOOPBACK is high, the output of the selected A-to-B logic element (before inversion) is the B-to-A input.

The AO port-enable/-disable control is provided by OEA. When OEA is low or when V_{CC} is less than 2.5 V, the AO port is in the high-impedance state. When OEA is high, the AO port is active (high or low logic levels).

The \overline{B} port is controlled by OEB and \overline{OEB} . If OEB is low, or \overline{OEB} is high, or when V_{CC} is less than 2.5 V, the \overline{B} port is inactive. If OEB is high and \overline{OEB} is low, the \overline{B} port is active.

BG V_{CC} and BG GND are the bias-generator reference inputs.

The A-to-B and B-to-A logic elements are active, regardless of the state of their associated outputs. The logic elements can enter new data (in flip-flop and latch modes) or retain previously stored data while the associated outputs are in the high-impedance (AO port) or inactive (\overline{B} port) states.

Output clamps are provided on the BTL outputs to reduce switching noise. One clamp reduces inductive ringing effects on V_{OH} during a low-to-high transition. The other clamps out ringing below the BTL V_{OL} voltage of 0.75 V. Both of these clamps are active only during ac switching and do not affect the BTL outputs during steady-state conditions.

BIAS V_{CC} establishes a voltage between 1.62 V and 2.1 V on the BTL outputs when V_{CC} is not connected.

The SN74FB2033K is characterized for operation from 0°C to 70°C.

Function Tables

FUNCTION								FUNCTION/MODE
INPUTS								
OEA	OEB	\overline{OEB}	OMODE1	OMODE0	IMODE1	IMODE0	LOOPBACK	
L	L	X	X	X	X	X	X	Isolation
L	X	H	X	X	X	X	X	Isolation
X	H	L	L	L	X	X	X	AI to \overline{B} , buffer mode
X	H	L	L	H	X	X	X	AI to \overline{B} , flip-flop mode
X	H	L	H	X	X	X	X	AI to \overline{B} , latch mode
H	L	X	X	X	L	L	L	\overline{B} to AO, buffer mode
H	X	H	X	X	L	L	L	\overline{B} to AO, buffer mode
H	L	X	X	X	L	H	L	\overline{B} to AO, flip-flop mode
H	X	H	X	X	L	H	L	\overline{B} to AO, flip-flop mode
H	L	X	X	X	H	X	L	\overline{B} to AO, latch mode
H	X	H	X	X	H	X	L	\overline{B} to AO, latch mode
H	L	X	X	X	L	L	H	AI to AO, buffer mode
H	X	H	X	X	L	L	H	AI to AO, buffer mode
H	L	X	X	X	L	H	H	AI to AO, flip-flop mode
H	X	H	X	X	L	H	H	AI to AO, flip-flop mode
H	L	X	X	X	H	X	H	AI to AO, latch mode
H	X	H	X	X	H	X	H	AI to AO, latch mode
H	H	L	X	X	X	X	L	AI to \overline{B} , \overline{B} to AO

Function Tables (Continued)

ENABLE/DISABLE

INPUTS			OUTPUTS	
OEA	OEB	$\overline{\text{OEB}}$	AO	B
L	X	X	Hi Z	
H	X	X	Active	
X	L	L		Inactive (H)
X	L	H		Inactive (H)
X	H	L		Active
X	H	H		Inactive (H)

BUFFER

INPUT	OUTPUT
L	H
H	L

LATCH

INPUTS		OUTPUT
CLK/LE	DATA	
H	L	H
H	H	L
L	X	Q ₀

LOOPBACK

LOOPBACK	Q [†]
L	$\overline{\text{B}}$ port
H	Point P [‡]

† Q is the input to the B-to-A logic element.

‡ P is the output of the A-to-B logic element (see functional block diagram).

SELECT

INPUTS		SELECTED-LOGIC ELEMENT
MODE1	MODE0	
L	L	Buffer
L	H	Flip-flop
H	X	Latch

FLIP-FLOP

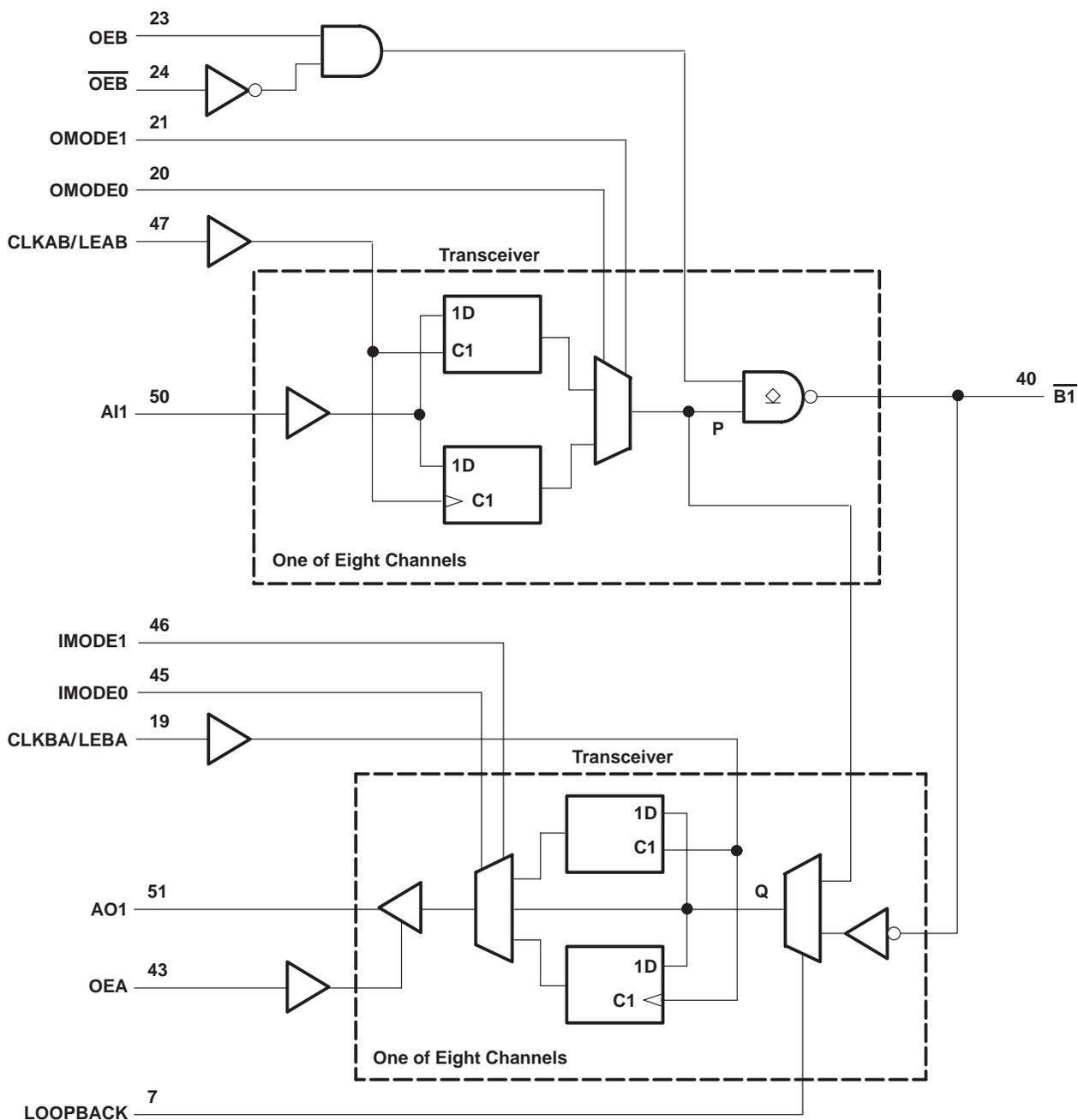
INPUTS		OUTPUT
CLK/LE	DATA	
L	X	Q ₀
↑	L	H
↑	H	L

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functional block diagram



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 7 V
Voltage range applied to any B output in the disabled or power-off state, V_O	–0.5 V to 3.5 V
Voltage range applied to any output in the high state, V_O : A port	–0.5 V to V_{CC}
Input voltage range, V_I : Except \overline{B} port	–1.2 V to 7 V
\overline{B} port	–1.2 V to 3.5 V
Input clamp current, I_{IK} : Except \overline{B} port	–40 mA
\overline{B} port	–18 mA
Current applied to any single output in the low state, I_O : A port	48 mA
\overline{B} port	200 mA
Package thermal impedance, θ_{JA} (see Note 1): RC package	79°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 2)

		MIN	NOM	MAX	UNIT
V_{CC} , BG V_{CC}	Supply voltage	4.75	5	5.25	V
BIAS V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	\overline{B} port	1.62	2.3	V
		Except \overline{B} port	2		
V_{IL}	Low-level input voltage	\overline{B} port	0.75	1.47	V
		Except \overline{B} port		0.8	
I_{OH}	High-level output current			–3	mA
I_{OL}	Low-level output current	AO port		24	mA
		\overline{B} port		100	
$\Delta t/\Delta v$	Input transition rise or fall rate			10	ns/V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: Unused pins (input or I/O) must be held high or low to prevent them from floating.



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electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V _{IK}	\overline{B} port	V _{CC} = 4.75 V,	I _I = -18 mA			-1.2	V
	Except \overline{B} port	V _{CC} = 4.75 V,	I _I = -40 mA			-0.5	
V _{OH}	AO port	V _{CC} = 4.75 V to 5.25 V,	I _{OH} = -10 μA			V _{CC} -1.1	V
		V _{CC} = 4.75 V	I _{OH} = -3 mA	2.5	2.85	3.4	
			I _{OH} = -32 mA	2			
V _{OL}	AO port	V _{CC} = 4.75 V	I _{OL} = 20 mA	0.33		0.5	V
			I _{OL} = 55 mA	0.8			
	\overline{B} port	V _{CC} = 4.75 V	I _{OL} = 100 mA	0.75	1.1		
			I _{OL} = 4 mA	0.5			
I _I	Except \overline{B} port	V _{CC} = 0,	V _I = 5.25 V			100	μA
I _{IH}	Except \overline{B} port	V _{CC} = 5.25 V,	V _I = 2.7 V			50	μA
	\overline{B} port‡	V _{CC} = 0 to 5.25 V,	V _I = 2.1 V			100	
I _{IL}	Except \overline{B} port	V _{CC} = 5.25 V,	V _I = 0.5 V			-50	μA
	\overline{B} port‡	V _{CC} = 5.25 V,	V _I = 0.75 V			-100	
I _{OH}	\overline{B} port	V _{CC} = 0 to 5.25 V,	V _O = 2.1 V			100	μA
I _{OZH}	AO port	V _{CC} = 2.1 V to 5.25 V,	V _O = 2.7 V			50	μA
I _{OZL}	AO port	V _{CC} = 2.1 V to 5.25 V,	V _O = 0.5 V			-50	μA
I _{OZPU} §	A port	V _{CC} = 0 to 2.1 V,	V _O = 0.5 V to 2.7 V			50	μA
I _{OZPD} §	A port	V _{CC} = 2.1 V to 0,	V _O = 0.5 V to 2.7 V			-50	μA
I _{OS} ¶	AO port	V _{CC} = 5.25 V,	V _O = 0	-40	-80	-150	mA
I _{CC}	All outputs on	V _{CC} = 5.25 V,	I _O = 0		45	70	mA
C _i	AI port and control inputs	V _I = 0.5 V or 2.5 V			5		pF
C _o	AO port	V _O = 0.5 V or 2.5 V			5		pF
C _{io} §	\overline{B} port per IEEE Std 1194.1-1991	V _{CC} = 0 to 4.75 V				6	pF
		V _{CC} = 4.75 V to 5.25 V				6	

† All typical values are at V_{CC} = 5 V, T_A = 25°C

‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

§ This parameter is warranted but not production tested.

¶ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.



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live-insertion characteristics over recommended operating free-air temperature range (see Note 3)

PARAMETER		TEST CONDITIONS			MIN	MAX	UNIT
I_{CC} (BIAS V_{CC})		$V_{CC} = 0$ to 4.75 V	$V_B = 0$ to 2 V,	BIAS $V_{CC} = 4.5$ V to 5.5 V		1.2	mA
		$V_{CC} = 4.75$ V to 5.25 V	$V_B = 0$ to 2 V,	BIAS $V_{CC} = 4.5$ V to 5.5 V		10	μ A
V_O	\bar{B} port	$V_{CC} = 0$,	BIAS $V_{CC} = 5$ V		1.62	2.1	V
I_O	\bar{B} port	$V_{CC} = 0$,	$V_B = 1$ V,	V_I (BIAS V_{CC}) = 4.75 V to 5.25 V	-1		μ A
		$V_{CC} = 0$ to 5.25 V,	OEB = 0 to 0.8 V		100		
		$V_{CC} = 0$ to 2.2 V,	OEB = 0 to 5 V		100		

NOTE 3: Power-up sequence is as follows: GND, BIAS V_{CC} , V_{CC} .

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 2)

		$V_{CC} = 5$ V, $T_A = 25^\circ$ C		MIN	MAX	UNIT
		MIN	MAX			
f_{clock}	Clock frequency	0	150	0	150	MHz
t_w	Pulse duration, CLKAB/LEAB or CLKBA/LEBA	3.3		3.3		ns
t_{su}	Setup time, data before CLKAB/LEAB or CLKBA/LEBA \uparrow	2.7		2.7		ns
t_h	Hold time, data after CLKAB/LEAB or CLKBA/LEBA \uparrow	0.7		0.7		ns

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, T _A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f _{max}			150			150		MHz
t _{PLH}	AI (through mode)	\bar{B}	2.8	5.1	6.8	2.8	8.1	ns
t _{PHL}			2.5	4.2	5.7	2.5	6.1	
t _{PLH}	\bar{B} (through mode)	AO	3.1	4.3	5.1	2.2	6.6	ns
t _{PHL}			3.1	4.2	5.1	2.6	6	
t _{PLH}	AI (transparent)	\bar{B}	2.8	5.1	6.8	2.8	8.1	ns
t _{PHL}			2.6	4.2	5.7	2.6	6.1	
t _{PLH}	\bar{B} (transparent)	AO	2.2	4.3	6	2.2	6.6	ns
t _{PHL}			2.5	4.2	5.6	2.5	6	
t _{PLH}	OEB	\bar{B}	2.7	5.1	6.8	2.7	8.3	ns
t _{PHL}			2.4	4.2	5.7	2.4	6.1	
t _{PLH}	\overline{OEB}	\bar{B}	2.5	4.8	6.4	2.5	7.7	ns
t _{PHL}			2.5	4.3	5.9	2.5	6.4	
t _{PZH}	OEA	AO	1.6	3.6	5.1	1.6	5.6	ns
t _{PZL}			2.3	4.3	5.7	2.3	6	
t _{PHZ}	OEA	AO	1.7	4	5.5	1.7	5.9	ns
t _{PLZ}			1.2	2.9	4.4	1.2	4.7	
t _{PLH}	CLKAB/LEAB	\bar{B}	5.2	6.5	7.8	3.7	9.9	ns
t _{PHL}			3.8	5.4	7.1	3.4	7.7	
t _{PLH}	CLKBA/LEBA	AO	1.7	3.8	5.5	1.7	5.9	ns
t _{PHL}			1.8	3.6	5.1	1.8	5.5	
t _{PLH}	OMODE	\bar{B}	2.9	6.6	8.4	2.9	10	ns
t _{PHL}			3	5.7	7.5	3	8.3	
t _{PLH}	IMODE	AO	1.4	4.1	5.8	1.4	6.4	ns
t _{PHL}			1.9	4.2	5.7	1.9	5.9	
t _{PLH}	LOOPBACK	AO	2	5.2	7.3	2	8.2	ns
t _{PHL}			2.6	4.8	6.3	2.6	6.4	
t _{PLH}	AI	AO	1.7	3.9	5.6	1.7	6.1	ns
t _{PHL}			2.2	4.3	5.7	2.2	5.9	
t _r	Rise time, 1.3 V to 1.8 V, \bar{B} port		1.8	2.5	3.8	1.7	4	ns
t _f	Fall time, 1.8 V to 1.3 V, \bar{B} port		1.7	2.5	3.8	1.5	4	
t _r	Rise time, 10% to 90%, AO		2.5	3.4	4.8	2	5	ns
t _f	Fall time, 90% to 10%, AO		1.5	2.5	3.8	1	5	
\bar{B} -port input pulse rejection						1		ns



output-voltage characteristics

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{OHP}^{\dagger}	Peak output voltage during turnoff of 100 mA into 40 nH	\bar{B} port See Figure 1		3	V
V_{OHV}^{\dagger}	Minimum output voltage during turnoff of 100 mA into 40 nH	\bar{B} port See Figure 1	1.62		V
V_{OLV}	Minimum output voltage during high-to-low switch	\bar{B} port $I_{OL} = -50$ mA	0.3		V

[†] This parameter is warranted but not production tested.

PARAMETER MEASUREMENT INFORMATION

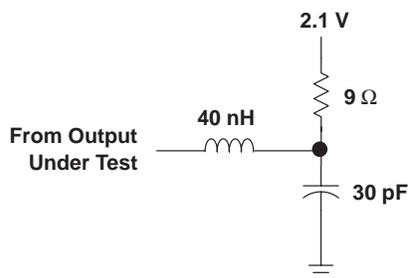
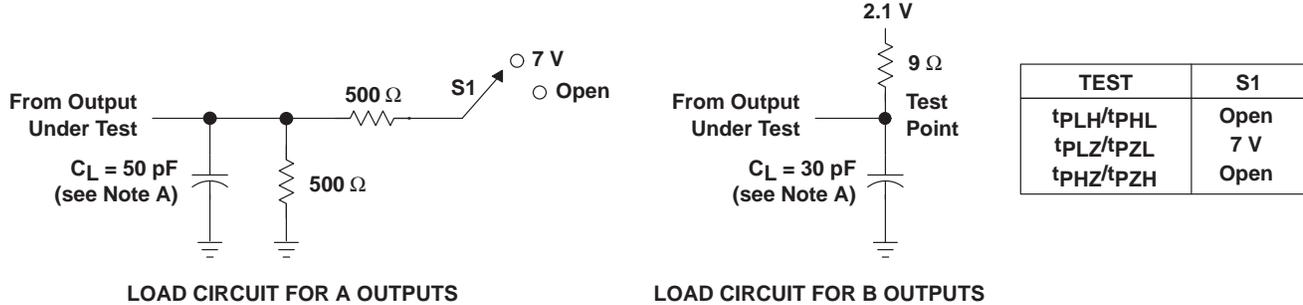


Figure 1. Load Circuit for V_{OHP} and V_{OHV}

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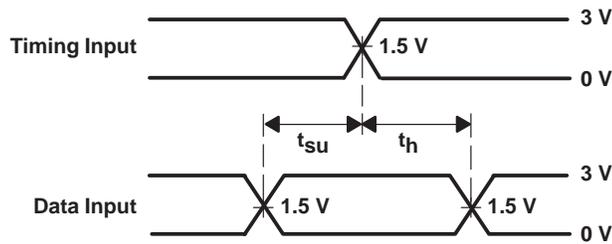
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PARAMETER MEASUREMENT INFORMATION

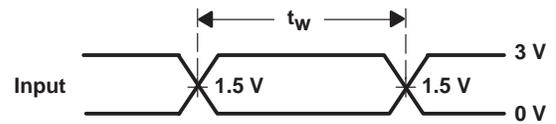


LOAD CIRCUIT FOR A OUTPUTS

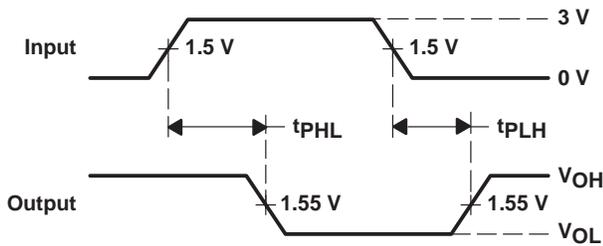
LOAD CIRCUIT FOR B OUTPUTS



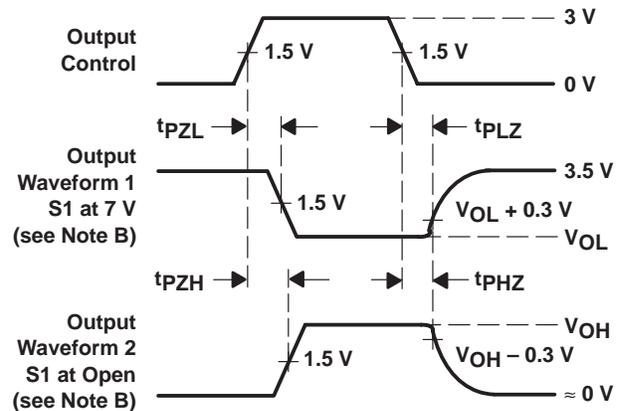
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



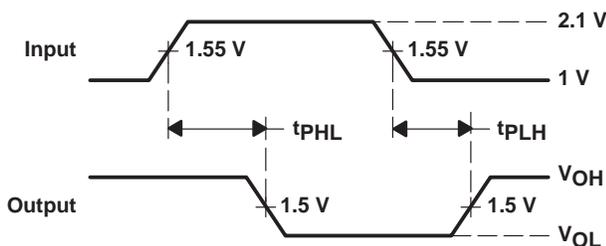
VOLTAGE WAVEFORMS
PULSE DURATION



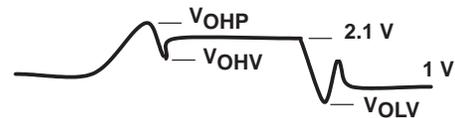
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (A TO B)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES (A PORT)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (B TO A)



VOLTAGE WAVEFORMS

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: TTL inputs: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns; BTL inputs: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms



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