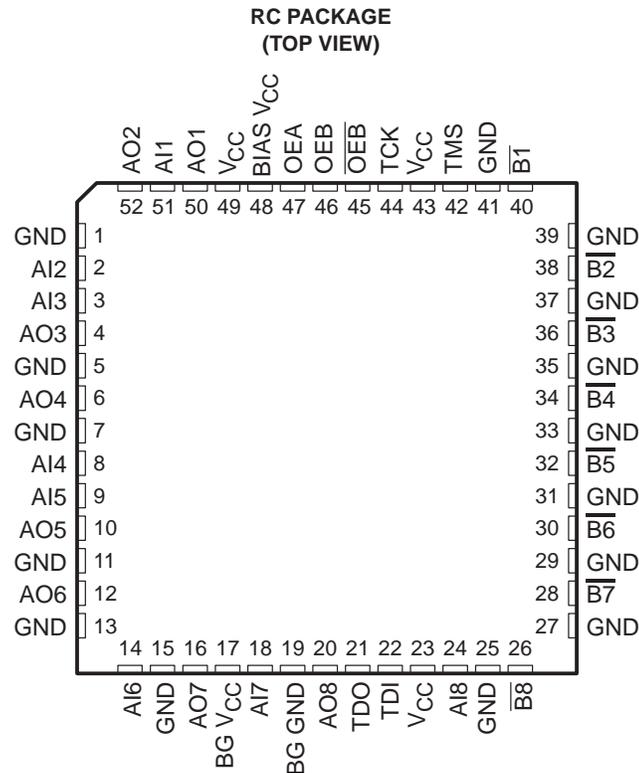


- **Compatible With IEEE Std 1194.1-1991 (BTL)**
- **TTL A Port, Backplane Transceiver Logic (BTL) \bar{B} Port**
- **Open-Collector \bar{B} -Port Outputs Sink 100 mA**
- **Isolated Logic-Ground and Bus-Ground Pins Reduce Noise**
- **High-Impedance State During Power Up and Power Down**
- **BIAS V_{CC} Pin Minimizes Signal Distortion During Live Insertion or Withdrawal**
- **\bar{B} -Port Biasing Network Preconditions the Connector and PC Trace to the BTL High-Level Voltage**
- **Packaged in Plastic Quad Flatpack**



description

The SN74FB2040 device is an 8-bit transceiver designed to translate signals between TTL and backplane transceiver logic (BTL) environments.

The \bar{B} port operates at BTL-signal levels. The open-collector \bar{B} ports are specified to sink 100 mA. Two output enables (OEB and \bar{OEB}) are provided for the \bar{B} outputs. When OEB is high and \bar{OEB} is low, the \bar{B} port is active and reflects the inverse of the data present at the A-input pins. When OEB is low, \bar{OEB} is high, or V_{CC} is less than 2.1 V, the \bar{B} port is turned off.

The A port operates at TTL-signal levels and has separate input and output pins. The A outputs reflect the inverse of the data at the \bar{B} port when the A-port output enable (OEA) is high. When OEA is low or when V_{CC} is less than 2.1 V, the A outputs are in the high-impedance state.

Pins are allocated for the four-wire IEEE Std 1149.1 (JTAG) test bus. TMS and TCK are not connected and TDI is shorted to TDO.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1999, Texas Instruments Incorporated

SN74FB2040 8-BIT TTL/BTL TRANSCEIVER

SCBS173I – NOVEMBER 1991 – REVISED SEPTEMBER 1999

description (continued)

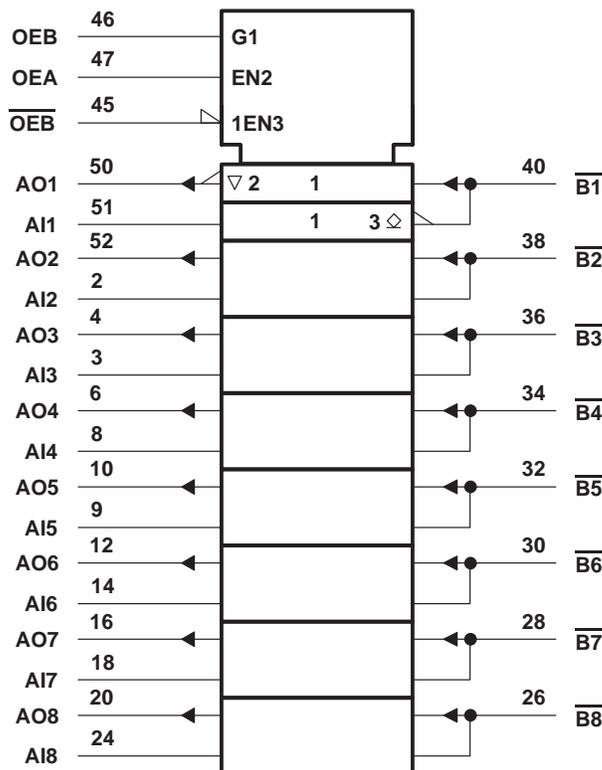
BIAS V_{CC} establishes a voltage between 1.62 V and 2.1 V on the BTL outputs when V_{CC} is not connected.

The SN74FB2040 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

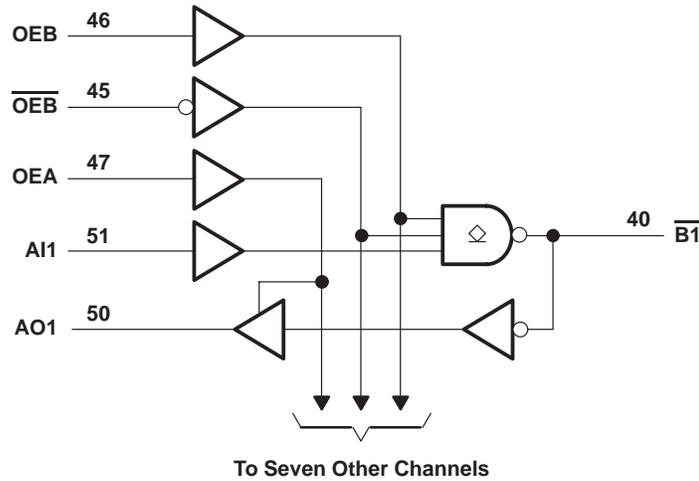
| INPUTS | | | FUNCTION |
|--------|-------------------------|-----|---|
| OEB | $\overline{\text{OEB}}$ | OEA | |
| L | X | L | Isolation |
| X | H | L | |
| L | X | H | $\overline{\text{B}}$ data to AO bus |
| X | H | H | |
| H | L | L | $\overline{\text{A}}$ data to B bus |
| H | L | H | $\overline{\text{A}}$ data to B bus, $\overline{\text{B}}$ data to AO bus |

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|--|--------------------|
| Supply voltage range, V_{CC} | -0.5 V to 7 V |
| Input voltage range, V_I : Except \overline{B} port | -1.2 V to 7 V |
| \overline{B} port | -1.2 V to 3.5 V |
| Voltage range applied to any \overline{B} output in the disabled or power-off state, V_O | -0.5 V to 3.5 V |
| Voltage range applied to any output in the high state, V_O : A port | -0.5 V to V_{CC} |
| Input clamp current, I_{IK} : Except \overline{B} port | -40 mA |
| \overline{B} port | -18 mA |
| Current applied to any single output in the low state, I_O : A port | 48 mA |
| \overline{B} port | 200 mA |
| Package thermal impedance, θ_{JA} (see Note 1) | 44°C/W |
| Storage temperature range, T_{stg} | -65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 2)

| | | MIN | NOM | MAX | UNIT |
|---|--------------------------------|----------------------------|------|------|------|
| V_{CC} , BIAS V_{CC} , BG V_{CC} | Supply voltage | 4.5 | 5 | 5.5 | V |
| V_{IH} | High-level input voltage | \overline{B} port | 1.62 | 2.3 | V |
| | | Except \overline{B} port | 2 | | |
| V_{IL} | Low-level input voltage | \overline{B} port | 0.75 | 1.47 | V |
| | | Except \overline{B} port | | 0.8 | |
| I_{IK} | Input clamp current | | | -18 | mA |
| I_{OH} | High-level output current | | | -3 | mA |
| I_{OL} | Low-level output current | AO port | | 24 | mA |
| | | \overline{B} port | | 100 | |
| T_A | Operating free-air temperature | 0 | | 70 | °C |

NOTE 2: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN74FB2040

8-BIT TTL/BTL TRANSCEIVER

SCBS1731 – NOVEMBER 1991 – REVISED SEPTEMBER 1999

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|-------------------|--|---|---------------------------------|------|------|------|------|
| V _{IK} | \bar{B} port | V _{CC} = MIN, | I _I = -18 mA | | | -1.2 | V |
| | Except \bar{B} port | V _{CC} = MIN, | I _I = -40 mA | | | -0.5 | |
| V _{OH} | AO port | V _{CC} = MIN | I _{OH} = -1 mA | | | | V |
| | | | I _{OH} = -3 mA | 2.5 | 3.3 | | |
| V _{OL} | AO port | V _{CC} = MIN | I _{OL} = 20 mA | | | | V |
| | | | I _{OL} = 24 mA | | 0.35 | 0.5 | |
| | \bar{B} port | V _{CC} = MIN | I _{OL} = 80 mA | 0.75 | | 1.1 | |
| | | | I _{OL} = 100 mA | | | 1.15 | |
| I _I | Except \bar{B} port | V _{CC} = 5.5 V, | V _I = 5.5 V | | | 50 | μA |
| I _{IH} ‡ | Except \bar{B} port | V _{CC} = 5.5 V, | V _I = 2.7 V | | | 50 | μA |
| I _{IL} ‡ | Except \bar{B} port | V _{CC} = 5.5 V, | V _I = 0.5 V | | | -50 | μA |
| | \bar{B} port | V _{CC} = 5.5 V, | V _I = 0.75 V | | | -100 | |
| I _{OH} | \bar{B} port | V _{CC} = 0 to 5.5 V, | V _O = 2.1 V | | | 100 | μA |
| I _{OZH} | AO port | V _{CC} = 5.5 V, | V _O = 2.7 V | | | 50 | μA |
| I _{OZL} | AO port | V _{CC} = 5.5 V, | V _O = 0.5 V | | | -50 | μA |
| I _{OZPU} | A port | V _{CC} = 0 to 2.1 V, | V _O = 0.5 V to 2.7 V | | | 50 | μA |
| I _{OZPD} | A port | V _{CC} = 2.1 V to 0, | V _O = 0.5 V to 2.7 V | | | -50 | μA |
| I _{OS} § | AO port | V _{CC} = 5.5 V, | V _O = 0 | -30 | | -180 | mA |
| I _{CC} | AI port to \bar{B} port | V _{CC} = 5.5 V, | I _O = 0 | | 40 | | mA |
| | \bar{B} port to AO port | | | | 70 | | |
| C _i | AI port | V _I = V _{CC} or GND | | | 3.5 | | pF |
| | Control inputs | | | | 3 | | |
| C _O | AO port | V _O = V _{CC} or GND | | | 6 | | pF |
| C _{io} | \bar{B} port per IEEE Std 1194.1-1991 | V _{CC} = 0 to 4.5 V | | | | 5 | pF |
| | | V _{CC} = 4.5 V to 5.5 V | | | | 5 | |

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

live-insertion specifications over recommended operating free-air temperature range

| PARAMETER | | TEST CONDITIONS | | MIN | MAX | UNIT |
|---|----------------|--------------------------------|--|------|-----|------|
| I _{CC} (BIAS V _{CC}) | | V _{CC} = 0 to 4.5 V | V _B = 0 to 2 V, V _I (BIAS V _{CC}) = 4.5 V to 5.5 V | | 450 | μA |
| | | V _{CC} = 4.5 to 5.5 V | | | 10 | |
| V _O | \bar{B} port | V _{CC} = 0, | V _I (BIAS V _{CC}) = 5 V | 1.62 | 2.1 | V |
| I _O | \bar{B} port | V _{CC} = 0, | V _B = 1 V, V _I (BIAS V _{CC}) = 4.5 V to 5.5 V | | -1 | μA |
| | | V _{CC} = 0 to 5.5 V, | OEB = 0 to 0.8 V | | 100 | |
| | | V _{CC} = 0 to 2.2 V, | OEB = 0 to 5 V | | 100 | |



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN74FB2040 8-BIT TTL/BTL TRANSCEIVER

SCBS173I – NOVEMBER 1991 – REVISED SEPTEMBER 1999

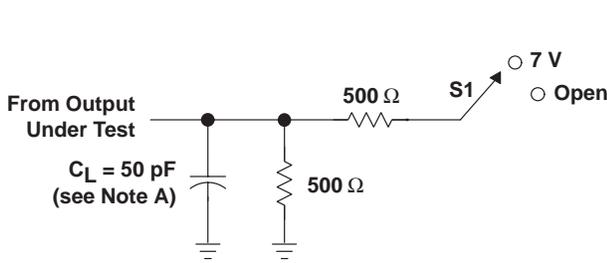
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V _{CC} = 5 V, T _A = 25°C | | | MIN | MAX | UNIT |
|---------------------------------------|--|----------------|---|-----|-----|-----|-----|------|
| | | | MIN | TYP | MAX | | | |
| t _{PLH} | AI | \bar{B} | 3.2 | 4.5 | 6 | 2.4 | 6.5 | ns |
| t _{PHL} | | | 2.8 | 4.2 | 5.6 | 2.7 | 5.8 | |
| t _{PLH} | \bar{B} | AO | 2.3 | 3.8 | 5.7 | 1.9 | 6.2 | ns |
| t _{PHL} | | | 2.3 | 4.2 | 5.9 | 2 | 8.2 | |
| t _{PLH} | OEB | \bar{B} | 3.7 | 5.1 | 6.7 | 3 | 7 | ns |
| t _{PHL} | | | 3.1 | 4.6 | 5.9 | 3 | 6.1 | |
| t _{PLH} | \overline{OEB} | \bar{B} | 3.6 | 5.2 | 6.8 | 3.3 | 7 | ns |
| t _{PHL} | | | 2.9 | 4.4 | 5.9 | 2.6 | 6.1 | |
| t _{PZH} | OEA | AO | 2.5 | 4 | 5.5 | 2.1 | 5.8 | ns |
| t _{PZL} | | | 2.1 | 3.6 | 4.8 | 2 | 5 | |
| t _{PHZ} | OEA | AO | 2.3 | 4.1 | 5.9 | 1.9 | 6.5 | ns |
| t _{PLZ} | | | 1.6 | 3.1 | 4.5 | 1.4 | 4.7 | |
| t _{sk(p)} | Pulse skew, AI to \bar{B} or \bar{B} to AO | | 0.5 | | | | | ns |
| t _{sk(o)} | Pulse skew, AI to \bar{B} or \bar{B} to AO | | 0.4 | | | | | ns |
| t _r | Rise time, 1.3 V to 1.8 V, \bar{B} port | | 2 | 2.8 | 3.8 | 1.7 | | ns |
| t _f | Fall time, 1.8 V to 1.3 V, \bar{B} port | | 1 | 1.9 | 3 | 1 | 4.2 | ns |
| \bar{B} -port input pulse rejection | | | | | | 1 | 3.4 | ns |

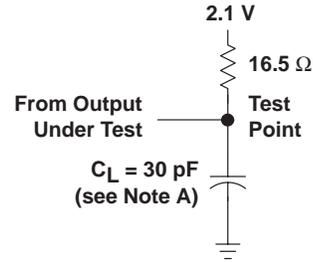
SN74FB2040 8-BIT TTL/BTL TRANSCEIVER

SCBS173I – NOVEMBER 1991 – REVISED SEPTEMBER 1999

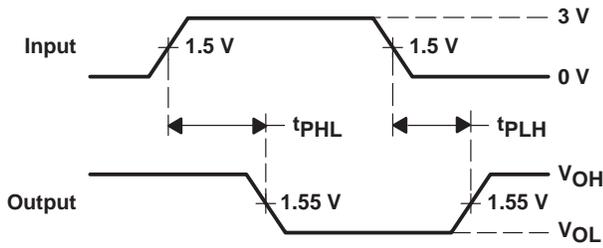
PARAMETER MEASUREMENT INFORMATION



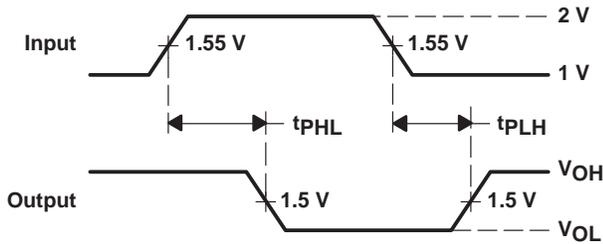
LOAD CIRCUIT FOR A OUTPUTS



LOAD CIRCUIT FOR B OUTPUTS

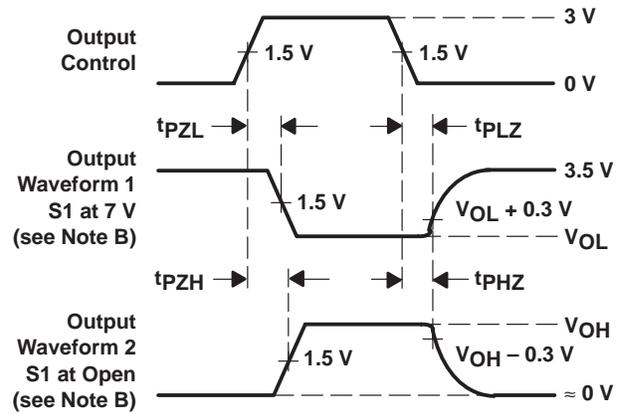


VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (A TO B)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (B TO A)

| TEST | S1 |
|-------------------|------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | 7 V |
| t_{PHZ}/t_{PZH} | Open |



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES (A PORT)

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: TTL inputs: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns; BTL inputs: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.

Copyright © Each Manufacturing Company.

All Datasheets cannot be modified without permission.

This datasheet has been download from :

www.AllDataSheet.com

100% Free DataSheet Search Site.

Free Download.

No Register.

Fast Search System.

www.AllDataSheet.com