

74FR2244

Octal Buffer/Line Driver with 25Ω Series Resistors in the Outputs

General Description

The 74FR2244 is a non-inverting octal buffer and line driver designed to drive capacitive inputs of MOS memory devices, address and clock lines or act as a low undershoot general purpose bus driver.

Features

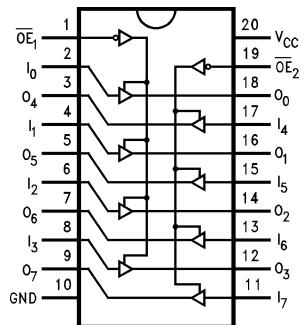
- 3-STATE outputs drive bus lines or buffer memory address registers
- Outputs sink 12 mA and source 15 mA
- 25Ω series resistors in outputs eliminate the need for external resistors
- Designed to drive the capacitive inputs of MOS devices

Ordering Code:

Order Number	Package Number	Package Description
74FR2244SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74FR2244SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74FR2244PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Pin Descriptions

Pin Names	Description
$\overline{OE}_1, \overline{OE}_2$	Output Enable Input (Active-LOW)
I_0-I_7	Inputs
$\overline{O}_0-\overline{O}_7$	Outputs

Truth Tables

Inputs		Outputs (Pins 12, 14, 16, 18)
\overline{OE}_1	I_n	
L	L	L
L	H	H
H	X	Z

Inputs		Outputs (Pins 3, 5, 7, 9)
\overline{OE}_2	I_n	
L	L	L
L	H	H
H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Absolute Maximum Ratings ^(Note 1)							Recommended Operating Conditions	
Storage Temperature								
Ambient Temperature under Bias								
Junction Temperature under Bias								
V _{CC} Pin Potential to Ground Pin								
Input Voltage (Note 2)								
Input Current (Note 2)								
Voltage Applied to Output								
in HIGH State (with V _{CC} = 0V)								
Standard Output								
3-STATE Output								
Current Applied to Output								
in LOW State (Max)								
ESD Last Passing Voltage (Min)								
Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired.								
Note 2: Either voltage limit or current limit is sufficient to protect inputs.								
DC Electrical Characteristics								
Symbol	Parameter	Min	Typ	Max	Units	V _{CC}	Conditions	
V _{IH}	Input HIGH Voltage	2.0			V		Recognized HIGH Signal	
V _{IL}	Input LOW Voltage			0.8	V		Recognized LOW Signal	
V _{CD}	Input Clamp Diode Voltage			-1.2	V	Min	I _{IN} = -18 mA	
V _{OH}	Output HIGH Voltage	2.4			V	Min	I _{OH} = -3 mA	
		2.0			V	Min	I _{OH} = -15 mA	
V _{OL}	Output LOW Voltage		0.5	V	Min	I _{OL} = 1 mA		
			0.75	V	Min	I _{OL} = 12 mA		
I _{IH}	Input HIGH Current		5	μA	Max	V _{IN} = 2.7V		
I _{BVI}	Input HIGH Current Breakdown Test		7	μA	Max	V _{IN} = 7.0V		
I _{IL}	Input LOW Current		-150	μA	Max	V _{IN} = 0.5V		
V _{ID}	Input Leakage Test	4.75			V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded	
I _{OD}	Output Circuit Leakage Current		3.75	μA	0.0	V _{OD} = 150 mV All Other Pins Grounded		
I _{OZH}	Output Leakage Current		20	μA	Max	V _{OUT} = 2.7V		
I _{OZL}	Output Leakage Current		-20	μA	Max	V _{OUT} = 0.5V		
I _{OS}	Output Short-Circuit Current	-100	-225	mA	Max	V _{OUT} = 0.0V		
I _{CEx}	Output HIGH Leakage Current		50	μA	Max	V _{OUT} = V _{CC}		
I _{ZZ}	Bus Drainage Test		100	μA	0.0	V _{OUT} = 5.25V		
I _{CCH}	Power Supply Current		40	mA	Max	All Outputs HIGH		
I _{CCL}	Power Supply Current		70	mA	Max	All Outputs LOW		
I _{CCZ}	Power Supply Current		46	mA	Max	Outputs 3-STATE		

AC Electrical Characteristics

Symbol	Parameter	$T_A = +25^\circ C$			$T_A = 0^\circ C$ to $+70^\circ C$		Units	
		$V_{CC} = +5.0V$			$V_{CC} = +5.0V$			
		Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay	1.0	2.6	4.4	1.0	4.4	ns	
t_{PHL}		1.0	1.8	4.4	1.0	4.4	ns	
t_{PZH}	Output Enable Time	2.5	4.8	7.1	2.5	7.1	ns	
t_{PZL}		2.5	3.9	7.1	2.5	7.1	ns	
t_{PHZ}	Output Disable Time	1.6	3.7	6.4	1.6	6.4	ns	
t_{PLZ}		1.6	3.6	6.4	1.6	6.4	ns	

Extended AC Electrical Characteristics

Symbol	Parameter	$T_A = 0^\circ C$ to $+70^\circ C$			$T_A = 0^\circ C$ to $+70^\circ C$		Units	
		$V_{CC} = +5.0V$			$V_{CC} = +5.0V$			
		Min	Max	Min	Max			
t_{PLH}	Propagation Delay	1.0	5.9	2.7	9.7	ns	ns	
t_{PHL}		1.0	5.9	2.7	9.7	ns	ns	
t_{PZH}	Output Enable Time	2.5	8.0			ns	ns	
t_{PZL}		2.5	8.0			ns	ns	
t_{PHZ}	Output Disable Time	1.6	7.0			ns	ns	
t_{PLZ}		1.6	7.0			ns	ns	
t_{OSHL}	Pin-to-Pin Skew for HL Transitions (Note 5)		1.5			ns	ns	
t_{OSLH}	Pin-to-Pin Skew for LH Transitions (Note 5)		1.5			ns	ns	
t_{OST}	Pin-to-Pin Skew for HL/LH Transitions (Note 5)		3.0			ns	ns	

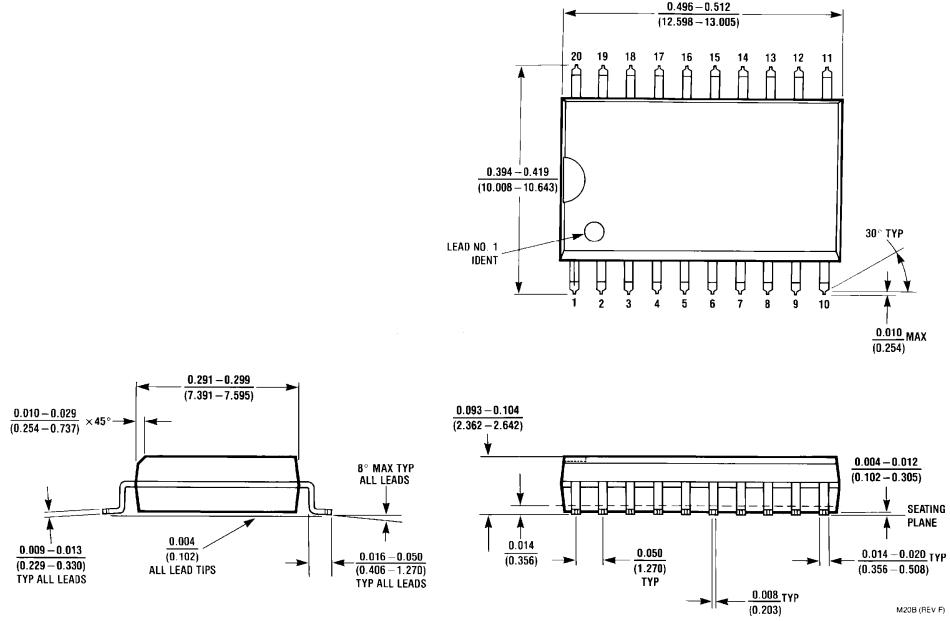
Note 3: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase, i.e., all LOW-to-HIGH, HIGH-to-LOW, 3-STATE-to-HIGH, etc.

Note 4: These specifications guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

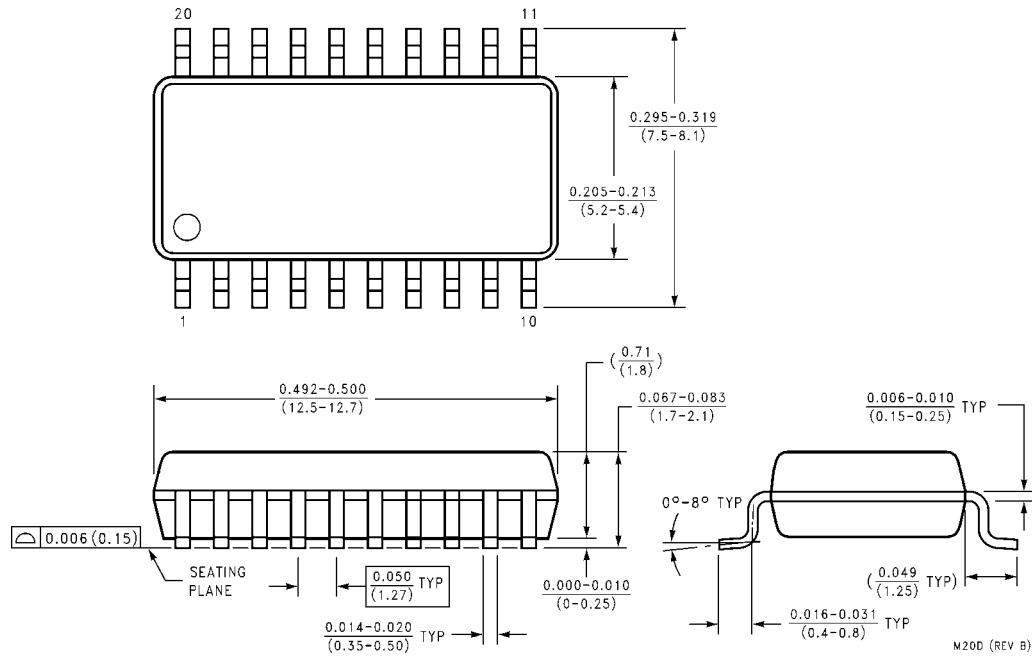
Note 5: Skew is defined as the absolute value of the difference between the actual propagation delays for any two outputs of the same device. The specification applies to any outputs switching HIGH-to-LOW, (t_{OSHL}), LOW-to-HIGH, (t_{OSLH}), or HIGH-to-LOW and/or LOW-to-HIGH, (t_{OST}). Specifications guaranteed with all outputs switching in phase.

Physical Dimensions

inches (millimeters) unless otherwise noted



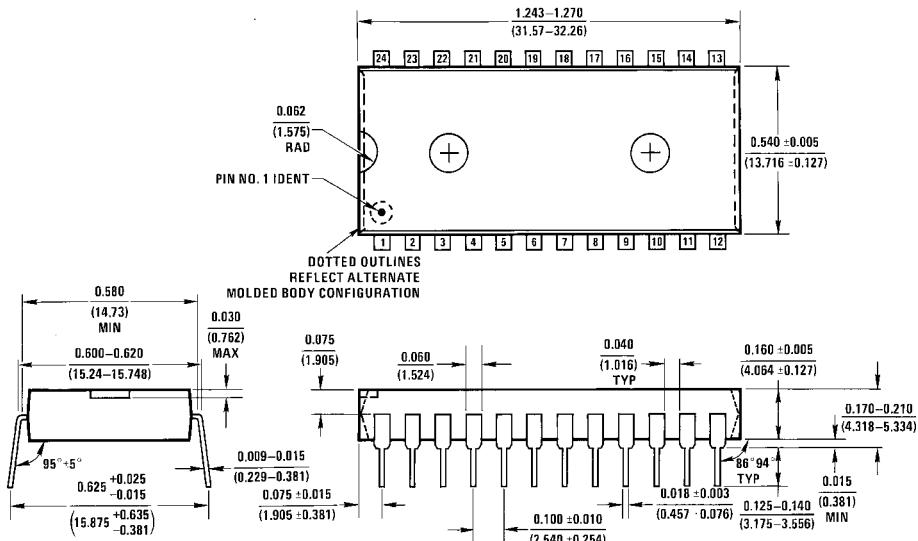
20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
Package Number M20B



20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M20D

Physical Dimensions

inches (millimeters) unless otherwise noted (Continued)



N24A (REV E)

20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N20A

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