

74FR245

Octal Bidirectional Transceiver with 3-STATE Outputs

General Description

The 74FR245 contains eight non-inverting bidirectional buffers with 3-STATE outputs and is intended for bus-oriented applications. Current sinking capability is 64 mA on both the A and B Ports. The Transmit/Receive (T/R) input determines the direction of data flow through the bidirectional transceiver. Transmit (active-HIGH) enables data from A Ports to B Ports; Receive (active-LOW) enables data from B Ports to A Ports. The Output Enable input, when HIGH, disables both A and B Ports by placing them in a High Z condition.

Features

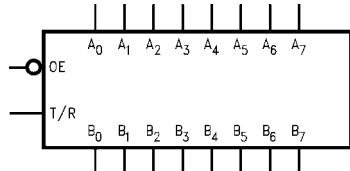
- Non-inverting buffers
- Bidirectional data path
- A and B output sink capability of 64 mA, source capability of 15 mA
- Guaranteed pin-to-pin skew

Ordering Code:

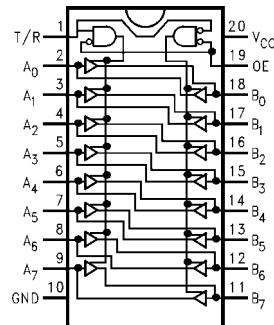
| Order Number | Package Number | Package Description |
|--------------|----------------|---|
| 74FR245SC | M20B | 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide |
| 74FR245SJ | M20D | 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| 74FR245PC | N20A | 20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide |

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbol



Connection Diagram



Pin Descriptions

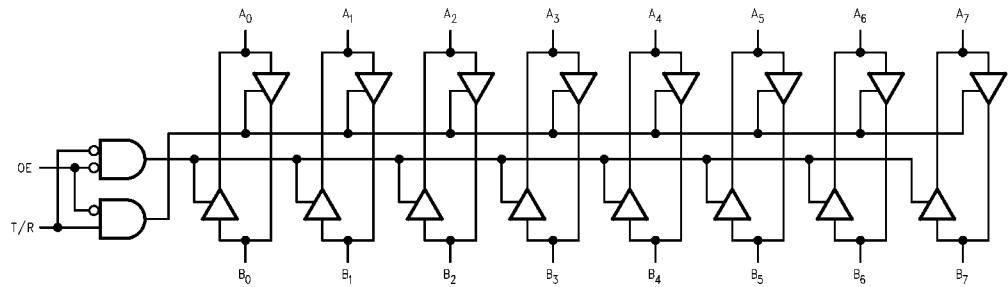
| Pin Names | Description |
|--------------------------------|----------------------------------|
| OE | Output Enable Input (Active-LOW) |
| T/R | Transmit/Receive Input |
| A ₀ -A ₇ | Side A Inputs or 3-STATE Outputs |
| B ₀ -B ₇ | Side B Inputs or 3-STATE Outputs |

Truth Table

| Inputs | Output | |
|--------|--------|---------------------|
| | OE | T/R |
| L | L | Bus B Data to Bus A |
| L | H | Bus A Data to Bus B |
| H | X | High Z State |

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram



Absolute Maximum Ratings(Note 1)

| | |
|--------------------------------------|-------------------------------|
| Storage Temperature | -65°C to +150°C |
| Ambient Temperature under Bias | -55°C to +125°C |
| Junction Temperature under Bias | -55°C to +150°C |
| V_{CC} Pin Potential to Ground Pin | -0.5V to +7.0V |
| Input Voltage (Note 2) | -0.5V to +7.0V |
| Input Current (Note 2) | -30 mA to +5.0 mA |
| Voltage Applied to Output | |
| in HIGH State (with $V_{CC} = 0V$) | |
| Standard Output | -0.5V to V_{CC} |
| 3-STATE Output | -0.5V to +5.5V |
| Current Applied to Output | |
| in LOW State (Max) | twice the rated I_{OL} (mA) |
| ESD Last Passing Voltage (Min) | 4000V |

Recommended Operating Conditions

| | |
|------------------------------|----------------|
| Free Air Ambient Temperature | 0°C to +70°C |
| Supply Voltage | +4.5V to +5.5V |

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

| Symbol | Parameter | Min | Typ | Max | Units | V _{CC} | Conditions |
|--------------------|---|------|-----|------|---------|-----------------|---|
| V_{IH} | Input HIGH Voltage | 2.0 | | | V | | Recognized HIGH Signal |
| V_{IL} | Input LOW Voltage | | | 0.8 | V | | Recognized LOW Signal |
| V_{CD} | Input Clamp Diode Voltage | | | -1.2 | V | Min | $I_{IN} = -18$ mA |
| V_{OH} | Output HIGH Voltage | 2.4 | | | V | Min | $I_{OH} = -3$ mA (A_n, B_n) |
| | | 2.0 | | | V | Min | $I_{OH} = -15$ mA (A_n, B_n) |
| V_{OL} | Output LOW Voltage | | | 0.55 | V | Min | $I_{OL} = 64$ mA (A_n, B_n) |
| I_{IH} | Input HIGH Current | | | 5 | μ A | Max | $V_{IN} = 2.7V$ ($\overline{OE}, \overline{T/R}$) |
| I_{BVI} | Input HIGH Current Breakdown Test | | | 7 | μ A | Max | $V_{IN} = 7.0V$ ($\overline{OE}, \overline{T/R}$) |
| I_{BVIT} | Input HIGH Current Breakdown Test (I/O) | | | 100 | μ A | Max | $V_{IN} = 5.5V$ (A_n, B_n) |
| I_{IL} | Input LOW Current | | | -250 | μ A | Max | $V_{IN} = 0.5V$ ($\overline{OE}, \overline{T/R}$) |
| V_{ID} | Input Leakage Test | 4.75 | | | V | 0.0 | $I_{ID} = 1.9$ μ A All Other Pins Grounded |
| I_{OD} | Output Circuit Leakage Current | | | 3.75 | μ A | 0.0 | $V_{IOD} = 150$ mV All Other Pins Grounded |
| $I_{IH} + I_{OZH}$ | Output Leakage Current | | | 25 | μ A | Max | $V_{OUT} = 2.7V$ (A_n, B_n) |
| $I_{IL} + I_{OZL}$ | Output Leakage Current | | | -150 | μ A | Max | $V_{OUT} = 0.5V$ (A_n, B_n) |
| I_{OS} | Output Short-Circuit Current | -100 | | -225 | mA | Max | $V_{OUT} = 0.0V$ (A_n, B_n) |
| I_{CEX} | Output HIGH Leakage Current | | | 50 | μ A | Max | $V_{OUT} = V_{CC}$ (A_n, B_n) |
| I_{ZZ} | Bus Drainage Test | | | 100 | μ A | 0.0 | $V_{OUT} = 5.25V$ (A_n, B_n) |
| I_{CCH} | Power Supply Current | 55 | 75 | | mA | Max | All Outputs HIGH |
| I_{CCL} | Power Supply Current | 75 | 110 | | mA | Max | All Outputs LOW |
| I_{CCZ} | Power Supply Current | 55 | 75 | | mA | Max | Outputs 3-STATE |
| C_{IN} | Input Capacitance | 8.0 | | | pF | 5.0 | $\overline{OE}, \overline{T/R}$ |
| | | 17.0 | | | pF | 5.0 | A_n, B_n |

AC Electrical Characteristics

| Symbol | Parameter | $T_A = +25^\circ C$ $V_{CC} = +5.0V$ $C_L = 50 pF$ | | | $T_A = 0^\circ C$ to $+70^\circ C$ $V_{CC} = +5.0V$ $C_L = 50 pF$ | | Units |
|-----------|---|--|-----|-----|---|-----|-------|
| | | Min | Typ | Max | Min | Max | |
| t_{PLH} | Propagation Delay A_n to B_n or B_n to A_n | 1.0 | 2.6 | 3.9 | 1.0 | 3.9 | ns |
| | | 1.0 | 1.7 | 3.9 | 1.0 | 3.9 | |
| t_{PZH} | Output Enable Time | 2.5 | 5.0 | 7.0 | 2.5 | 7.0 | ns |
| | | 2.5 | 4.3 | 7.0 | 2.5 | 7.0 | |
| t_{PHZ} | Output Disable Time | 1.7 | 3.7 | 6.5 | 1.7 | 6.5 | ns |
| | | 1.7 | 3.6 | 6.5 | 1.7 | 6.5 | |
| t_{PLZ} | | | | | | | |

Extended AC Characteristics

| Symbol | Parameter | $T_A = 0^\circ C$ to $+70^\circ C$ $V_{CC} = +5.0V$ $C_L = 50 pF$ | | | $T_A = 0^\circ C$ to $+70^\circ C$ $V_{CC} = +5.0V$ $C_L = 250 pF$ (Note 4) | | Units |
|------------------------|---|---|------|-----|--|----|-------|
| | | Min | Max | Min | Max | | |
| t_{PLH} | Propagation Delay A_n to B_n or B_n to A_n | 1.0 | 5.9 | 2.5 | 7.5 | ns | |
| | | 1.0 | 5.9 | 2.5 | 7.5 | | |
| t_{PZH} | Output Enable Time | 2.5 | 11.9 | | | ns | |
| | | 2.5 | 11.9 | | | | |
| t_{PHZ} | Output Disable Time | 1.3 | 6.5 | | | ns | |
| | | 1.3 | 6.5 | | | | |
| t_{OSHL} (Note 5) | Pin to Pin Skew for HL Transitions | | 1.7 | | | ns | |
| t_{OSLH} (Note 5) | Pin to Pin Skew for LH Transitions | | 1.0 | | | ns | |
| t_{OST} (Note 5) | Pin to Pin Skew for HL/LH Transitions | | 3.3 | | | ns | |

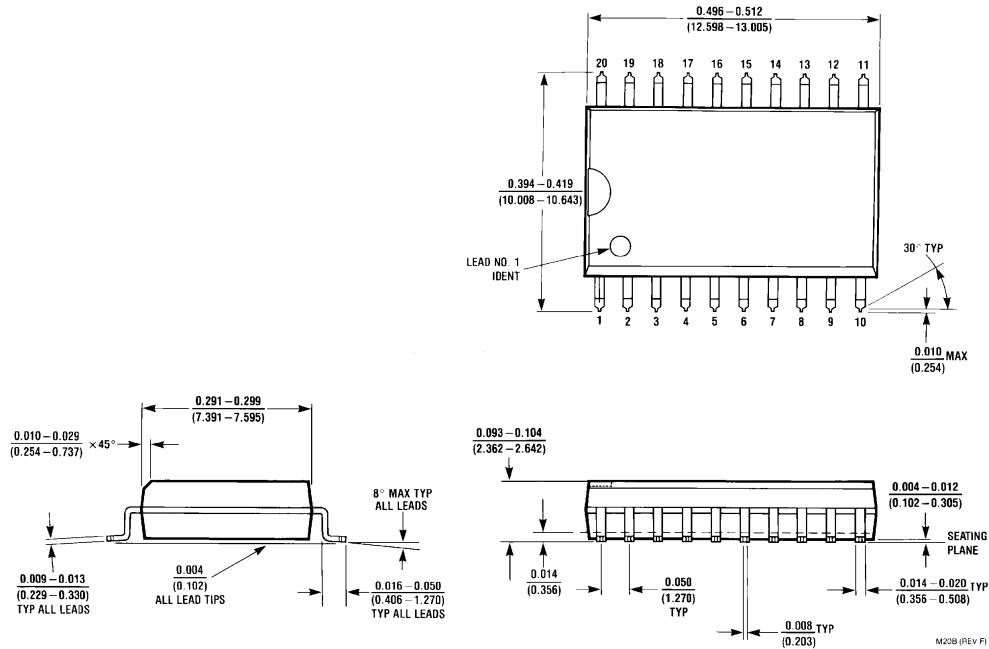
Note 3: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase, i.e., all LOW-to-HIGH, HIGH-to-LOW, 3-STATE-to-HIGH, etc.

Note 4: These specifications guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

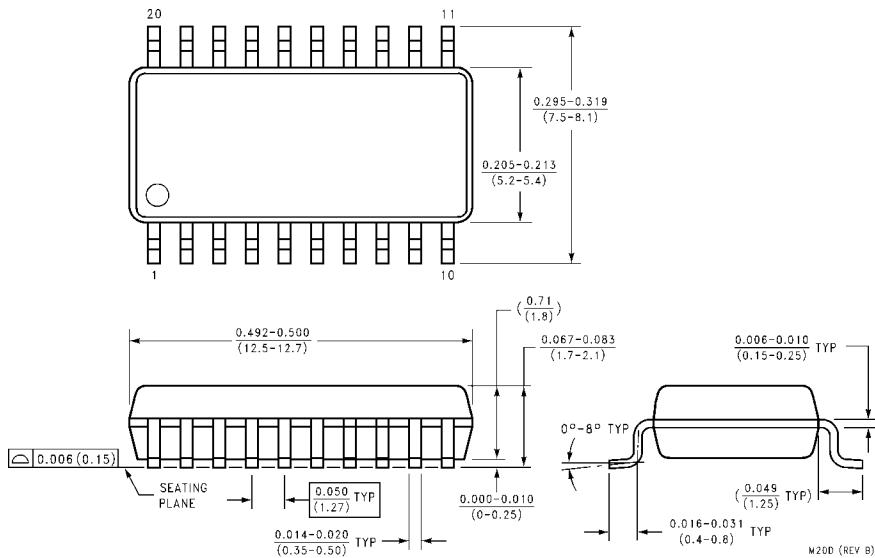
Note 5: Skew is defined as the absolute value of the difference between the actual propagation delays for any two outputs of the same device. The specification applies to any outputs switching HIGH-to-LOW (t_{OSHL}), LOW-to-HIGH (t_{OSLH}), or HIGH-to-LOW and/or LOW-to-HIGH (t_{OST}). Specifications guaranteed with all outputs switching in phase.

Physical Dimensions

inches (millimeters) unless otherwise noted

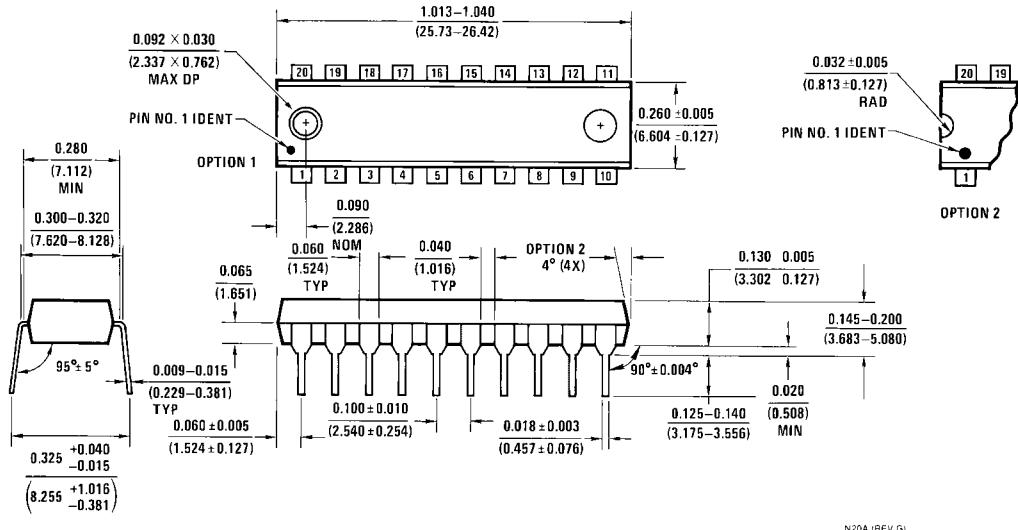


20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
Package Number M20B



20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M20D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N20A**

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