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 Members of the Texas Instruments Widebus™ Family 	SN54GTL16616 SN74GTL16616	6 WD PACKAGE DGG OR DL PACKAGE
● Universal Rus Transceiver (URT™)	(10	P VIEW)
Combines D Type Letebes and D Type		
Compines D-Type Latches and D-Type		56 L CEAB
Flip-Flops for Operation in Transparent,	LEAB 2	55 CLKAB
Latched, Clocked, or Clock-Enabled Mode	A1 🛛 3	54 🛛 B1
 GTL Buffered CLKAB Signal (CLKOUT) 	GND 4	53 🛛 GND
Translate Between GTL/GTL+ Signal Levels	A2 🛛 5	52 🛛 B2
and LVTTL Logic Levels	A3 🛛 6	51 🛛 B3
Support Mixed-Mode (3.3 V and 5 V) Signal	V _{CC} (3.3 V) 🛛 7	50 🛛 V _{CC} (5 V)
Operation on A-Port and Control Inputs	A4 🛛 8	49 🛛 B4
Equivalent to '16601 Eurotian	A5 🛛 9	48 🛛 B5
	A6 🛿 10	47 🛛 B6
 I_{off} Supports Partial-Power-Down Mode 	GND 🛿 11	46 🛛 GND
Operation	A7 🚺 12	45 🛛 B7
 Bus Hold on Data Inputs Eliminates the 	A8 🚺 13	44 🛛 B8
Need for External Pullup/Pulldown	A9 🚺 14	43 🛛 B9
Resistors on A Port	A10 🚺 15	42 🛛 B10
Latch-Up Performance Exceeds 100 mA Per	A11 🚺 16	41 🛛 B11
JESD 78, Class II	A12 🚺 17	40 🛛 B12
Distributed Vcc and GND-Pin Configuration	GND [18	39 🛛 GND
Minimizes High-Speed Switching Noise	A13 🚺 19	38 🛛 B13
Backage Ontions Include Plastic Shrink	A14 🛛 20	37 🛛 B14
 Fackage Options include Flastic Shrink Small-Outling (DL) Thin Shrink 	A15 🛛 21	36 🛛 B15
Small-Outline (DC), Thin Shrink Small-Outline (DCC), and Coramic Elat	V _{CC} (3.3 V) [22	35 🛛 V _{RFF}
(WD) Packages	A16 23	34 🛛 B16
(WD) Fackages	A17 🛛 24	33 🛛 B17
description	GND 25	32 🛛 GND
		31 CLKOUT
The 'GTL16616 devices are 17-bit universal	OEBA 27	30 CLKBA
bus transceivers (UBTs) that provide	LEBA	29 T CEBA

signal-level translation. They combine D-type flip-flops and D-type latches to allow for transparent, latched, clocked, and clocked-enabled modes of data transfer identical to the '16601 function. Additionally, they provide for a copy of CLKAB at GTL/GTL+ signal levels (CLKOUT) and conversion of a GTL/GTL+ clock to LVTTL logic levels (CLKIN). The devices provide an interface between cards operating at LVTTL logic levels and a backplane operating at GTL/GTL+ signal levels. Higher-speed operation is a direct result of the reduced output swing (<1 V), reduced input threshold levels, and output edge control (OEC[™]).

The user has the flexibility of using this device at either GTL ($V_{TT} = 1.2$ V and $V_{REF} = 0.8$ V) or the preferred higher noise margin GTL+ ($V_{TT} = 1.5$ V and $V_{REF} = 1$ V) signal levels. GTL+ is the Texas Instruments derivative of the Gunning transceiver logic (GTL) JEDEC standard JESD 8-3. The B port normally operates at GTL or GTL+ signal levels, while the A-port and control inputs are compatible with LVTTL logic levels and are 5-V tolerant. V_{REF} is the reference input voltage for the B port. V_{CC} (5 V) supplies the internal and GTL circuitry while V_{CC} (3.3 V) supplies the LVTTL output buffers.



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LVTTL-to-GTL/GTL+ and GTL/GTL+-to-LVTTL

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description (continued)

Data flow in each direction is controlled by output-enable (OEAB and OEBA), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. The clock can be controlled by the clock-enable (CEAB and CEBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CEAB is low and CLKAB is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the low-to-high transition of CLKAB if CEAB also is low. When OEAB is low, the outputs are active. When OEAB is high, the outputs are in the high-impedance state. Data flow for B to A is similar to that of A to B, but uses OEBA, LEBA, CLKBA, and CEBA.

These devices are fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

Active bus-hold circuitry holds unused or undriven LVTTL inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54GTL16616 is characterized for operation over the full military temperature range of -55° C to 125° C. The SN74GTL16616 is characterized for operation from -40° C to 85° C.

			_		-	
	INPUTS					NODE
CEAB	OEAB	LEAB	CLKAB	Α	В	MODE
Х	Н	Х	Х	Х	Z	Isolation
L	L	L	H or L	Х	в ₀ ‡	Latabad storage of A data
L	L	L	H or L	Х	в ₀ §	Latched storage of A data
Х	L	Н	Х	L	L	Transport
Х	L	Н	Х	Н	н	Transparent
L	L	L	\uparrow	L	L	Clasked storage of A data
L	L	L	\uparrow	Н	н	Clocked storage of A data
Н	L	L	Х	Х	B ₀ §	Clock inhibit

FUNCTION TABLE[†]

[†] A-to-<u>B</u> data flow is shown. B-to-A data flow is similar, but uses OEBA, LEBA, CLKBA, and CEBA.

[‡] Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low

§ Output level before the indicated steady-state input conditions were established



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logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC} : 3.3 V	–0.5 V to 4.6 V
5 V	_0.5 V to 7 V
Input voltage range, VI (see Note 1): A-port and control inputs	–0.5 V to 7 V
B port and V _{REF}	–0.5 V to 4.6 V
Voltage range applied to any output in the high or power-off state, V_{O}	
(see Note 1): A port	–0.5 V to 7 V
B port	–0.5 V to 4.6 V
Current into any output in the low state, I_{Ω} : A port	128 mA
B port	80 mA
Current into any A-port output in the high state. In (see Note 2)	64 mA
Continuous current through each Vcc or GND	±100 mA
Input clamp current. In $(V_1 < 0)$	
Output clamp current l_{OK} (Vo < 0)	-50 mA
Backage thermal impedance (), (and Note 2); DCC package	GAOCAN
Package inermal impedance, θ_{JA} (see Note 3): DGG package	
DL package	56°C/W
Storage temperature range, T _{stg}	. −65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This current flows only when the output is in the high state and $V_O > V_{CC}$.

3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Notes 4 through 6)

			SN	154GTL1661	6	SN74GTL16616			
			MIN	NOM	MAX	MIN	NOM	MAX	
Vee	Supplyvaltage	3.3 V	3.15	3.3	3.45	3.15	3.3	3.45	V
VCC	Supply voltage	5 V	4.75	5	5.25	4.75	5	5.25	
V	Termination	GTL	1.14	1.2	1.26	1.14	1.2	1.26	V
VTT	voltage	GTL+	1.35	1.5	1.65	1.35	1.5	1.65	
V	Cupply voltogo	GTL	0.74	0.8	0.87	0.74	0.8	0.87	V
VREF	Supply voltage	GTL+	0.87	1 🖉	1.1	0.87	1	1.1	
	Input voltage	B port		E.	VTT			VTT	V
		Except B port		Q.	5.5			5.5	1 ^v
	High-level	B port	V _{REF} +50 mV	5		V _{REF} +50 mV			V
VIН	input voltage	Except B port	2	201		2			v
Ma	Low-level	B port	4	۲ کر	/REF-50 mV		,	V _{REF} -50 mV	V
VIL VIL	input voltage	Except B port		7	0.8			0.8	ľ
Iк	Input clamp currer	nt			-18			-18	mA
ЮН	High-level output current	A port			-32			-32	mA
	Low-level	A port			64			64	
OL	output current	B port			40			40	
ТА	Operating free-air	temperature	-55		125	-40		85	°C

NOTES: 4. All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

5. Normal connection sequence is GND first, $V_{CC} = 5 V$ second, and $V_{CC} = 3.3 V$, I/O, control inputs, V_{TT} and V_{REF} (any order) last. 6. V_{TT} and R_{TT} can be adjusted to accommodate backplane impedances as long as they do not exceed the DC absolute I_{OL} ratings.

Similarly, V_{REF} can be adjusted to optimize noise margins, but normally is 2/3 V_{TT}.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

		TEAT COND		SN54GTL16616 SN74GTL16616 MIN TYP [†] MAX MIN TYP [†]		6					
	VEIER	TEST COND	TIONS			MAX	UNII				
VIK		V _{CC} (3.3 V) = 3.15 V, V _{CC} (5	V) = 4.75 V, IJ = -18 mA			-1.2			-1.2	V	
Vон	A port	V _{CC} (3.3 V)= 3.15 V to 3.45 V, V _{CC} (5 V) = 4.75 V to 5.25 V	I _{OH} = –100 μA	V _{CC} -0.2			V _{CC} -0.2			V	
	[·]	V _{CC} (3.3 V) = 3.15 V,	I _{OH} = –8 mA	2.4			2.4				
		V _{CC} (5 V) = 4.75 V	I _{OH} = -32 mA	2			2				
			I _{OL} = 100 μA			0.2			0.2		
	Anort	V _{CC} (3.3 V) = 3.15 V,	I _{OL} = 16 mA			0.4			0.4		
VOL	Apon	V _{CC} (5 V) = 4.75 V	I _{OL} = 32 mA			0.5			0.5	V	
			I _{OL} = 64 mA			0.55			0.55	v	
	B port	V _{CC} (3.3 V) = 3.15 V, V _{CC} (5 V) = 4.75 V	I _{OL} = 40 mA			0.4			0.4		
	Control inputs	V _{CC} = 0 or 3.45 V, V _{CC} (5 V) = 0 or 5.25 V	V _I = 5.5 V			10			10		
	A port		VI = 5.5 V			20			20		
l II		V _{CC} (3.3 V) = 3.45 V, V _{CC} (5 V) = 5.25 V	$V_{I} = V_{CC} (3.3 V)$			1			1	μA	
			VI = 0		4	-30			-30		
	Bnort	V _{CC} (3.3 V) = 3.45 V,	VI = VCC (3.3 V)		IE .	5			5		
	в роп	V _{CC} (5 V) = 5.25 V	V _I = 0		2F	-5			-5		
loff		$V_{CC} = 0$, V_I or $V_O = 0$ to 4.5 V	,	4	2	100			100	μA	
	A port	V_{CC} (3.3 V) = 3.15 V,	V _I = 0.8 V	75 5			75				
II(hold)			V _I = 2 V	-75			-75			μΑ	
ll(hold)			$V_{I} = 0 \text{ to } V_{CC} (3.3 \text{ V})^{\ddagger}$	40		±500			±500		
10711	A port	V_{CC} (3.3 V) = 3.45 V, V_{CC} (5	V) = 5.25 V, V _O = 3 V			1			1	Δ	
'OZH	B port	V_{CC} (3.3 V) = 3.45 V, V_{CC} (5	V) = 5.25 V, V _O = 1.2 V			10			10	μΛ	
1071	A port	V_{CC} (3.3 V) = 3.45 V, V_{CC} (5	V) = 5.25 V, V_{O} = 0.5 V			-1			-1	Δ	
'OZL	B port	V_{CC} (3.3 V) = 3.45 V, V_{CC} (5	V) = 5.25 V, V_0 = 0.4 V			-10			$\begin{array}{c} 0.5 \\ 0.55 \\ \hline 0.4 \\ \hline 0.5 \\ \hline 0.4 \\ \hline 0.5 \\ \hline 0.4 \\ \hline 0.5 \\ \hline 0.4 \\ \hline $	μΛ	
		V _{CC} (3.3 V) = 3.45 V,	Outputs high			1			1		
I CC (3.3 V)	Dort	V_{CC} (5 V) = 5.25 V, I _O = 0,	Outputs low			5			5	mA	
(0.0.1)	F	$V_{I} = V_{CC} (3.3 \text{ V}) \text{ or GND}$	Outputs disabled		-	1			1		
	A D	V _{CC} (3.3 V) = 3.45 V,	Outputs high			120			120		
ICC (5 V)	A or B	V_{CC} (5 V) = 5.25 V, I_{O} = 0,	Outputs low			120			120	mA	
(0.1)	pon	$V_{I} = V_{CC} (3.3 \text{ V}) \text{ or GND}$	Outputs disabled			120			120		
∆ICC§		V_{CC} (3.3 V) = 3.45 V, V_{CC} (5 A-port or control inputs at V_{CC} One input at 2.7 V	V) = 5.25 V, (3.3 V) or GND,			1			1	mA	
Ci	Control inputs	V _I = 3.15 V or 0			3.5			3.5		pF	
Cia	A port	V _O = 3.15 V or 0			12			12		рF	
	B port	Per IEEE Std 1194.1				5			5	PL_	

[†] All typical values are at V_{CC} (3.3 V) = 3.3 V, V_{CC} (5 V) = 5 V, T_A = 25°C.

[‡] This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another. § This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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timing requirements over recommended ranges of supply voltage and operating free-air temperature, $V_{TT} = 1.2$ V and $V_{REF} = 0.8$ V for GTL (unless otherwise noted) (see Figure 1)

			SN54GTI	16616	SN74GTL	16616	LINUT		
			MIN	MAX	MIN	MAX	UNIT		
fclock	Clock frequency			95		95	MHz		
	Pulso duration	LEAB or LEBA high	3.3		3.3		00		
١W	Puise duration	CLKAB or CLKBA high or low	5.5		5.5		115		
		A before CLKAB↑	1.3		1.3				
		B before CLKBA↑	2.5	FW	2.5				
	Setup time	A before LEAB↓	0	EN	0		ns		
^t su		B before LEBA↓	1.1 🗸		1.1				
		CEAB before CLKAB [↑]	2.2		2.2				
		CEBA before CLKBA↑	2.7		2.7				
		A after CLKAB↑	21.6		1.6				
		B after CLKBA↑	0.4		0.4				
↓	Hold time	A after LEAB↓	4		4				
τh	Hold lime	B after LEBA↓	3.5		3.5		ns		
		CEAB after CLKAB↑	1.1		1.1				
		CEBA after CLKBA↑	0.9		0.9				



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switching characteristics over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.2 V and V_{REF} = 0.8 V for GTL (see Figure 1)

DADAMETED	FROM	то	SN54GTL16616			SN74GTL16616			
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT
fmax			95			95			MHz
^t PLH	٨	R	1.4	3	4.6	1.7	3	4.4	00
^t PHL	A	в	1.2	2.8	4.7	1.4	2.8	4.5	115
^t PLH		P	2.1	3.8	5.6	2.3	3.8	5.4	200
^t PHL	LEAD	D	1.9	3.7	5.6	2.2	3.7	5.3	115
^t PLH		P	2.2	4	5.9	2.4	4	5.7	-
^t PHL	ULKAB	D	1.8	3.7	5.7	2.1	3.7	5.4	115
^t PLH			4.5	6.1	8.2	4.7	6.1	8.1	-
^t PHL	CLKAD	GLKOUT	5.5	7.9	11.4	5.7	7.9	11.3	115
^t dis	OEAB		2	3.8	5.8	2.1	3.8	5.6	00
t _{en}		DEAD DOI CERCOT	2	3.6	5.2	2.1	3.6	5.1	115
t _r	Transition time, B or	utputs (0.5 V to 1 V)		\$ 1.2			1.2		ns
tf	Transition time, B or	utputs (1 V to 0.5 V)	20	0.7			0.7		ns
^t PLH	P	٨	1.6	4	6.8	1.7	4	6.7	00
^t PHL	в	A	1.3	2.9	4.7	1.4	2.9	4.7	115
^t PLH		٨	2.3	3.8	6.1	2.4	3.8	5.8	200
^t PHL	LEDA	~	1.9	3	4.8	2	3	4.6	115
^t PLH		٨	2.5	4	6.3	2.6	4	6	00
^t PHL	CERBA	A	2.1	3.4	5.1	2.2	3.4	4.9	115
^t PLH			7.2	10	14.7	7.4	10	14.4	20
^t PHL			5.9	8.1	11.8	6.1	8.1	11.7	115
ten	OERA	A or CLKIN	2.7	5.3	8.1	2.8	5.3	7.8	ns
^t dis	UEDA		2.6	4.3	6.7	2.7	4.3	6.4	115

[†] All typical values are at V_{CC} (3.3 V) = 3.3 V, V_{CC} (5 V) = 5 V, T_A = 25°C.



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timing requirements over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.5 V and V_{REF} = 1 V for GTL+ (unless otherwise noted) (see Figure 1)

			SN54GTI	16616	SN74GTL	16616	LINUT		
			MIN	MAX	MIN	MAX	UNIT		
fclock	Clock frequency			95		95	MHz		
	Pulso duration	LEAB or LEBA high	3.3		3.3		00		
١W	ruise uuralion	CLKAB or CLKBA high or low	5.5		5.5		115		
		A before CLKAB↑	1.3		1.3				
		B before CLKBA↑	2.3	-In	2.3				
	Setup time	A before LEAB↓	0	N:	0		ns		
ⁱ su		B before LEBA↓	1.3		1.3				
		CEAB before CLKAB↑	2.2		2.2				
		CEBA before CLKBA↑	2.7		2.7				
		A after CLKAB↑	A.6		1.6				
		B after CLKBA↑	~ 0.6		0.6				
L.	Hold time	A after LEAB↓	4		4				
τh	Hold lime	B after LEBA↓	3.5		3.5		ns		
		CEAB after CLKAB↑	1.1		1.1				
		CEBA after CLKBA↑	0.9		0.9				



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switching characteristics over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.5 V and V_{REF} = 1 V for GTL+ (see Figure 1)

DADAMETED	FROM	то	SN5	4GTL16	616	SN74GTL16616			
PARAMETER	(INPUT)	(OUTPUT)	MIN	түр†	MAX	MIN	TYP [†]	MAX	UNIT
f _{max}			95			95			MHz
^t PLH	٨	R	1.4	3	4.6	1.7	3	4.4	00
^t PHL	~	в	1.2	2.9	4.8	1.4	2.9	4.6	115
^t PLH		P	2.1	3.8	5.6	2.3	3.8	5.4	200
^t PHL	LLAD	в	1.9	3.7	5.7	2.2	3.7	5.4	115
^t PLH		P	2.2	4	5.9	2.4	4	5.7	00
^t PHL	CLKAB	D	1.8	3.8	5.8	2.1	3.8	5.5	115
^t PLH	CLKAR		4.5	6.1	8.2	4.7	6.1	8.1	-
^t PHL	CLNAD	CEROOT	5.5	8	11.5	5.7	8	11.4	115
^t PLH	OEAB	OEAB B or CLKOUT	2	3.6	5.2	2.1	3.6	5.1	ns
^t PHL			2	3.8	5.9	2.1	3.8	5.7	
t _r	Transition time, B or	utputs (0.5 V to 1 V)		\$ 1.4			1.4		ns
tf	Transition time, B or	utputs (1 V to 0.5 V)	40	1			1		ns
^t PLH	в	P A	1,5	3.9	6.8	1.6	3.9	6.6	ne
^t PHL	В	~	1.2	2.8	4.5	1.3	2.8	4.5	115
^t PLH	LEBA	۸	2.3	3.8	6.1	2.4	3.8	5.8	ne
^t PHL	LEDA	~	1.9	3	4.8	2	3	4.6	115
^t PLH		۸	2.5	4	6.3	2.6	4	6	ne
^t PHL	OERBA	~	2.1	3.4	5.1	2.2	3.4	4.9	115
^t PLH			7.1	9.9	14.7	7.3	9.9	14.3	20
^t PHL	CLKOUT	CERIN	5.8	8	11.6	6	8	11.5	115
ten	OERA	A or CLKIN	2.7	5.3	8.1	2.8	5.3	7.8	ns
^t dis	UEDA		2.6	4.3	6.7	2.7	4.3	6.4	115

[†] All typical values are at V_{CC} (3.3 V) = 3.3 V, V_{CC} (5 V) = 5 V, T_A = 25°C.



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PARAMETER MEASUREMENT INFORMATION $V_{TT} = 1.2 V$, $V_{REF} = 0.8 V$ FOR GTL AND $V_{TT} = 1.5 V$, $V_{REF} = 1 V$ FOR GTL+



[†] All control inputs are TTL levels.

NOTES: A. CL includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_Q = 50 Ω , t_f \leq 2.5 ns, t_f \leq 2.5 ns.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
- Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.





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