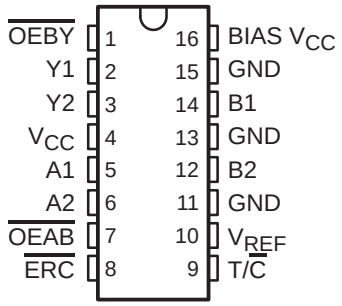
- **Bidirectional Interface Between GTL+ Signal Levels and LVTTL Logic Levels**
- **LVTTL Interfaces Are 5-V Tolerant**
- **High-Drive GTL+ Outputs (100 mA)**
- **LVTTL Outputs (–24 mA/24 mA)**
- **Variable Edge-Rate Control ($\overline{ERC}$) Input Selects GTL+ Rise and Fall Times for Optimal Data-Transfer Rate and Signal Integrity**
- **I_{off}, Power-Up 3-State, and BIAS V_{CC} Support Live Insertion**
- **Polarity Control Selects True or Complementary Outputs**
- **Package Options Include Plastic Small-Outline (D), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages**

D, DGV, OR PW PACKAGE
(TOP VIEW)



description

The SN74GTLP1394 is a high-drive 2-bit 3-wire bus transceiver that provides LVTTL-to-GTL+ and GTL+-to-LVTTL signal-level translation. It allows for transparent and inverted transparent modes of data transfer with separate LVTTL input and LVTTL output pins. The device provides a high-speed interface between cards operating at LVTTL logic levels and a backplane operating at GTL+ signal levels and is especially designed to work with the Texas Instruments TSB14C01A 1394 Backplane Physical-Layer Controller. High-speed (about two times faster than standard LVTTL or TTL) backplane operation is a direct result of GTLP's reduced output swing (<1 V), reduced input threshold levels, improved differential input, and output edge control (OEC™). Improved GTLP OEC circuits minimize bus settling time and have been designed and tested using several backplane models. The high drive is suitable for driving double-terminated low-impedance backplanes using incident-wave switching.

GTL+ is the Texas Instruments derivative of the Gunning transceiver logic (GTL) JEDEC standard JESD 8-3. The AC specification of the SN74GTLP1394 is given only at the preferred higher noise margin GTL+, but the user has the flexibility of using this device at either GTL (V_{TT} = 1.2 V and V_{REF} = 0.8 V) or GTL+ (V_{TT} = 1.5 V and V_{REF} = 1 V) signal levels.

Normally, the B port operates at GTL or GTL+ levels. The A inputs, Y outputs, and control inputs are compatible with LVTTL logic levels and are 5-V tolerant. V_{REF} is the reference input voltage for the B port.

This device is fully specified for live-insertion applications using I_{off}, power-up 3-state, and BIAS V_{CC}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict. The BIAS V_{CC} circuitry precharges and preconditions the B-port input/output connections, preventing disturbance of active data on the backplane during card insertion or removal, and permits true live-insertion capability.

High-drive GTLP backplane interface devices feature adjustable edge-rate control ($\overline{ERC}$). Changing the $\overline{ERC}$ input voltage between GND and V_{CC} adjusts the B-port output rise and fall times. This allows the designer to optimize system data-transfer rate and signal integrity to the backplane load.

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description (continued)

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, the output-enable ($\overline{OE}$) input should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74GTLP1394 is characterized for operation from –40°C to 85°C.

functional description

The output-enable ($\overline{OEAB}$) input controls the activity of the B port. When $\overline{OEAB}$ is low, the B-port outputs are active. When $\overline{OEAB}$ is high, the B-port outputs are disabled.

Separate input and output pins allow the device to transmit and receive simultaneously. The $\overline{OEBY}$ input controls the Y outputs. When $\overline{OEBY}$ is low, the Y outputs are active. When $\overline{OEBY}$ is high, the Y outputs are disabled.

The polarity-control (T/$\overline{C}$) input is provided to select polarity of data transmission in both directions. When T/$\overline{C}$ is high, data transmission is true, and A data goes to the B bus and B data goes to the Y bus. When T/$\overline{C}$ is low, data transmission is complementary, and $\overline{A}$ data goes to the B bus and $\overline{B}$ data goes to the Y bus.

Function Tables

OUTPUT ENABLE

INPUTS			OPERATION OR FUNCTION	MODE
T/$\overline{C}$	$\overline{OEAB}$	$\overline{OEBY}$		
X	H	H	Z	Isolation
H	L	H	A data to B bus	True driver
H	H	L	B data to Y bus	True driver
H	L	L	A data to B bus, B data to Y bus	True transceiver
L	L	H	$\overline{A}$ data to B bus	Inverted driver
L	H	L	$\overline{B}$ data to Y bus	Inverted driver
L	L	L	$\overline{A}$ data to B bus, $\overline{B}$ data to Y bus	Inverted transceiver

OUTPUT EDGE-RATE CONTROL ($\overline{ERC}$)

INPUT $\overline{ERC}$		OUTPUT B-PORT EDGE RATE
LOGIC LEVEL	NOMINAL VOLTAGE	
L	GND	Slow
H	V_{CC}	Fast

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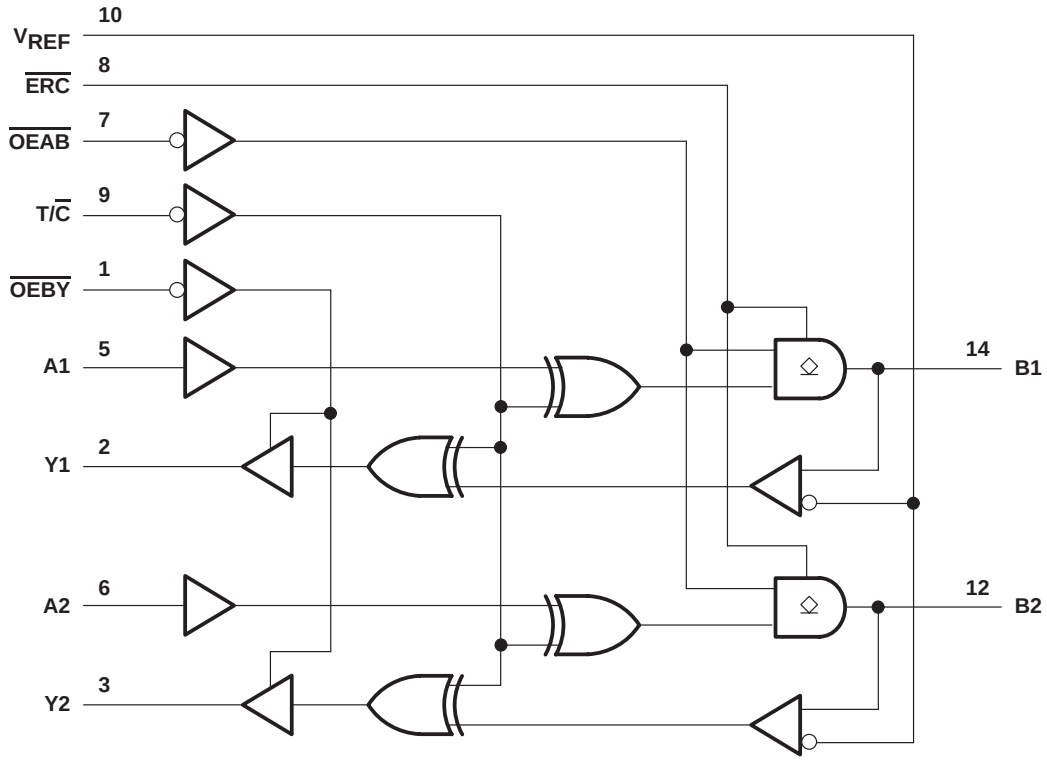
logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} and BIAS V_{CC} . . . . . –0.5 V to 4.6 V
Input voltage range, V_I (see Note 1): A and control inputs . . . . . –0.5 V to 7 V
B port, $\overline{ERC}$, and V_{REF} . . . . . –0.5 V to 4.6 V
Voltage range applied to any output in the high-impedance or power-off state, V_O
(see Note 1): Y . . . . . –0.5 V to 7 V
B port . . . . . –0.5 V to 4.6 V
Voltage range applied to any output in the high or low state, V_O
(see Note 1): Y . . . . . –0.5 V to V_{CC} + 0.5 V
B port . . . . . –0.5 V to 4.6 V
Current into any output in the low state, I_O: Y . . . . . 48 mA
B port . . . . . 200 mA
Current into any output in the high state, I_O (see Note 2) . . . . . 48 mA
Continuous current through each V_{CC} or GND . . . . . ±100 mA
Input clamp current, I_{IK} (V_I < 0) . . . . . –50 mA
Output clamp current, I_{OK} (V_O < 0) . . . . . –50 mA
Package thermal impedance, θ_{JA} (see Note 3): D package . . . . . 73°C/W
DGV package . . . . . 120°C/W
PW package . . . . . 108°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JESD 51.

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recommended operating conditions (see Notes 4 through 6)

			MIN	NOM	MAX	UNIT
V_{CC}, BIAS V_{CC}	Supply voltage		3.15	3.3	3.45	V
V_{TT}	Termination voltage	GTL	1.14	1.2	1.26	V
		GTL+	1.35	1.5	1.65	
V_{REF}	Supply voltage	GTL	0.74	0.8	0.87	V
		GTL+	0.87	1	1.1	
V_I	Input voltage	B port			V_{TT}	V
		Except B port			V_{CC}	
V_{IH}	High-level input voltage	B port	V_{REF}+0.05			V
		$\overline{ERC}$	V_{CC}–0.6	V_{CC}		
		Except B port and $\overline{ERC}$	2			
V_{IL}	Low-level input voltage	B port			V_{REF}–0.05	V
		$\overline{ERC}$		GND	0.6	
		Except B port and $\overline{ERC}$			0.8	
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current	Y			–24	mA
I_{OL}	Low-level output current	Y			24	mA
		B port			100	
T_A	Operating free-air temperature		–40		85	°C

NOTES: 4. All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

5. Normal connection sequence is GND first, BIAS V_{CC} = 3.3 V second, and V_{CC} = 3.3 V, I/O, control inputs, V_{TT} and V_{REF} (any order) last. However, if the B-port I/O precharge is not required, the acceptable connection sequence is GND first and V_{CC} = 3.3 V, BIAS V_{CC} = 3.3 V, I/O, control inputs, V_{TT} and V_{REF} (any order) last. When V_{CC} is connected, the BIAS V_{CC} circuitry is disabled.

6. V_{TT} and R_{TT} can be adjusted to accommodate backplane impedances as long as they do not exceed the DC absolute I_{OL} ratings. Similarly, V_{REF} can be adjusted to optimize noise margins, but normally is 2/3 V_{TT}.

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electrical characteristics over recommended operating free-air temperature range for GTL+ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 3.15 V,	I_I = –18 mA			–1.2	V
V_{OH}	Y	V_{CC} = 3.15 V to 3.45 V,	I_{OH} = –100 µA	V_{CC}–0.2			V
		V_{CC} = 3.15 V	I_{OH} = –12 mA	2.4			
			I_{OH} = –24 mA	2			
V_{OL}	Y	V_{CC} = 3.15 V to 3.45 V,	I_{OL} = 100 µA			0.2	V
		V_{CC} = 3.15 V	I_{OL} = 12 mA			0.4	
			I_{OL} = 24 mA			0.5	
	B port	V_{CC} = 3.15 V	I_{OL} = 10 mA			0.2	
			I_{OL} = 64 mA			0.4	
			I_{OL} = 100 mA			0.55	
I_I‡	B port	V_{CC} = 3.45 V,	V_I = 0 to 1.5 V			±5	µA
	A and control inputs	V_{CC} = 3.45 V	V_I = 0 to V_{CC}			±5	
			V_I = 5.5 V			±5	
I_{CC}	Y or B port	V_{CC} = 3.45 V, I_O = 0, V_I (A or control input) = V_{CC} or GND, V_I (B port) = V_{TT} or GND	Outputs high			20	mA
			Outputs low			20	
			Outputs disabled			20	
ΔI_{CC}§		V_{CC} = 3.45 V, One A or control input at V_{CC} – 0.6 V, Other A or control inputs at V_{CC} or GND				1.5	mA
C_i	A	V_I = 3.15 V or 0					pF
	Control inputs						
C_o	Y	V_O = 3.15 V or 0					pF
C_{io}	B port	V_O = 1.5 V or 0					pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For I/O ports, the parameter I_I includes the off-state output leakage current.
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

live-insertion specifications for A and Y over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS			MIN	MAX	UNIT
I_{off}	V_{CC} = 0,	BIAS V_{CC} = 0,	V_I or V_O = 0 to 5.5 V		100	µA
I_{OZPU}	V_{CC} = 0 to 1.5 V,	V_O = 0.5 V to 3 V,	$\overline{OE}$ = 0		±100	µA
I_{OZPD}	V_{CC} = 1.5 V to 0,	V_O = 0.5 V to 3 V,	$\overline{OE}$ = 0		±100	µA

live-insertion specifications for B port over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS			MIN	MAX	UNIT
I_{off}	V_{CC} = 0,	BIAS V_{CC} = 0,	V_I or V_O = 0 to 1.5 V		100	µA
I_{OZPU}	V_{CC} = 0 to 1.5 V,	V_O = 0.5 V to 1.5 V,	$\overline{OE}$ = 0		±100	µA
I_{OZPD}	V_{CC} = 1.5 V to 0,	V_O = 0.5 V to 1.5 V,	$\overline{OE}$ = 0		±100	µA
I_{CC} (BIAS V_{CC})	V_{CC} = 0 to 3.15 V	BIAS V_{CC} = 3.15 V to 3.45 V,	V_O (B port) = 0 to 1.5 V		5	mA
	V_{CC} = 3.15 V to 3.45 V				10	µA
V_O	V_{CC} = 0,	BIAS V_{CC} = 3.3 V		0.95	1.05	V
I_O	V_{CC} = 0,	BIAS V_{CC} = 3.15 V to 3.45 V,	V_O (B port) = 0.6 V	–1		µA

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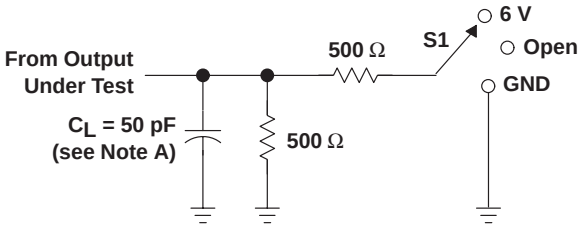
switching characteristics over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.5 V and V_{REF} = 1 V for GTL+ (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	EDGE RATE†	MIN	TYP‡	MAX	UNIT
t_{pd}	A	B	Slow				ns
			Fast				
		Y	Slow				
			Fast				
	T/$\overline{C}$	B	Slow				
			Fast				
t_{en}	$\overline{OEAB}$	B	Slow				ns
t_{dis}							
t_{en}	$\overline{OEAB}$	B	Fast				ns
t_{dis}							
t_r	Rise time, B outputs (0.6 V to 1.3 V)		Slow				ns
			Fast				
t_f	Fall time, B outputs (1.3 V to 0.6 V)		Slow				ns
			Fast				
t_{pd}	B	Y					ns
	T/$\overline{C}$						
t_{en}	$\overline{OEBY}$	Y					ns
t_{dis}							

† Slow ($\overline{ERC}$ = GND) and Fast ($\overline{ERC}$ = V_{CC})
‡ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

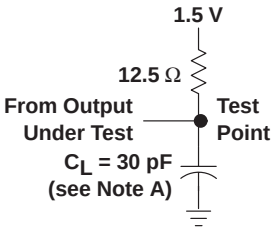
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

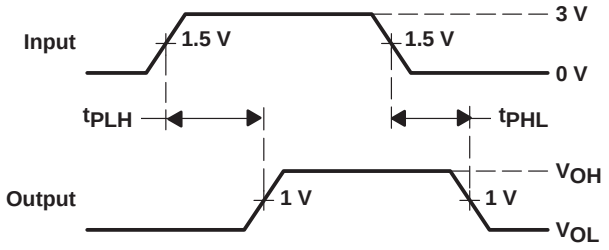


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

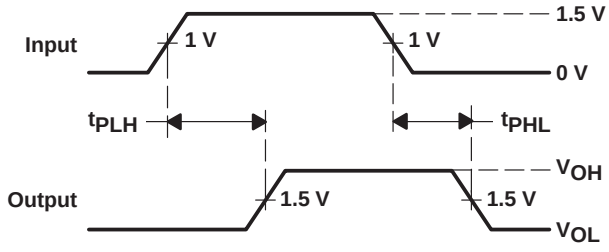
LOAD CIRCUIT FOR Y OUTPUTS



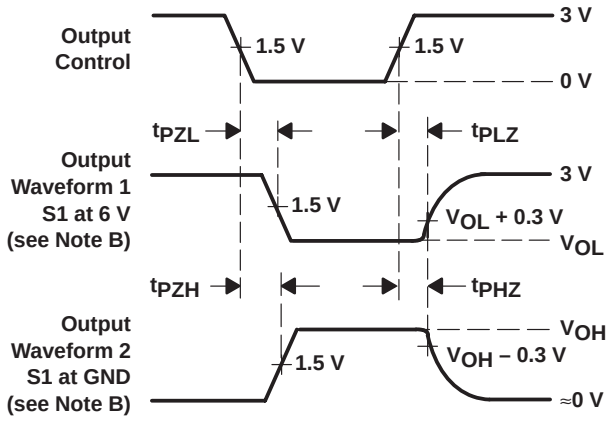
LOAD CIRCUIT FOR B OUTPUTS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(A to B port)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(B port to Y)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
(A)

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, slew rate ≤ 1 V/ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

DISTRIBUTED-LOAD BACKPLANE SWITCHING CHARACTERISTICS

This data sheet is specified for and tested to the lump load shown in Figure 1. However, the designer probably uses this GTLP device in a distributed load like that shown in Figure 2, in which actual B-port backplane switching characteristics are different. Therefore, the device is modeled as shown in Figure 3, which very closely matches the results obtained using Figure 2. Switching characteristics based on Figure 3 more closely match actual backplane design requirements.

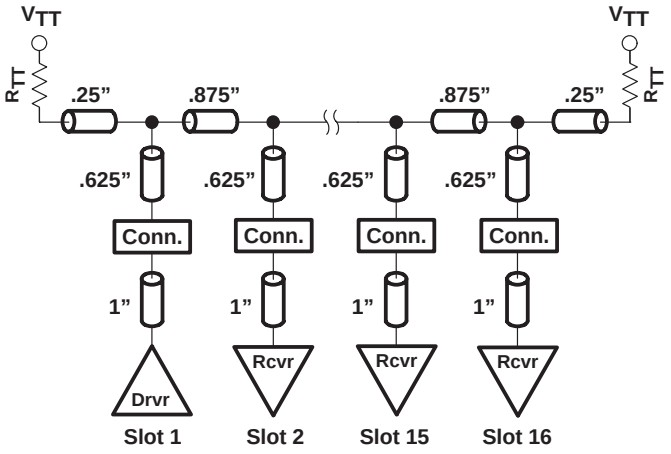


Figure 2. Test Backplane Model

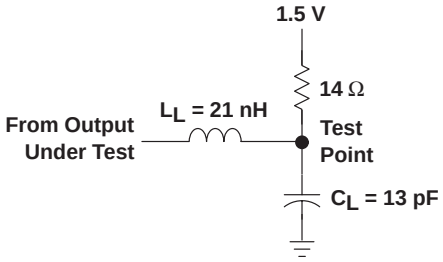


Figure 3. Distributed-Load Circuit for B Outputs

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.5 V and V_{REF} = 1 V for GTL+ (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	EDGE RATE†	MIN	TYP‡	MAX	UNIT
t_{pd}	A	B	Slow				ns
			Fast				
		Y	Slow				
			Fast				
	T/C	B	Slow				
			Fast				
t_{en}	$\overline{OEAB}$	B	Slow				ns
t_{dis}							
t_{en}	$\overline{OEAB}$	B	Fast				ns
t_{dis}							
t_r	Rise time, B outputs (0.6 V to 1.3 V)		Slow				ns
			Fast				
t_f	Fall time, B outputs (1.3 V to 0.6 V)		Slow				ns
			Fast				

† Slow ($\overline{ERC}$ = GND) and Fast ($\overline{ERC}$ = V_{CC})
‡ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

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