

High Supply Voltage 220MHz Unity-Gain Stable Operational Amplifiers

The ISL55002 and ISL55004 are high speed, low power, low cost monolithic operational amplifiers. The ISL55002 and ISL55004 are unity-gain stable and feature a 300V/ μ s slew rate and 220MHz bandwidth while requiring only 9mA of supply current.

The power supply operating range of the ISL55002 and ISL55004 is from ± 15 V down to ± 2.5 V. For single-supply operation, the ISL55002 and ISL55004 operate from 30V down to 5V.

The ISL55002 and ISL55004 also feature an extremely wide output voltage swing of -12.75 V/ $+13.4$ V with $V_S = \pm 15$ V and $R_L = 1$ k Ω .

At a gain of +1, the ISL55002 and ISL55004 have a -3dB bandwidth of 220MHz with a phase margin of 50°. Because of its conventional voltage-feedback topology, the ISL55002 and ISL55004 allow the use of reactive or non-linear elements in its feedback network. This versatility combined with low cost and 140mA of output-current drive makes the ISL55002 and ISL55004 an ideal choice for price-sensitive applications requiring low power and high speed.

The ISL55002 is available in an 8-pin SO package and the ISL55004 in a 14-pin SO (0.150") package. All are specified for operation over the full -40° C to $+85^\circ$ C temperature range.

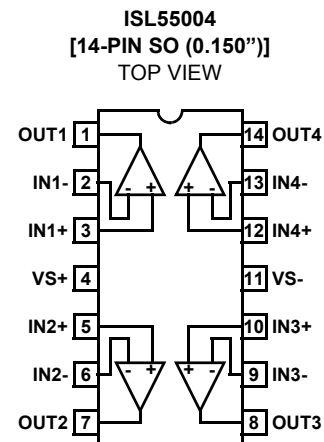
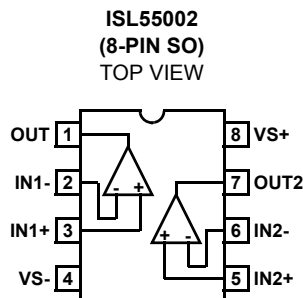
Features

- 220MHz -3dB bandwidth
- Unity-gain stable
- Low supply current: 9mA @ $V_S = \pm 15$ V
- Wide supply range: ± 2.5 V to ± 15 V dual-supply and 5V to 30V single-supply
- High slew rate: 300V/ μ s
- Fast settling: 75ns to 0.1% for a 10V step
- Wide output voltage swing: -12.75 V/ $+13.6$ V with $V_S = \pm 15$ V, $R_L = 1$ k Ω
- Low cost, enhanced replacement for the AD847 and LM6361
- Pb-free plus anneal available (RoHS compliant)

Applications

- Video amplifiers
- Single-supply amplifiers
- Active filters/integrators
- High speed sample-and-hold
- High speed signal processing
- ADC/DAC buffers
- Pulse/RF amplifiers
- Pin diode receivers
- Log amplifiers
- Photo multiplier amplifiers
- Difference amplifiers

Pinouts



Ordering Information

| PART NUMBER | PACKAGE | TAPE & REEL | PKG. DWG. # |
|-------------------------------|------------------------------------|-------------|-------------|
| ISL55002IB | 8-Pin SO | - | M8.15 |
| ISL55002IB-T7 | 8-Pin SO | 7" | M8.15 |
| ISL55002IB-T13 | 8-Pin SO | 13" | M8.15 |
| ISL55002IBZ (See Note) | 8-Pin SO (Pb-Free) | - | M8.15 |
| ISL55002IBZ-T7 (See Note) | 8-Pin SO (Pb-Free) | 7" | M8.15 |
| ISL55002IBZ-T13 (See Note) | 8-Pin SO (Pb-Free) | 13" | M8.15 |
| ISL55004IB | 14-Pin SO (0.150") | - | M14.15 |
| ISL55004IB-T7 | 14-Pin SO (0.150") | 7" | M14.15 |
| ISL55004IB-T13 | 14-Pin SO (0.150") | 13" | M14.15 |
| ISL55004IBZ (See Note) | 14-Pin SO (0.150") (Pb-Free) | - | M14.15 |
| ISL55004IBZ-T7 (See Note) | 14-Pin SO (0.150") (Pb-Free) | 7" | M14.15 |
| ISL55004IBZ-T13 (See Note) | 14-Pin SO (0.150") (Pb-Free) | 13" | M14.15 |

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

ISL55002, ISL55004

Absolute Maximum Ratings (T_A = 25°C)

| | | | |
|--|-----------------|--|-----------------|
| Supply Voltage (V _S) | ±16.5V or 33V | Power Dissipation (P _D) | See Curves |
| Input Voltage (V _{IN}) | ±V _S | Operating Temperature Range (T _A) | -40°C to +85°C |
| Differential Input Voltage (dV _{IN}) | ±10V | Operating Junction Temperature (T _J) | +150°C |
| Continuous Output Current | 60mA | Storage Temperature (T _{ST}) | -65°C to +150°C |

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: T_J = T_C = T_A

DC Electrical Specifications V_S = ±15V, R_L = 1kΩ, T_A = 25°C, unless otherwise specified.

| PARAMETER | DESCRIPTION | CONDITION | MIN | TYP | MAX | UNIT |
|-------------------|---------------------------------------|--|-------|--------|-----|-------|
| V _{OS} | Input Offset Voltage | V _S = ±15V | | 1.2 | 5 | mV |
| TCV _{OS} | Average Offset Voltage Drift | | | | | μV/°C |
| I _B | Input Bias Current | V _S = ±15V | | 0.6 | 3.5 | μA |
| I _{OS} | Input Offset Current | V _S = ±15V | | 0.2 | 2 | μA |
| TCI _{OS} | Average Offset Current Drift (Note 1) | | | TBD | | nA/°C |
| A _{VOL} | Open-loop Gain | V _S = ±15V, V _{OUT} = ±10V, R _L = 1kΩ | 12000 | 21000 | | V/V |
| PSRR | Power Supply Rejection Ratio | V _S = ±5V to ±15V | 75 | 100 | | dB |
| CMRR | Common-mode Rejection Ratio | V _{CM} = ±10V, V _{OUT} = 0V | 75 | 90 | | dB |
| CMIR | Common-mode Input Range | V _S = ±15V | | 13 | | V |
| V _{OUT} | Output Voltage Swing | V _{O+} , R _L = 1kΩ | 13.3 | 13.4 | | V/V |
| | | V _{O-} , R _L = 1kΩ | -12.6 | -12.75 | | V/V |
| | | V _{O+} , R _L = 150Ω | 9.6 | 10.7 | | V/V |
| | | V _{O-} , R _L = 150Ω | -6.5 | -8.2 | | V/V |
| I _{SC} | Output Short Circuit Current | T _A = 25°C | 80 | 140 | | mA |
| I _S | Supply Current (per amplifier) | V _S = ±15V, no load | | 9 | 9.5 | mA |
| R _{IN} | Input Resistance | | 2.0 | 3.2 | | MΩ |
| C _{IN} | Input Capacitance | A _V = +1 @10MHz | | 1 | | pF |
| R _{OUT} | Output Resistance | A _V = +1 | | 50 | | mΩ |
| PSOR | Power Supply Operating Range | Dual supply | ±2.25 | | ±15 | V |
| | | Single supply | 4.5 | | 30 | V |

NOTE:

1. Measured from T_{MIN} to T_{MAX}.

AC Electrical Specifications V_S = ±15V, A_V = +1, R_L = 1kΩ unless otherwise specified.

| PARAMETER | DESCRIPTION | CONDITION | MIN | TYP | MAX | UNIT |
|-----------|---|--|-----|-----|-----|------|
| BW | -3dB Bandwidth (V _{OUT} = 0.4V _{PP}) | V _S = ±15V, A _V = +1 | | 220 | | MHz |
| | | V _S = ±15V, A _V = -1 | | 55 | | MHz |
| | | V _S = ±15V, A _V = +2 | | 53 | | MHz |
| | | V _S = ±15V, A _V = +5 | | 17 | | MHz |
| GBWP | Gain Bandwidth Product | V _S = ±15V | | 70 | | MHz |
| PM | Phase Margin | R _L = 1kΩ, C _L = 5pF | | 55 | | ° |

AC Electrical Specifications $V_S = \pm 15V, A_V = +1, R_L = 1k\Omega$ unless otherwise specified. (Continued)

| PARAMETER | DESCRIPTION | CONDITION | MIN | TYP | MAX | UNIT |
|-----------|----------------------------------|---------------------------|-----|------|-----|-----------------|
| SR | Slew Rate (Note 1) | | 260 | 300 | | V/ μ s |
| FPBW | Full-power Bandwidth (Note 2) | $V_S = \pm 15V$ | | 9.5 | | MHz |
| t_S | Settling to +0.1% ($A_V = +1$) | $V_S = \pm 15V, 10V$ step | | 75 | | ns |
| dG | Differential Gain (Note 3) | NTSC/PAL | | 0.01 | | % |
| dP | Differential Phase | NTSC/PAL | | 0.05 | | $^\circ$ |
| eN | Input Noise Voltage | 10kHz | | 12 | | nV/ \sqrt{Hz} |
| iN | Input Noise Current | 10kHz | | 1.5 | | pA/ \sqrt{Hz} |

NOTES:

1. Slew rate is measured on rising edge.
2. For $V_S = \pm 15V, V_{OUT} = 10V_{PP}$, for $V_S = \pm 5V, V_{OUT} = 5V_{PP}$. Full-power bandwidth is based on slew rate measurement using $FPBW = SR / (2\pi * V_{PEAK})$.
3. Video performance measured at $V_S = \pm 15V, A_V = +2$ with two times normal video level across $R_L = 150\Omega$. This corresponds to standard video levels across a back-terminated 75Ω load. For other values of R_L , see curves.

Typical Performance Curves

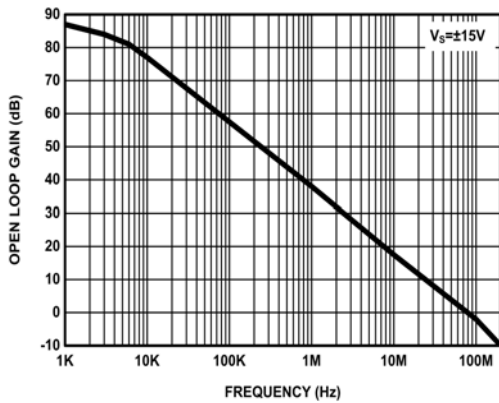


FIGURE 1. OPEN-LOOP GAIN vs FREQUENCY

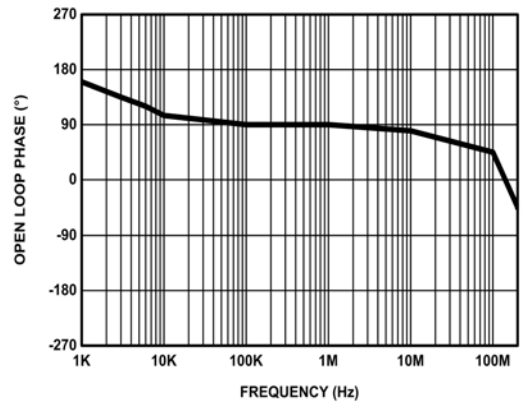


FIGURE 2. OPEN-LOOP PHASE vs FREQUENCY

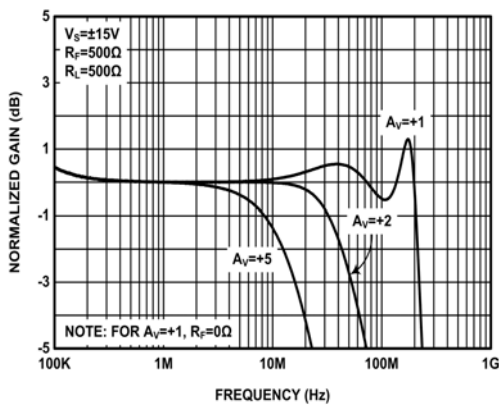


FIGURE 3. GAIN vs FREQUENCY FOR VARIOUS NON-INVERTING GAIN SETTINGS

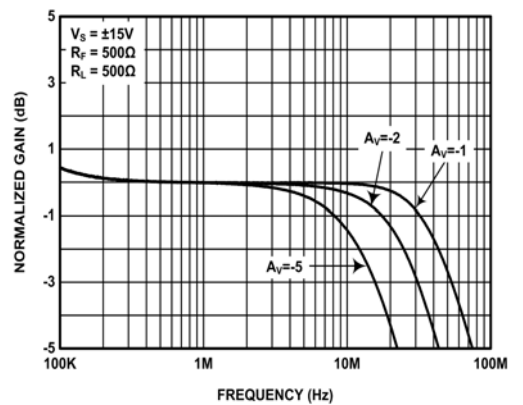


FIGURE 4. GAIN vs FREQUENCY FOR VARIOUS INVERTING GAIN SETTINGS

Typical Performance Curves

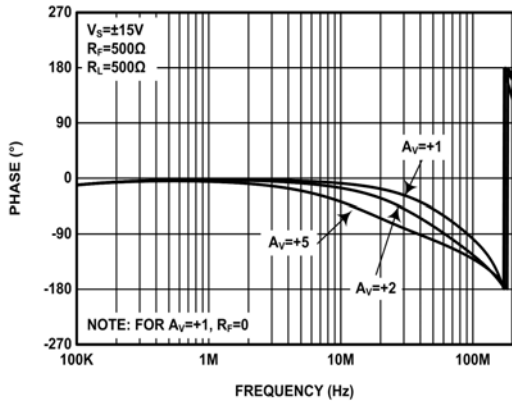


FIGURE 5. PHASE vs FREQUENCY FOR VARIOUS NON-INVERTING GAIN SETTINGS

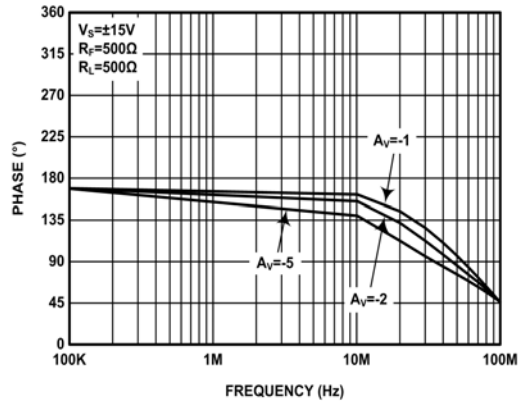


FIGURE 6. PHASE vs FREQUENCY FOR VARIOUS INVERTING GAIN SETTINGS

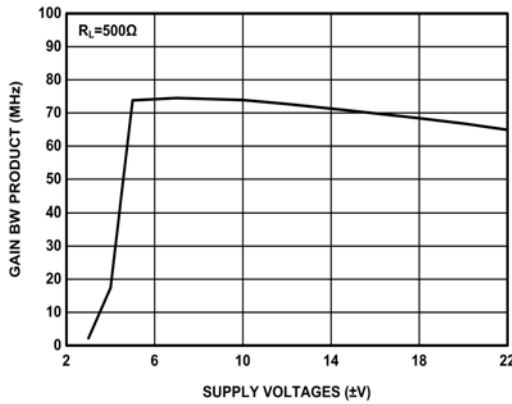


FIGURE 7. GAIN BANDWIDTH PRODUCT vs SUPPLY

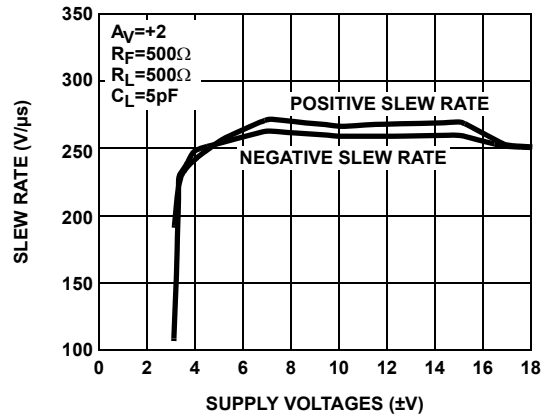


FIGURE 8. SLEW RATE vs SUPPLY

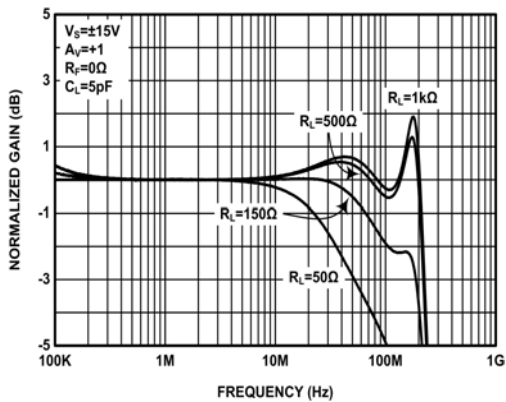


FIGURE 9. GAIN vs FREQUENCY FOR VARIOUS R_{LOAD} ($A_V = +1$)

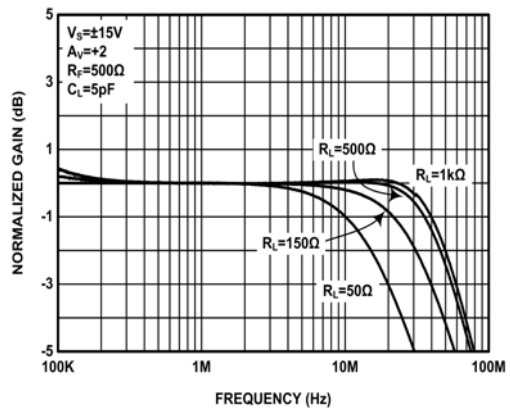


FIGURE 10. GAIN vs FREQUENCY FOR VARIOUS R_{LOAD} ($A_V = +2$)

Typical Performance Curves

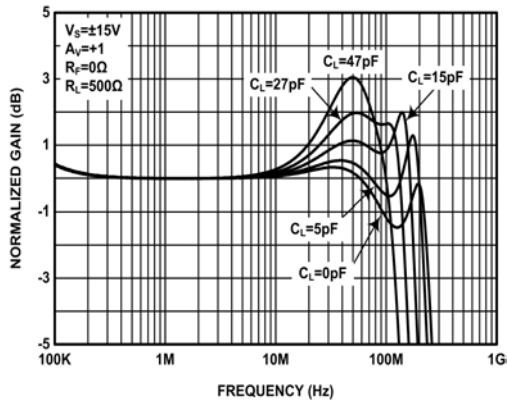


FIGURE 11. GAIN vs FREQUENCY FOR VARIOUS C_{LOAD} ($A_V = +1$)

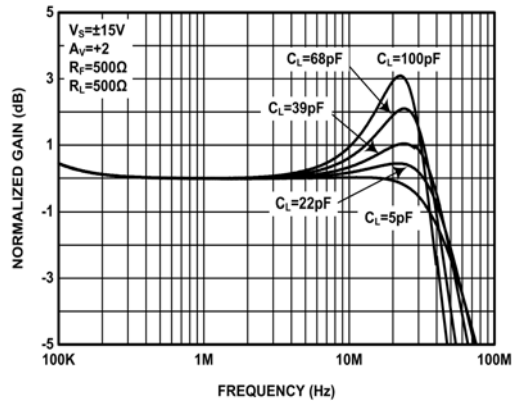


FIGURE 12. GAIN vs FREQUENCY FOR VARIOUS C_{LOAD} ($A_V = +2$)

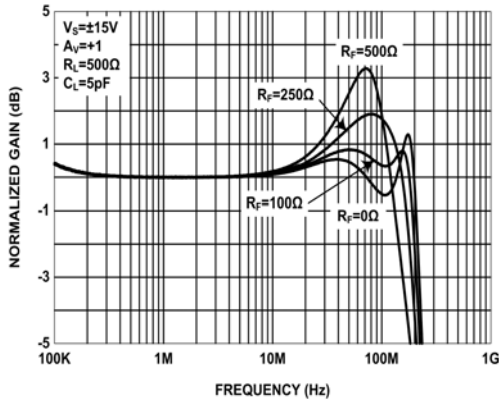


FIGURE 13. GAIN vs FREQUENCY FOR VARIOUS $R_{FEEDBACK}$ ($A_V = +1$)

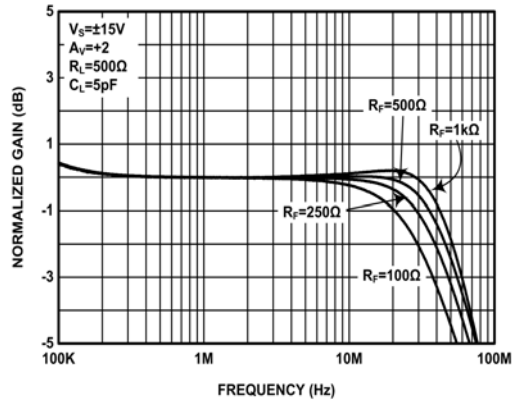


FIGURE 14. GAIN vs FREQUENCY FOR VARIOUS $R_{FEEDBACK}$ ($A_V = +2$)

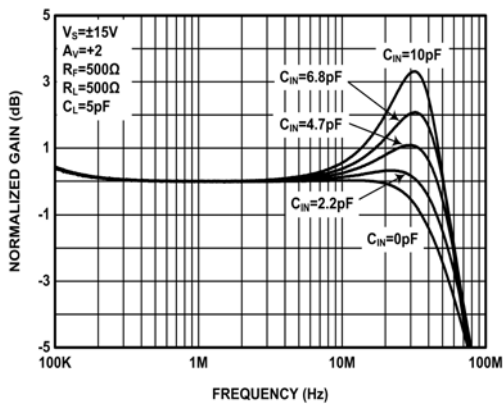


FIGURE 15. GAIN vs FREQUENCY FOR VARIOUS INVERTING INPUT CAPACITANCE (C_{IN})

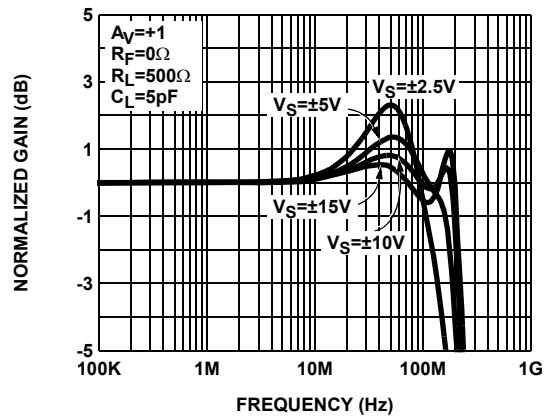


FIGURE 16. GAIN vs FREQUENCY FOR VARIOUS SUPPLY SETTINGS

Typical Performance Curves

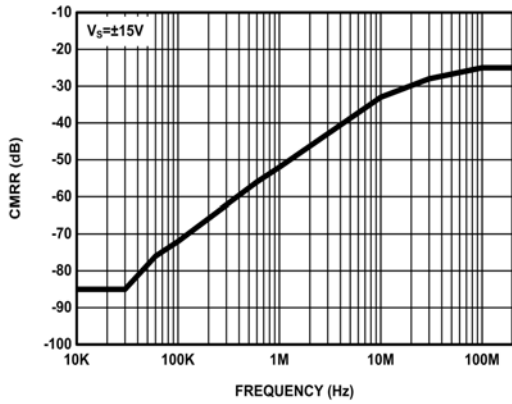


FIGURE 17. COMMON-MODE REJECTION RATIO (CMRR)

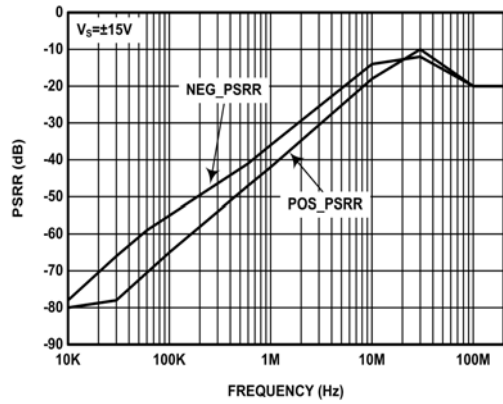


FIGURE 18. POWER SUPPLY REJECTION RATIO (PSRR)

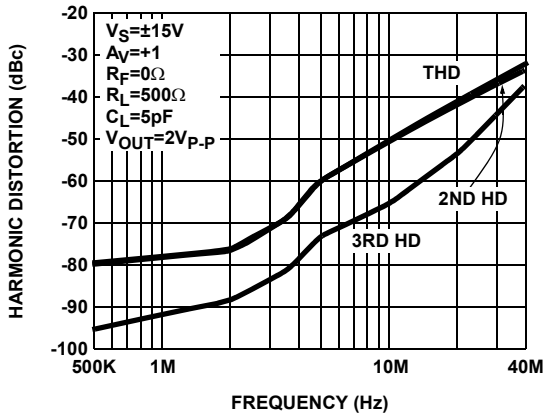


FIGURE 19. HARMONIC DISTORTION vs FREQUENCY ($A_V = +1$)

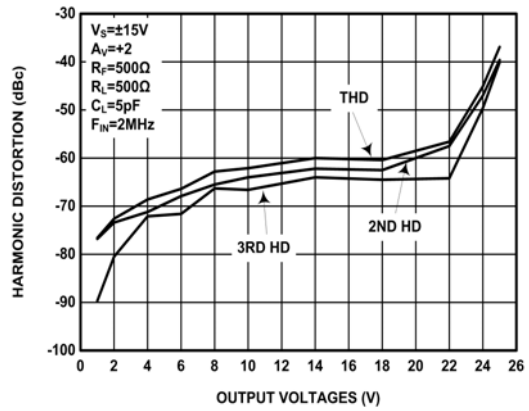


FIGURE 20. HARMONIC DISTORTION vs OUTPUT VOLTAGE ($A_V = +2$)

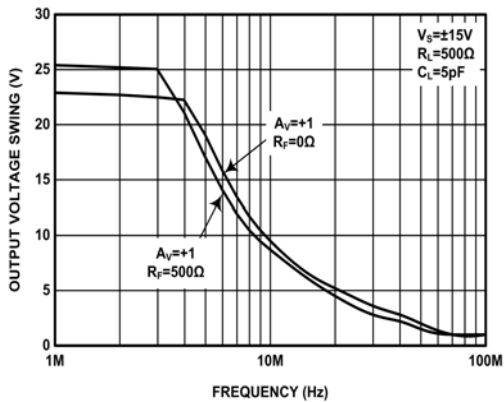


FIGURE 21. OUTPUT SWING vs FREQUENCY FOR VARIOUS GAIN SETTINGS

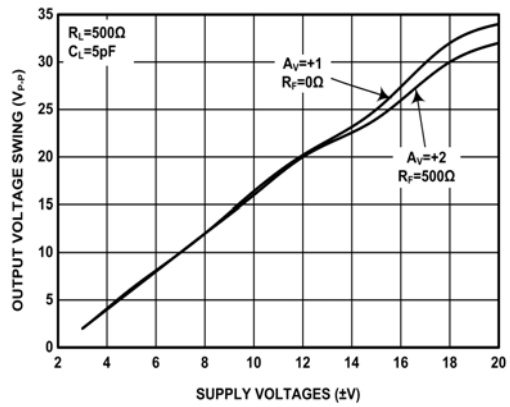


FIGURE 22. OUTPUT SWING vs SUPPLY VOLTAGE FOR VARIOUS GAIN SETTINGS

Typical Performance Curves

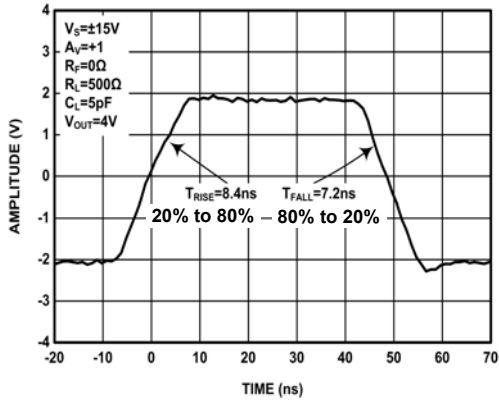


FIGURE 23. LARGE SIGNAL RISE AND FALL TIMES

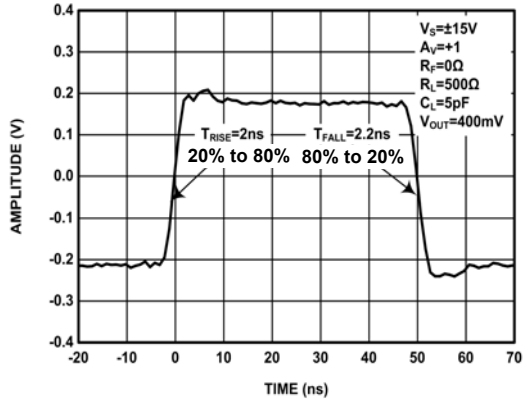


FIGURE 24. SMALL SIGNAL RISE AND FALL TIMES

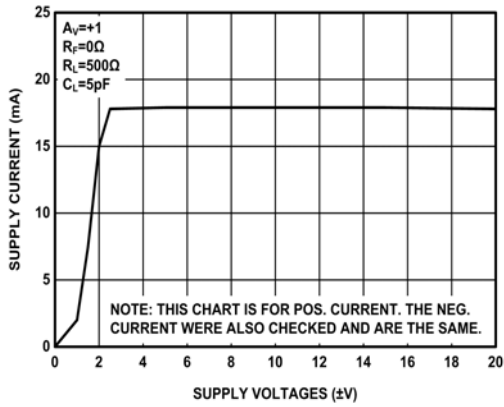


FIGURE 25. SUPPLY CURRENT vs SUPPLY VOLTAGE

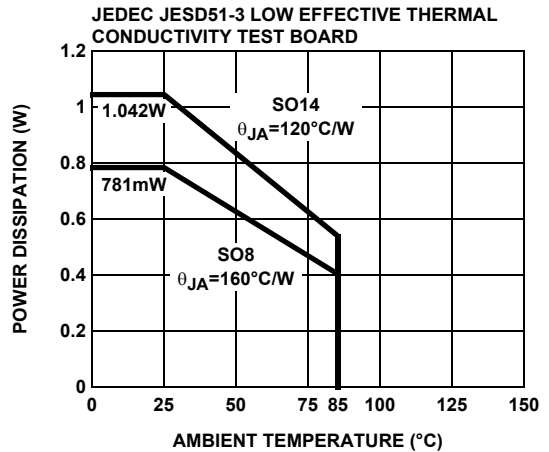


FIGURE 26. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

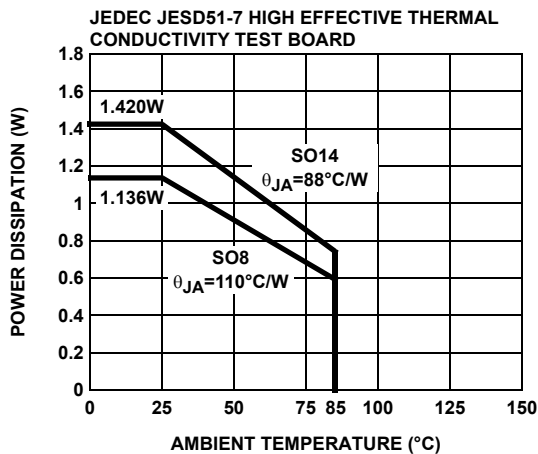


FIGURE 27. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

Product Description

The ISL55002 and ISL55004 are wide bandwidth, low power, and low offset voltage feedback operational amplifiers. These devices are internally compensated for closed loop gain of +1 or greater. Connected in voltage follower mode and driving a 500Ω load, the -3dB bandwidth is around a 220MHz. Driving a 150Ω load and a gain of 2, the bandwidth is about 90MHz while maintaining a 300V/μs slew rate.

The ISL55002 and ISL55004 are designed to operate with supply voltage from +15V to -15V. That means for single supply application, the supply voltage is from 0V to 30V. For split supplies application, the supply voltage is from ±15V. The amplifier has an input common-mode voltage range from 1.5V above the negative supply (V_{S-} pin) to 1.5V below the positive supply (V_{S+} pin). If the input signal is outside the above specified range, it will cause the output signal to be distorted.

The outputs of the ISL55002 and ISL55004 can swing from -12.75V to +13.4V for $V_S = \pm 15V$. As the load resistance becomes lower, the output swing is lower.

Choice Of Feedback Resistor And Gain Bandwidth Product

For applications that require a gain of +1, no feedback resistor is required. Just short the output pin to the inverting input pin. For gains greater than +1, the feedback resistor forms a pole with the parasitic capacitance at the inverting input. As this pole becomes smaller, the amplifier's phase margin is reduced. This causes ringing in the time domain and peaking in the frequency domain. Therefore, R_F can't be very big for optimum performance. If a large value of R_F must be used, a small capacitor in the few Pico farad range in parallel with R_F can help to reduce the ringing and peaking at the expense of reducing the bandwidth. For gain of +1, $R_F = 0$ is optimum. For the gains other than +1, optimum response is obtained with R_F with proper selection of R_F and R_G (see Figures 15 and 16 for selection.)

Video Performance

For good video performance, an amplifier is required to maintain the same output impedance and the same frequency response as DC levels are changed at the output. This is especially difficult when driving a standard video load of 150Ω, because of the change in output current with DC level. The dG and dP of this device is about 0.01% and 0.05°, while driving 150Ω at a gain of 2. Driving high impedance loads would give a similar or better dG and dP performance.

Driving Capacitive Loads and Cables

The ISL55002 and ISL55004 can drive 47pF loads in parallel with 500Ω with less than 3dB of peaking at gain of +1 and as much as 100pF at a gain of +2 with under 3dB of peaking. If less peaking is desired in applications, a small series resistor

(usually between 5Ω to 50Ω) can be placed in series with the output to eliminate most peaking. However, this will reduce the gain slightly. If the gain setting is greater than 1, the gain resistor R_G can then be chosen to make up for any gain loss which may be created by the additional series resistor at the output.

When used as a cable driver, double termination is always recommended for reflection-free performance. For those applications, a back-termination series resistor at the amplifier's output will isolate the amplifier from the cable and allow extensive capacitive drive. However, other applications may have high capacitive loads without a back-termination resistor. Again, a small series resistor at the output can help to reduce peaking.

Output Drive Capability

The ISL55002 and ISL55004 do not have internal short circuit protection circuitry. They have a typical short circuit current of 140mA. If the output is shorted indefinitely, the power dissipation could easily overheat the die or the current could eventually compromise metal integrity. Maximum reliability is maintained if the output current never exceeds ±60mA. This limit is set by the design of the internal metal interconnect. Note that in transient applications, the part is robust.

Short circuit protection can be provided externally with a back match resistor in series with the output placed close as possible to the output pin. In video applications this would be a 75Ω resistor and will provide adequate short circuit protection to the device. Care should still be taken not to stress the device with a short at the output.

Power Dissipation

With the high output drive capability of the ISL55002 and ISL55004, it is possible to exceed the 150°C absolute maximum junction temperature under certain load current conditions. Therefore, it is important to calculate the maximum junction temperature for an application to determine if load conditions or package types need to be modified to assure operation of the amplifier in a safe operating area.

The maximum power dissipation allowed in a package is determined according to:

$$PD_{MAX} = \frac{T_{JMAX} - T_{AMAX}}{\theta_{JA}}$$

Where:

- T_{JMAX} = Maximum junction temperature
- T_{AMAX} = Maximum ambient temperature
- θ_{JA} = Thermal resistance of the package

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage, plus the power in the IC due to the load, or:

For sourcing:

$$PD_{MAX} = V_S \times I_{SMAX} + \sum_{i=1}^n (V_S - V_{OUTi}) \times \frac{V_{OUTi}}{R_{Li}}$$

For sinking:

$$PD_{MAX} = V_S \times I_{SMAX} + \sum_{i=1}^n (V_{OUTi} - V_S) \times I_{LOADi}$$

Where:

- V_S = Supply voltage
- I_{SMAX} = Maximum quiescent supply current
- V_{OUT} = Maximum output voltage of the application
- R_{LOAD} = Load resistance tied to ground
- I_{LOAD} = Load current
- N = number of amplifiers (max = 2)

By setting the two PD_{MAX} equations equal to each other, we can solve the output current and R_{LOAD} to avoid the device overheat.

Power Supply Bypassing Printed Circuit Board Layout

As with any high frequency device, a good printed circuit board layout is necessary for optimum performance. Lead lengths should be as short as possible. The power supply pin must be well bypassed to reduce the risk of oscillation. For normal single supply operation, where the V_{S-} pin is connected to the ground plane, a single 4.7 μ F tantalum capacitor in parallel with a 0.1 μ F ceramic capacitor from V_{S+} to GND will suffice. This same capacitor combination should be placed at each supply pin to ground if split supplies are to be used. In this case, the V_{S-} pin becomes the negative supply rail.

Printed Circuit Board Layout

For good AC performance, parasitic capacitance should be kept to minimum. Use of wire wound resistors should be avoided because of their additional series inductance. Use of sockets should also be avoided if possible. Sockets add parasitic inductance and capacitance that can result in compromised performance. Minimizing parasitic capacitance at the amplifier's inverting input pin is very important. The feedback resistor should be placed very close to the inverting input pin. Strip line design techniques are recommended for the signal traces.

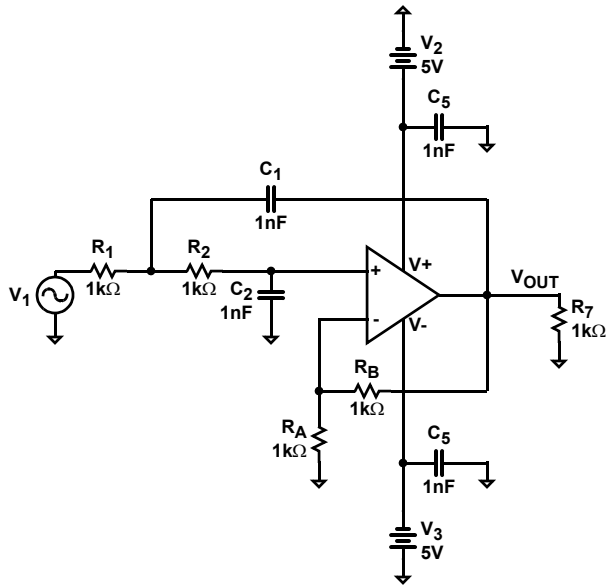
Application Circuits

Sullen Key Low Pass Filter

A common and easy to implement filter taking advantage of the wide bandwidth, low offset and low power demands of the ISL55002 and ISL55004. A derivation of the transfer function is provided for convenience (See Figure 28).

Sullen Key High Pass Filter

Again this useful filter benefits from the characteristics of the ISL55002 and ISL55004. The transfer function is very similar to the low pass so only the results are presented (See Figure 29).



$$K = 1 + \frac{R_B}{R_A}$$

$$V_o = K \frac{1}{R_2 C_2 s + 1} V_1$$

$$\frac{V_1 - V_i}{R_1} + \frac{K - V_1}{R_2} + \frac{V_o - V_i}{C_1 s} = 0$$

$$H(s) = \frac{K}{R_1 C_1 R_2 C_2 s^2 + ((1 - K)R_1 C_1 + R_1 C_2 + R_2 C_2)s + 1}$$

$$H(j\omega) = \frac{1}{1 - \omega^2 R_1 C_1 R_2 C_2 + j\omega((1 - K)R_1 C_1 + R_1 C_2 + R_2 C_2)}$$

$$H_{olp} = K$$

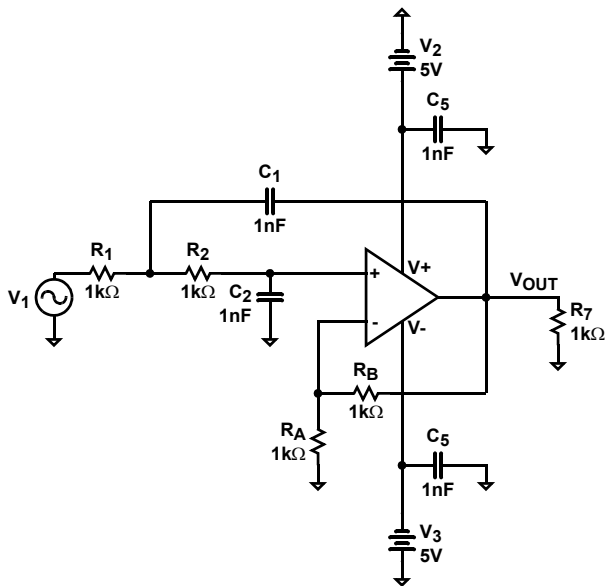
$$\omega_o = \frac{1}{\sqrt{R_1 C_1 R_2 C_2}}$$

$$Q = \frac{1}{(1 - K)\sqrt{\frac{R_1 C_1}{R_2 C_2}} + \sqrt{\frac{R_1 C_2}{R_2 C_1}} + \sqrt{\frac{R_2 C_2}{R_1 C_1}}}$$

$H_{olp} = K$
 $\omega_o = \frac{1}{RC}$
 $Q = \frac{1}{3 - K}$

Equations simplify if we let all components be equal $R=C$

FIGURE 28. SULLEN KEY LOW PASS FILTER



$H_{olp} = K$
 $\omega_o = \frac{1}{\sqrt{R_1 C_1 R_2 C_2}}$
 $Q = \frac{1}{(1 - K)\sqrt{\frac{R_1 C_1}{R_2 C_2}} + \sqrt{\frac{R_1 C_2}{R_2 C_1}} + \sqrt{\frac{R_2 C_2}{R_1 C_1}}}$

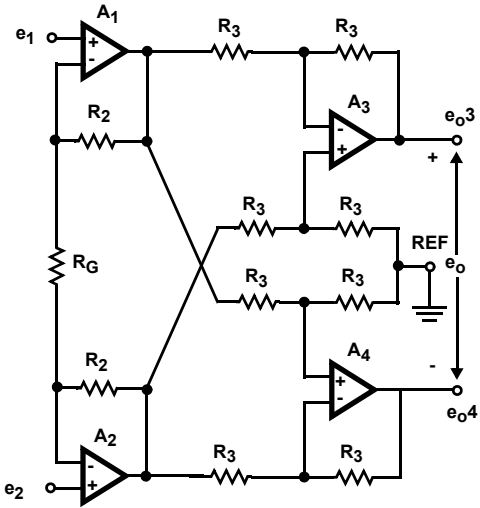
$H_{olp} = \frac{K}{4 - K}$
 $\omega_o = \frac{\sqrt{2}}{RC}$
 $Q = \frac{\sqrt{2}}{4 - K}$

Equations simplify if we let all components be equal $R=C$

FIGURE 29. SULLEN KEY HIGH PASS FILTER

Differential Output Instrumentation Amplifier

The addition of a third amplifier to the conventional three amplifier instrumentation amplifier introduces the benefits of differential signal realization, specifically the advantage of using common-mode rejection to remove coupled noise and ground potential errors inherent in remote transmission. This configuration also provides enhanced bandwidth, wider output swing and faster slew rate than conventional three amplifier solutions with only the cost of an additional amplifier and few resistors.



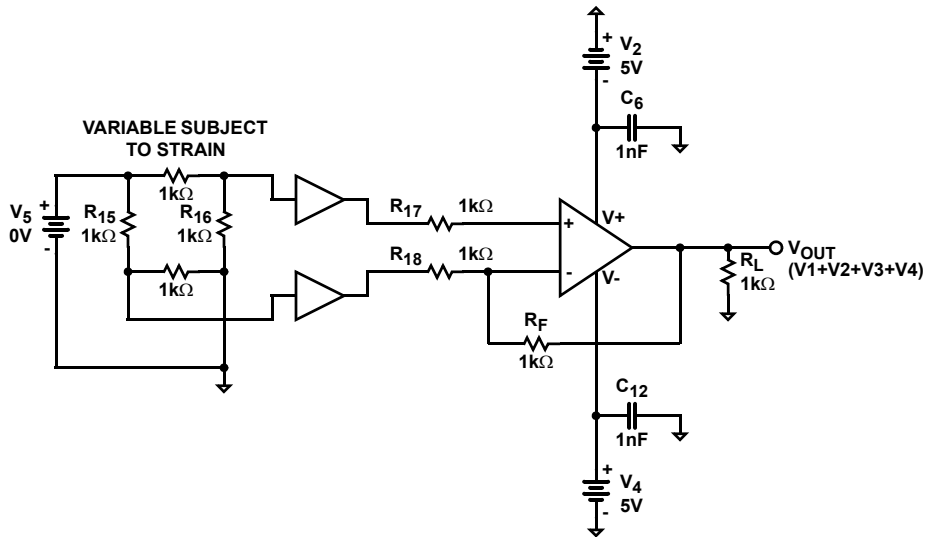
$$e_{o3} = -(1 + 2R_2/R_G)(e_1 - e_2) \quad e_{o4} = (1 + 2R_2/R_G)(e_1 - e_2)$$

$$e_o = -2(1 + 2R_2/R_G)(e_1 - e_2)$$

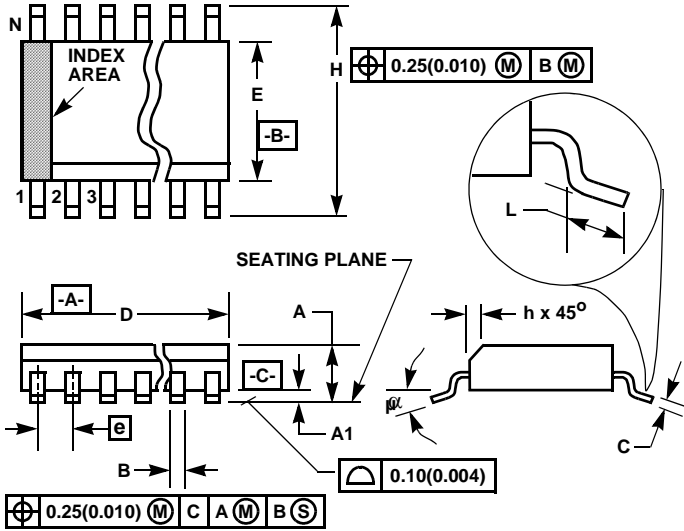
$$BW = \frac{2f_{C1,2}}{|A_{Di}|} \quad A_{Di} = -2(1 + 2R_2/R_G)$$

Strain Gauge

The strain gauge is an ideal application to take advantage of the moderate bandwidth and high accuracy of the ISL55002 and ISL55004. The operation of the circuit is very straightforward. As the strain variable component resistor in the balanced bridge is subjected to increasing strain, its resistance changes, resulting in an imbalance in the bridge. A voltage variation from the referenced high accuracy source is generated and translated to the difference amplifier through the buffer stage. This voltage difference as a function of the strain is converted into an output voltage.



Small Outline Plastic Packages (SOIC)



M8.15 (JEDEC MS-012-AA ISSUE C)
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

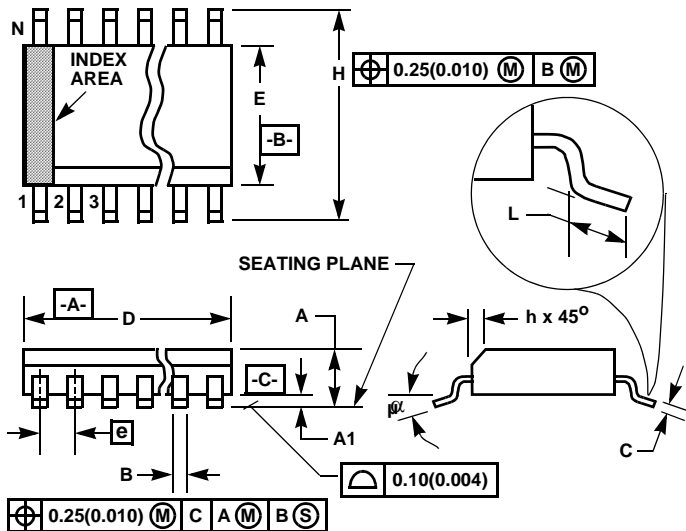
| SYMBOL | INCHES | | MILLIMETERS | | NOTES |
|----------|-----------|--------|-------------|------|-------|
| | MIN | MAX | MIN | MAX | |
| A | 0.0532 | 0.0688 | 1.35 | 1.75 | - |
| A1 | 0.0040 | 0.0098 | 0.10 | 0.25 | - |
| B | 0.013 | 0.020 | 0.33 | 0.51 | 9 |
| C | 0.0075 | 0.0098 | 0.19 | 0.25 | - |
| D | 0.1890 | 0.1968 | 4.80 | 5.00 | 3 |
| E | 0.1497 | 0.1574 | 3.80 | 4.00 | 4 |
| e | 0.050 BSC | | 1.27 BSC | | - |
| H | 0.2284 | 0.2440 | 5.80 | 6.20 | - |
| h | 0.0099 | 0.0196 | 0.25 | 0.50 | 5 |
| L | 0.016 | 0.050 | 0.40 | 1.27 | 6 |
| N | 8 | | 8 | | 7 |
| α | 0° | 8° | 0° | 8° | - |

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Rev. 0 12/93

Small Outline Plastic Packages (SOIC)



**M14.15 (JEDEC MS-012-AB ISSUE C)
14 LEAD NARROW BODY SMALL OUTLINE PLASTIC
PACKAGE**

| SYMBOL | INCHES | | MILLIMETERS | | NOTES |
|----------|-----------|--------|-------------|------|-------|
| | MIN | MAX | MIN | MAX | |
| A | 0.0532 | 0.0688 | 1.35 | 1.75 | - |
| A1 | 0.0040 | 0.0098 | 0.10 | 0.25 | - |
| B | 0.013 | 0.020 | 0.33 | 0.51 | 9 |
| C | 0.0075 | 0.0098 | 0.19 | 0.25 | - |
| D | 0.3367 | 0.3444 | 8.55 | 8.75 | 3 |
| E | 0.1497 | 0.1574 | 3.80 | 4.00 | 4 |
| e | 0.050 BSC | | 1.27 BSC | | - |
| H | 0.2284 | 0.2440 | 5.80 | 6.20 | - |
| h | 0.0099 | 0.0196 | 0.25 | 0.50 | 5 |
| L | 0.016 | 0.050 | 0.40 | 1.27 | 6 |
| N | 14 | | 14 | | 7 |
| α | 0° | 8° | 0° | 8° | - |

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

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