# 24LC04B/08B

4K/8K 2.5V I^{2}C™ Serial EEPROMs

FEATURES

- Single supply with operation down to 2.5V
- Low power CMOS technology
  - 1 mA active current typical
  - 10 µA standby current typical at 5.5V
  - 5 µA standby current typical at 3.0V
- Organized as two or four blocks of 256 bytes (2 x 256 x 8) and (4 x 256 x 8)
- 2-wire serial interface bus, I^{2}C™ compatible
- Schmitt trigger, filtered inputs for noise suppression
- Output slope control to eliminate ground bounce
- 100 kHz (2.5V) and 400 kHz (5V) compatibility
- Self-timed write cycle (including auto-erase)
- Page-write buffer for up to 16 bytes
- 2 ms typical write cycle time for page-write
- Hardware write protect for entire memory
- Can be operated as a serial ROM
- Factory programming (QTP) available
- ESD protection > 4,000V
- 1,000,000 erase/write cycles guaranteed
- Data retention > 200 years
- 8-pin DIP, 8-lead or 14-lead SOIC packages
- Available for extended temperature ranges
  - Commercial (C):   0°C to +70°C
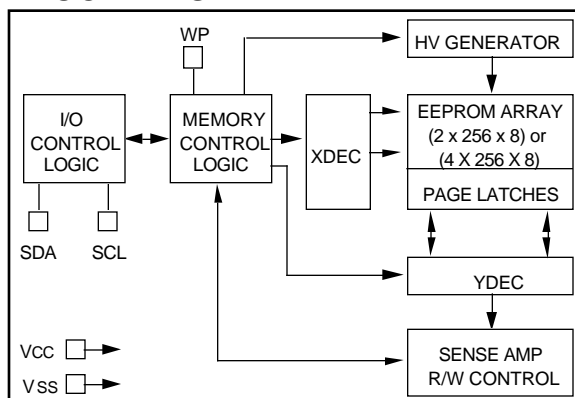 - Industrial (I):   -40°C to +85°C

DESCRIPTION

The Microchip Technology Inc. 24LC04B/08B is a 4K or 8K bit Electrically Erasable PROM. The device is organized as two or four blocks of 256 x 8-bit memory with a 2-wire serial interface. Low voltage design permits operation down to 2.5 volts with typical standby and active currents of only 5 µA and 1 mA respectively. The 24LC04B/08B also has a page-write capability for up to 16 bytes of data. The 24LC04B/08B is available in the standard 8-pin DIP and both 8-lead and 14-lead surface mount SOIC packages.
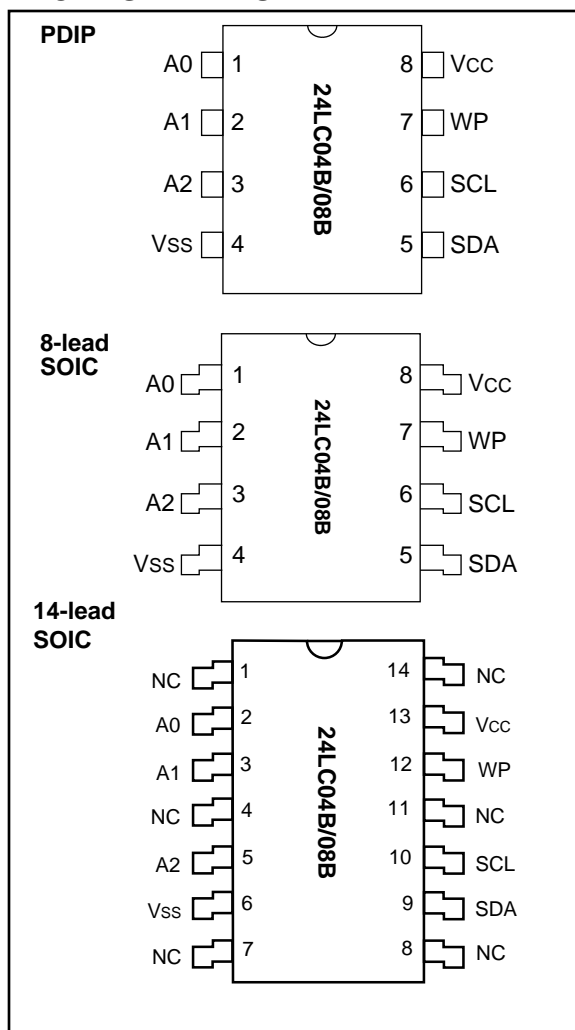
I^{2}C is a trademark of Philips Corporation.

PACKAGE TYPES

BLOCK DIAGRAM

24LC04B/08B

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

Vcc...7.0V
All inputs and outputs w.r.t. Vss .... -0.3V to Vcc + 1.0V
Storage temperature .... -65°C to +150°C
Ambient temp. with power applied .... -65°C to +125°C
Soldering temperature of leads (10 seconds) .... +300°C
ESD protection on all pins ....≥ 4 kV

*Notice: Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1:   PIN FUNCTION TABLE

Name	Function
Vss	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
WP	Write Protect Input
Vcc	+2.5V to 5.5V Power Supply
A0, A1, A2	**No Internal Connection**

TABLE 1-2:   DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Units	Vcc = +2.5V to +5.5V Commercial (C): Tamb = 0°C to +70°C Industrial (I): Tamb = -40°C to +85°C
WP, SCL and SDA pins:					
High level input voltage	V_{IH}	.7 Vcc	—	V	
Low level input voltage	V_{IL}	—	.3 Vcc	V	
Hysteresis of Schmitt trigger Inputs	V_{HYS}	.05 Vcc	—	V	(Note)
Low level output voltage	V_{OL}	—	.40	V	I_{OL} = 3.0mA, Vcc = 2.5V
Input leakage current	I_{LI}	-10	10	µA	V_{IN} = .1V to Vcc
Output leakage current	I_{LO}	-10	10	µA	V_{OUT} = .1V to Vcc
Pin capacitance (all inputs/outputs)	C_{IN}, C_{OUT}	—	10	pF	Vcc = 5.0V (Note) Tamb = 25°C, Fclk = 1 MHz
Operating current	I_{CC} WRITE	—	3	mA	Vcc = 5.5V, SCL = 400 kHz
	I_{CC} READ	—	1	mA	
Standby current	I_{CCS}	—	30	µA	Vcc = 3.0V, SDA = SCL = Vcc
		—	100	µA	Vcc = 5.5V, SDA = SCL = Vcc

Note: This parameter is periodically sampled and not 100% tested.

FIGURE 1-1:   BUS TIMING START/STOP

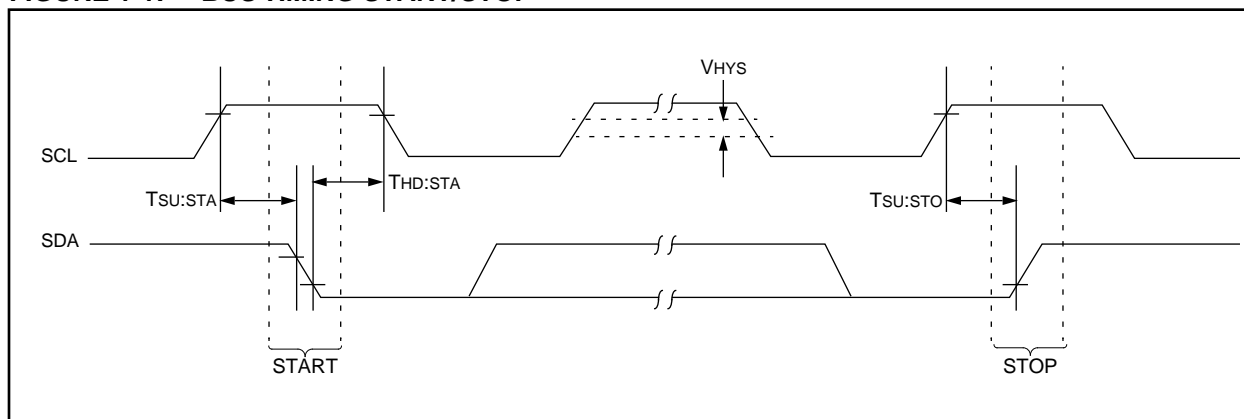**TABLE 1-3:   AC CHARACTERISTICS**

Parameter	Symbol	STANDARD MODE		Vcc = 4.5 - 5.5V FAST MODE		Units	Remarks
		Min	Max	Min	Max		
Clock frequency	F_{CLK}	—	100	—	400	kHz	
Clock high time	T_{HIGH}	4000	—	600	—	ns	
Clock low time	T_{LOW}	4700	—	1300	—	ns	
SDA and SCL rise time	T_R	—	1000	—	300	ns	(Note 1)
SDA and SCL fall time	T_F	—	300	—	300	ns	(Note 1)
START condition hold time	$T_{HD:STA}$	4000	—	600	—	ns	After this period the first clock pulse is generated
START condition setup time	$T_{SU:STA}$	4700	—	600	—	ns	Only relevant for repeated START condition
Data input hold time	$T_{HD:DAT}$	0	—	0	—	ns	
Data input setup time	$T_{SU:DAT}$	250	—	100	—	ns	
STOP condition setup time	$T_{SU:STO}$	4000	—	600	—	ns	
Output valid from clock	T_{AA}	—	3500	—	900	ns	(Note 2)
Bus free time	T_{BUF}	4700	—	1300	—	ns	Time the bus must be free before a new transmission can start
Output fall time from V_{IH} min to V_{IL} max	T_{OF}	—	250	20 +0.1 C_B	250	ns	(Note 1), $C_B \le 100$ pF
Input filter spike suppression (SDA and SCL pins)	T_{SP}	—	50	—	50	ns	(Note 3)
Write cycle time	T_{WR}	—	10	—	10	ms	Byte or Page mode
Endurance 24LC04B	—	10M	—	10M	—	cycles	25°C, Vcc = 5.0V, Block Mode
24LC08B	—	1M	—	1M	—		(Note 4)

Note 1: Not 100% tested. C_B = total capacitance of one bus line in pF.

   2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

   3: The combined T_{SP} and V_{HYS} specifications are due to new Schmitt trigger inputs which provide improved noise and spike suppression. This eliminates the need for a Ti specification for standard operation.

   4: This parameter is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model whcih can be obtained on our BBS or website.

FIGURE 1-2:   BUS TIMING DATA
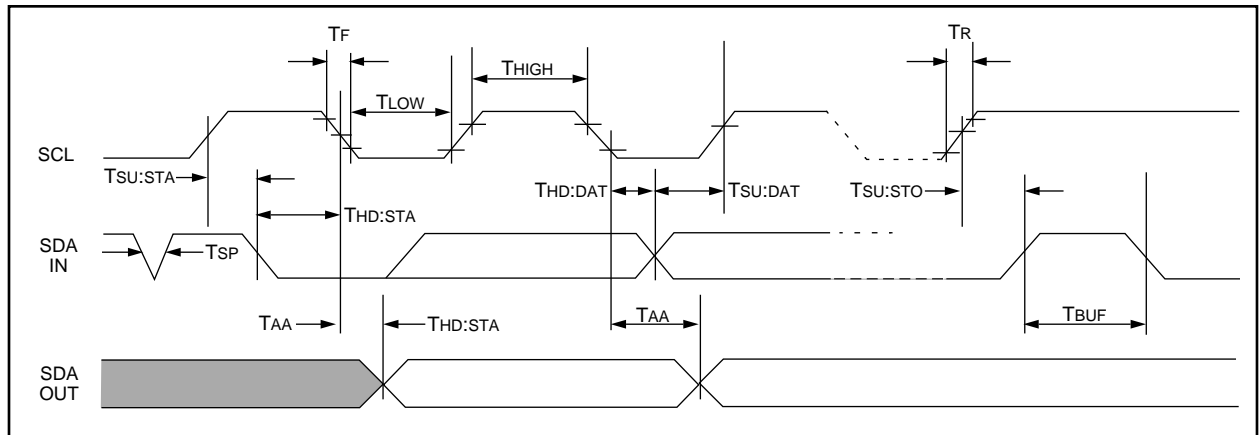
24LC04B/08B

2.0   FUNCTIONAL DESCRIPTION

The 24LC04B/08B supports a Bi-directional 2-wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 24LC04B/08B works as slave. Both, master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

3.0   BUS CHARACTERISTICS

The following **bus protocol** has been defined:

• Data transfer may be initiated only when the bus is not busy.
• During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (Figure 3-1).

3.1   Bus not Busy (A)

Both data and clock lines remain HIGH.

3.2   Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

3.3   Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

3.4   Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited, although only the last 16 will be stored when doing a write operation. When an overwrite does occur it will replace data in a first in first out fashion.

3.5   Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

> **Note:**   The 24LC04B/08B does not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges, has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 3-1:   DATA TRANSFER SEQUENCE ON THE SERIAL BUS
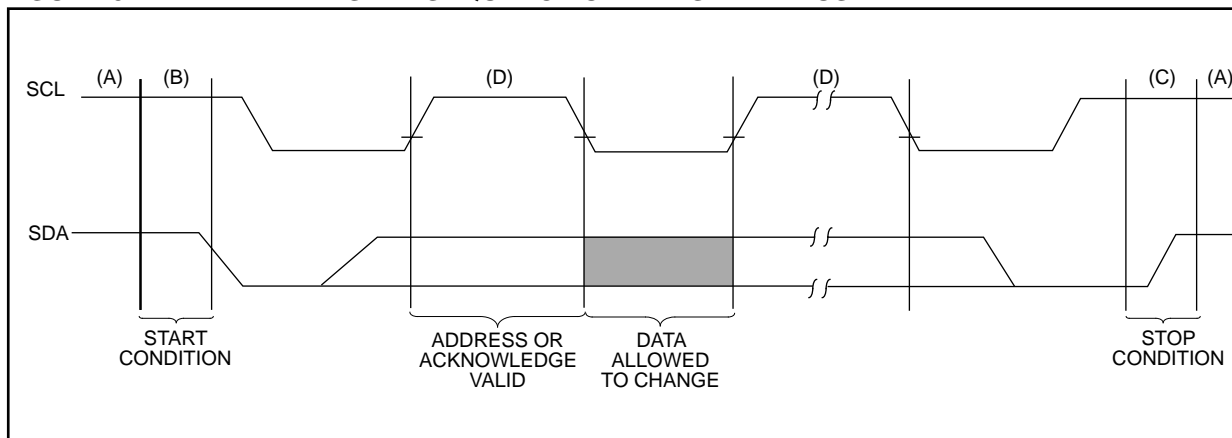
3.6   Device Addressing

A control byte is the first byte received following the start condition from the master device. The control byte consists of a 4-bit control code, for the 24LC04B/08B this is set as 1010 binary for read and write operations. The next three bits of the control byte are the block select bits (B2, B1, B0). B2 is a don't care for both the 24LC04B and 24LC08B; B1 is a don't care for the 24LC04B. They are used by the master device to select which of the two or four 256 word blocks of memory are to be accessed. These bits are in effect the most significant bits of the word address.

The last bit of the control byte defines the operation to be performed. When set to one a read operation is selected, when set to zero a write operation is selected. Following the start condition, the 24LC04B/08B monitors the SDA bus checking the device type identifier being transmitted, upon a 1010 code the slave device outputs an acknowledge signal on the SDA line. Depending on the state of the R/$\overline{W}$ bit, the 24LC04B/08B will select a read or write operation.

Operation	Control Code	Block Select	R/$\overline{W}$
Read	1010	Block Address	1
Write	1010	Block Address	0

FIGURE 3-2:   CONTROL BYTE ALLOCATION

X = Don't care. B1 is don't care for 24LC04B.
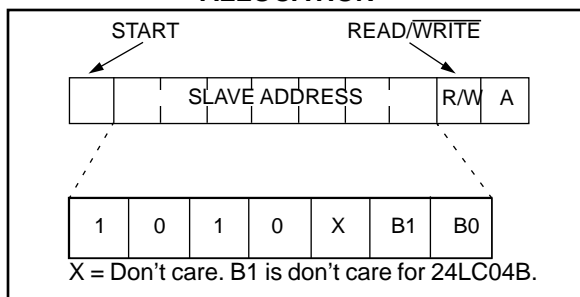
4.0   WRITE OPERATION

4.1   Byte Write

Following the start condition from the master, the device code (4 bits), the block address (3 bits), and the R/$\overline{W}$ bit which is a logic low is placed onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore the next byte transmitted by the master is the word address and will be written into the address pointer of the 24LC04B/08B. After receiving another acknowledge signal from the 24LC04B/08B the master device will transmit the data word to be written into the addressed memory location. The 24LC04B/08B acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time the 24LC04B/08B will not generate acknowledge signals (Figure 4-1).

4.2   Page Write

The write control byte, word address and the first data byte are transmitted to the 24LC04B/08B in the same way as in a byte write. But instead of generating a stop condition the master transmits up to 16 data bytes to the 24LC04B/08B which are temporarily stored in the on-chip page buffer and will be written into the memory after the master has transmitted a stop condition. After the receipt of each word, the four lower order address pointer bits are internally incremented by one. The higher order seven bits of the word address remains constant. If the master should transmit more than 16 words prior to generating the stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the stop condition is received an internal write cycle will begin (Figure 4-2).
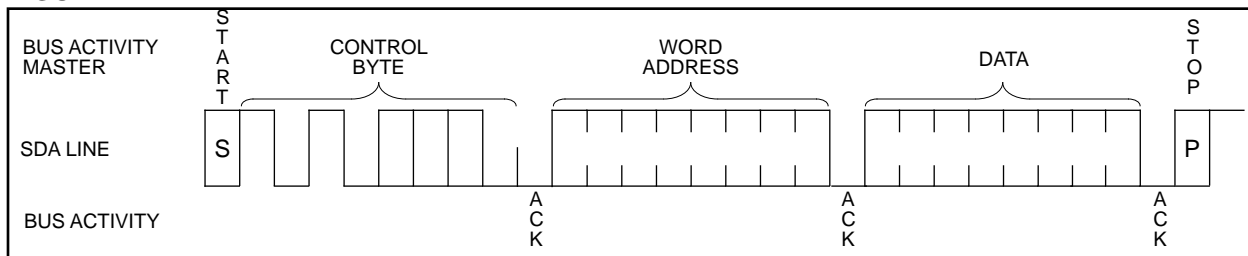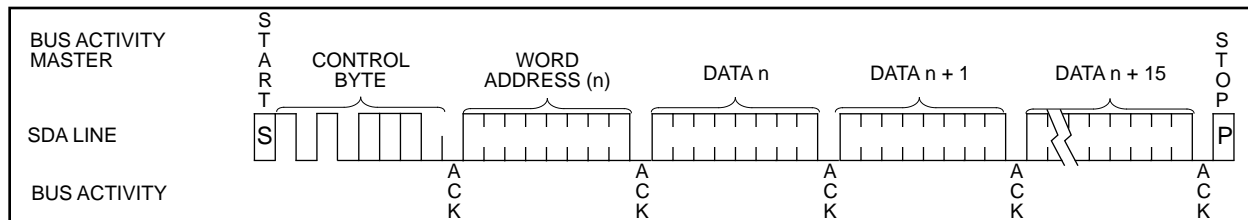
FIGURE 4-1:   BYTE WRITE

FIGURE 4-2:   PAGE WRITE

5.0   ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command (R/$\overline{W}$ = 0). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 5-1 for flow diagram.

FIGURE 5-1:   ACKNOWLEDGE POLLING FLOW
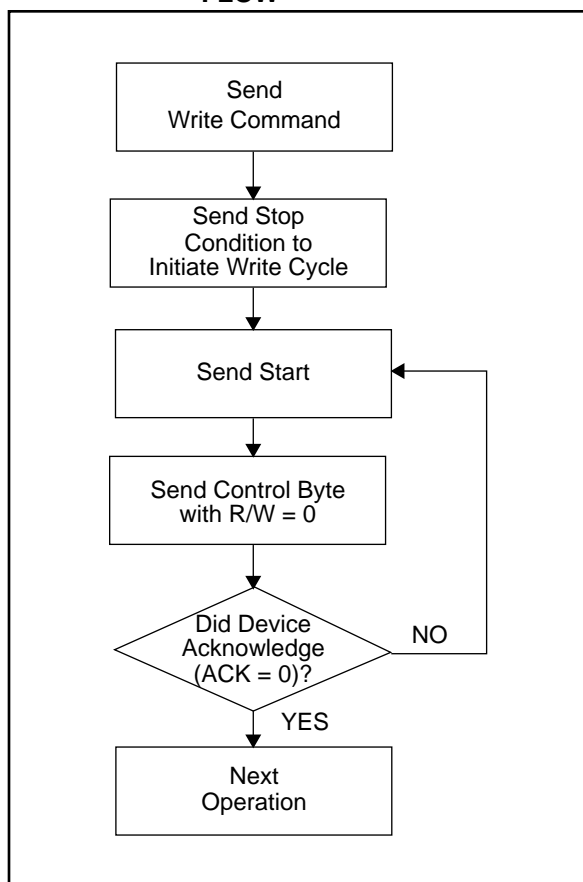
6.0   WRITE PROTECTION

The 24LC04B/08B can be used as a serial ROM when the WP pin is connected to Vcc. Programming will be inhibited and the entire memory will be write-protected.

7.0   READ OPERATION

Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

7.1   Current Address Read

The 24LC04B/08B contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access   (either a read or write operation) was to address n, the next current address read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ bit set to one, the 24LC04B/08B issues an acknowledge and transmits the 8-bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24LC04B/08B discontinues transmission (Figure 7-1).

7.2   Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24LC04B/08B as part of a write operation. After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the R/$\overline{W}$ bit set to a one. The 24LC04B/08B will then issue an acknowledge and transmits the 8-bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24LC04B/08B discontinues transmission (Figure 7-2).

7.3   Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24LC04B/08B transmits the first data byte, the master issues an acknowledge as opposed to a stop condition in a random read. This directs the 24LC04B/08B to transmit the next sequentially addressed 8-bit word (Figure 7-3).

To provide sequential reads the 24LC04B/08B contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation.

7.4   Noise Protection

The 24LC04B/08B employs a Vcc threshold detector circuit which disables the internal erase/write logic if the Vcc is below 1.5 volts at nominal conditions.

The SCL and SDA inputs have Schmitt trigger and filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus.
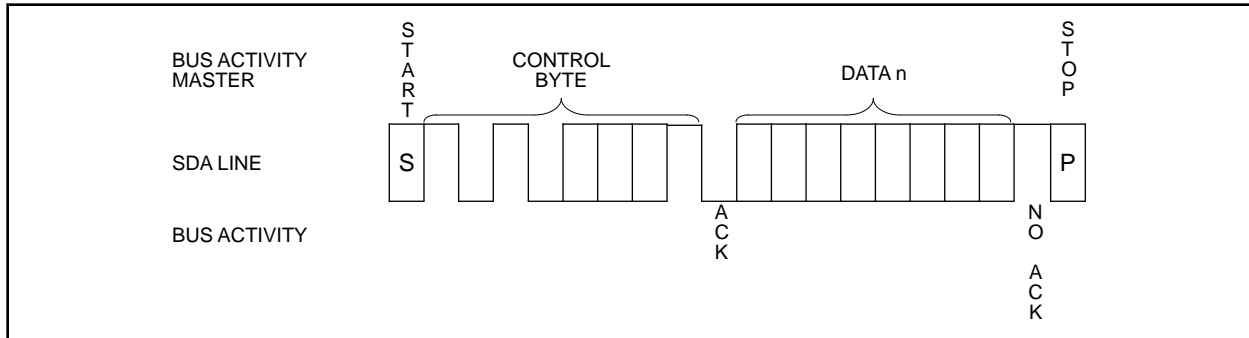
FIGURE 7-1:   CURRENT ADDRESS READ
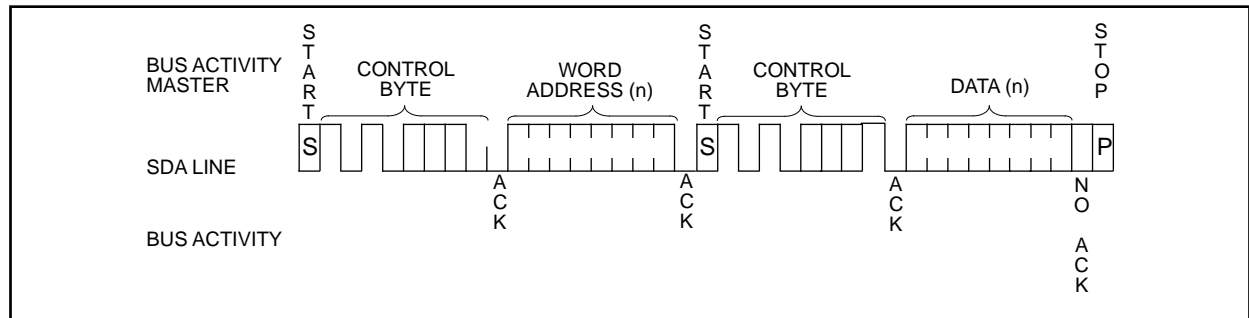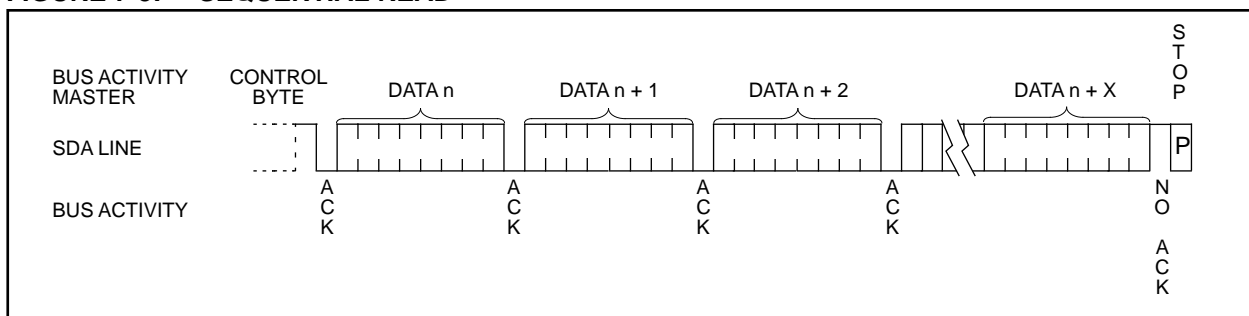

FIGURE 7-2:   RANDOM READ

FIGURE 7-3:   SEQUENTIAL READ

8.0   PIN DESCRIPTIONS

8.1   SDA Serial Address/Data Input/Output

This is a Bi-directional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal, therefore the SDA bus requires a pullup resistor to V_{CC} (typical 10KΩ for 100 kHz, 1KΩ for 400 kHz).

For normal data transfer SDA is allowed to change only during SCL low.   Changes during SCL high are reserved for indicating the START and STOP conditions.

8.2   SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

8.3   WP

This pin must be connected to either V_{SS} or V_{CC}.

If tied to V_{SS}, normal memory operation is enabled (read/write the entire memory).

If tied to V_{CC}, WRITE operations are inhibited.   The entire memory will be write-protected. Read operations are not affected.

This feature allows the user to use the 24LC04B/08B as a serial ROM when WP is enabled (tied to V_{CC}).

8.4   A0, A1, A2

These pins are not used by the 24LC04B/08B. They may be left floating or tied to either V_{SS} or V_{CC}.

NOTES:

NOTES:

NOTES:

24LC04B/08B

24LC04B/08B Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

24LC04B/08B – __ /P

Package:
P = Plastic DIP (300 mil Body), 8-lead
SL = Plastic SOIC (150 mil Body), 14-lead
SN = Plastic SOIC (150 mil Body), 8-lead
SM = Plastic SOIC (207 mil Body), 8-lead

Temperature Range:
Blank = 0°C to +70°C
I = -40°C to +85°C

Device:
24LC04B   4K I^{2}C Serial EEPROM
24LC04BT   4K1^{2}C Serial EEPROM (Tape and Reel)
24LC08B   8K1^{2}C Serial EEPROM
24LC04BT   8K 1^{2}C Serial EEPROM (Tape and Reel)

WORLDWIDE SALES & SERVICE

AMERICAS

Corporate Office
Microchip Technology Inc.
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 602 786-7200 Fax: 602 786-7277
Technical Support: 602 786-7627
Web: http://www.microchip.com

Atlanta
Microchip Technology Inc.
500 Sugar Mill Road, Suite 200B
Atlanta, GA 30350
Tel: 770 640-0034 Fax: 770 640-0307

Boston
Microchip Technology Inc.
5 Mount Royal Avenue
Marlborough, MA 01752
Tel: 508 480-9990 Fax: 508 480-8575

Chicago
Microchip Technology Inc.
333 Pierce Road, Suite 180
Itasca, IL 60143
Tel: 708 285-0071 Fax: 708 285-0075

Dallas
Microchip Technology Inc.
14651 Dallas Parkway, Suite 816
Dallas, TX 75240-8809
Tel: 972 991-7177 Fax: 972 991-8588

Dayton
Microchip Technology Inc.
Suite 150
Two Prestige Place
Miamisburg, OH 45342
Tel: 513 291-1654 Fax: 513 291-9175

Los Angeles
Microchip Technology Inc.
18201 Von Karman, Suite 1090
Irvine, CA 92612
Tel: 714 263-1888 Fax: 714 263-1338

New York
Microchip Technmgy Inc.
150 Motor Parkway, Suite 416
Hauppauge, NY 11788
Tel: 516 273-5305 Fax: 516 273-5335

San Jose
Microchip Technology Inc.
2107 North First Street, Suite 590
San Jose, CA 95131
Tel: 408 436-7950 Fax: 408 436-7955

Toronto
Microchip Technology Inc.
5925 Airport Road, Suite 200
Mississauga, Ontario L4V 1W1, Canada
Tel: 905 405-6279 Fax: 905 405-6253

ASIA/PACIFIC

China
Microchip Technology
Unit 406 of Shanghai Golden Bridge Bldg.
2077 Yan'an Road West, Hongiao District
Shanghai, Peoples Republic of China
Tel: 86 21 6275 5700
Fax: 011 86 21 6275 5060

Hong Kong
Microchip Technology
RM 3801B, Tower Two
Metroplaza
223 Hing Fong Road
Kwai Fong, N.T. Hong Kong
Tel: 852 2 401 1200 Fax: 852 2 401 3431

India
Microchip Technology
No. 6, Legacy, Convent Road
Bangalore 560 025 India
Tel: 91 80 526 3148 Fax: 91 80 559 9840

Korea
Microchip Technology
168-1, Youngbo Bldg. 3 Floor
Samsung-Dong, Kangnam-Ku,
Seoul, Korea
Tel: 82 2 554 7200 Fax: 82 2 558 5934

Singapore
Microchip Technology
200 Middle Road
#10-03 Prime Centre
Singapore 188980
Tel: 65 334 8870 Fax: 65 334 8850

Taiwan, R.O.C
Microchip Technology
10F-1C 207
Tung Hua North Road
Taipei, Taiwan, ROC
Tel: 886 2 717 7175 Fax: 886 2 545 0139

EUROPE

United Kingdom
Arizona Microchip Technology Ltd.
Unit 6, The Courtyard
Meadow Bank, Furlong Road
Bourne End, Buckinghamshire SL8 5AJ
Tel: 44 1628 850303 Fax: 44 1628 850178

France
Arizona Microchip Technology SARL
Zone Industrielle de la Bonde
2 Rue du Buisson aux Fraises
91300 Massy - France
Tel: 33 1 69 53 63 20 Fax: 33 1 69 30 90 79

Germany
Arizona Microchip Technology GmbH
Gustav-Heinemann-Ring 125
D-81739 Muenchen, Germany
Tel: 49 89 627 144 0 Fax: 49 89 627 144 44

Italy
Arizona Microchip Technology SRL
Centro Direzionale Colleone Pas Taurus 1
Viale Colleoni 1
20041 Agrate Brianza
Milan Italy
Tel: 39 39 6899939 Fax: 39 39 689 9883

JAPAN

Microchip Technology Intl. Inc.
Benex S-1 6F
3-18-20, Shin Yokohama
Kohoku-Ku, Yokohama
Kanagawa 222 Japan
Tel: 81 45 471 6166 Fax: 81 45 471 6122

9/3/96