- **−55°C to 125°C Operating Temperature Range, QML Processing**
- **Processed to MIL-PRF-38535 (QML)**
- **Performance**
  - **SMJ320C30-40 (50-ns Cycle)**
    40 MFLOPS
    20 MIPS
  - **SMJ320C30-50 (40-ns Cycle)**
    50 MFLOPS
    25 MIPS
- **Two 1K-Word × 32-Bit Single-Cycle Dual-Access On-Chip RAM Blocks**
- **Validated Ada Compiler**
- **64-Word × 32-Bit Instruction Cache**
- **32-Bit Instruction and Data Words, 24-Bit Addresses**
- **40 / 32-Bit Floating-Point / Integer Multiplier and Arithmetic Logic Unit (ALU)**
- **Parallel ALU and Multiplier Execution in a Single Cycle**
- **On-Chip Direct Memory Access (DMA) Controller for Concurrent I/O and CPU Operation**
- **Integer, Floating-Point, and Logical Operations**
- **One 4K-Word × 32-Bit Single-Cycle Dual-Access On-Chip ROM Block**
- **Two 32-Bit External Ports (24- and 13-Bit Address)**
- **Two Serial Ports With Support for 8- / 16- / 24- / 32-Bit Transfers**
- **Packaging**
  - **181-Pin Grid Array Ceramic Package (GB Suffix)**
  - **196-Pin Ceramic Quad Flatpack With Nonconductive Tie-Bar (HFG Suffix)**
- **SMD Approval for 40- and 50-MHz Versions**
- **Two Address Generators With Eight Auxiliary Registers and Two Auxiliary Register Arithmetic Units (ARAUs)**
- **Zero-Overhead Loops With Single-Cycle Branches**
- **Interlocked Instructions for Multiprocessing Support**
- **32-Bit Barrel Shifter**
- **Eight Extended-Precision Registers (Accumulators)**
- **Two- and Three-Operand Instructions**
- **Conditional Calls and Returns**
- **Block Repeat Capability**
- **Fabricated Using Enhanced Performance Implanted CMOS (EPIC™) by Texas Instruments**
- **Two 32-Bit Timers**

description

The SMJ320C30 internal busing and special digital signal processor (DSP) instruction set has the speed and flexibility to execute up to 50 MFLOPS. The SMJ320C30 device optimizes speed by implementing functions in hardware that other processors implement through software or microcode. This hardware-intensive approach provides performance previously unavailable on a single chip. The emphasis on total system cost has resulted in a less expensive processor that can be designed into systems currently using costly bit-slice processors.

- SMJ320C30-40: 50-ns single-cycle execution time, 5% supply
- SMJ320C30-50: 40-ns single-cycle execution time, 5% supply

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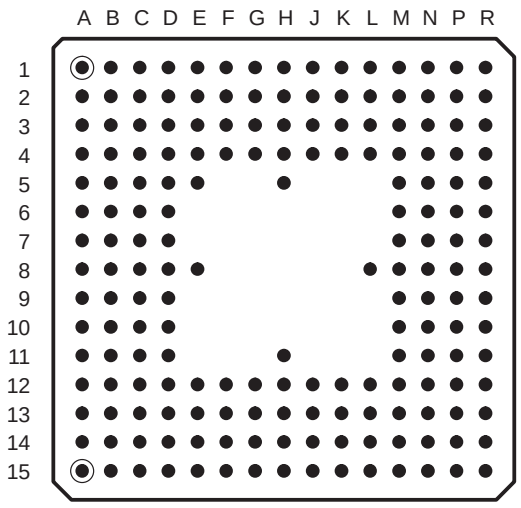
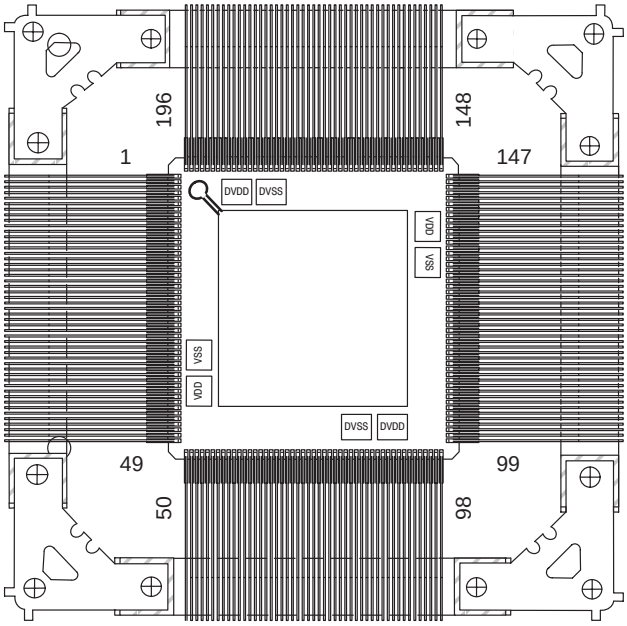
EPIC is a trademark of Texas Instruments Incorporated.

description (continued)

181-Pin GB Grid Array Package
(BOTTOM VIEW)



196-Pin HFG Quad Flatpack
(TOP VIEW)



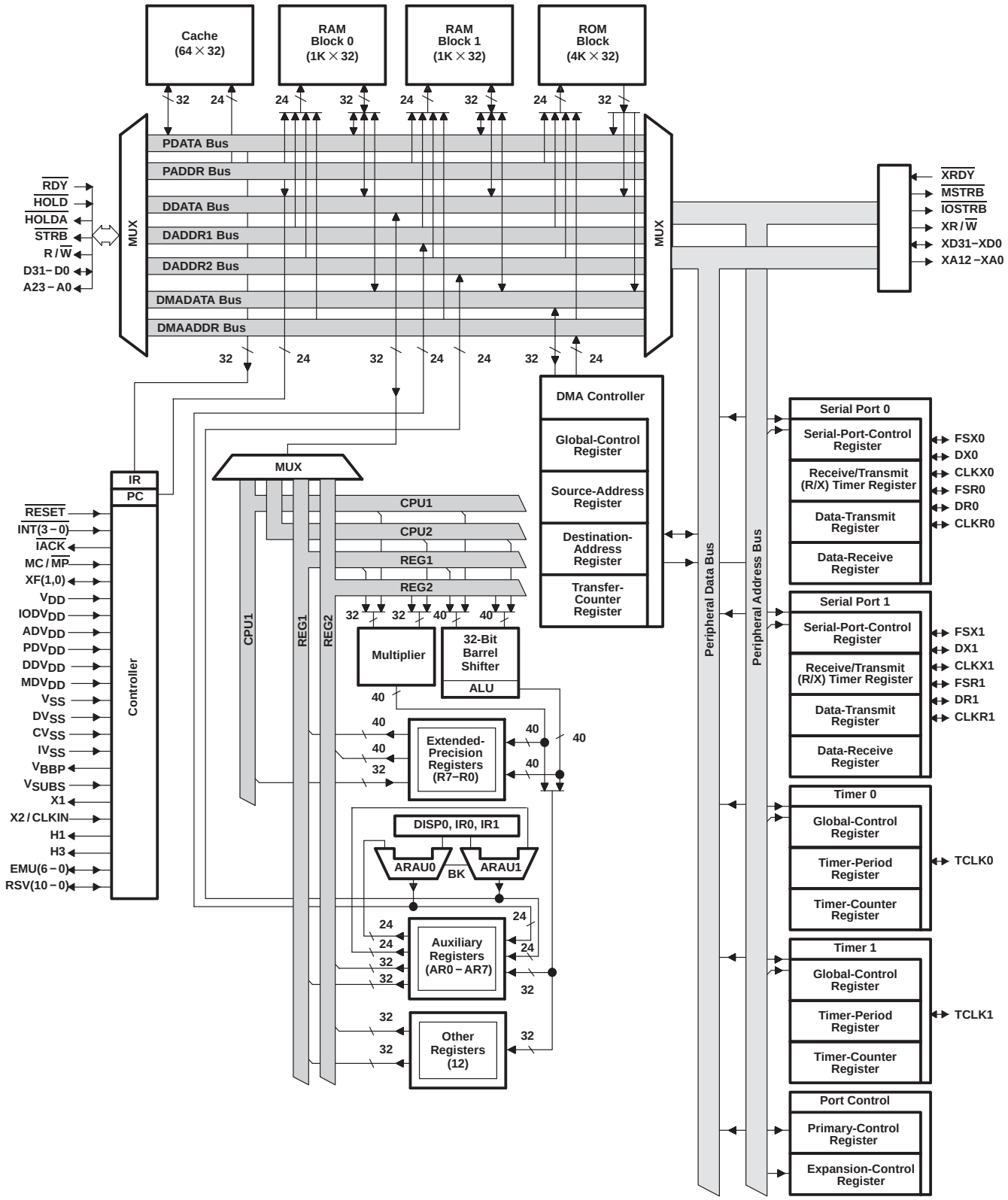
The SMJ320C30 can perform parallel multiply and ALU operations on integer or floating-point data in a single cycle. Each processor also possesses a general-purpose register file, a program cache, dedicated ARAUs, internal dual-access memories, one DMA channel supporting concurrent I/O, and a short machine-cycle time. High performance and ease of use are results of these features.

General-purpose applications are enhanced by the large address space, multiprocessor interface, internally and externally generated wait states, two external interface ports, two timers, two serial ports, and multiple interrupt structure. The SMJ320C30 supports a wide variety of system applications from host processor to dedicated coprocessor.

High-level language support is implemented easily through a register-based architecture, large address space, powerful addressing modes, flexible instruction set, and well-supported floating-point arithmetic.

For additional information when designing for cold temperature operation, please see Texas Instruments application report *320C3x, 320C4x and 320MCM42x Power-up Sensitivity at Cold Temperature*, literature number SGUA001.

functional block diagram



memory map

Figure 1 shows the memory map for the SMJ320C30. See the *TMS320C3x User's Guide* (literature number SPRU031) for a detailed description of this memory mapping. Figure 2 shows the reset, interrupt, and trap vector/branches memory-map locations. Figure 3 shows the peripheral bus memory-mapped registers.

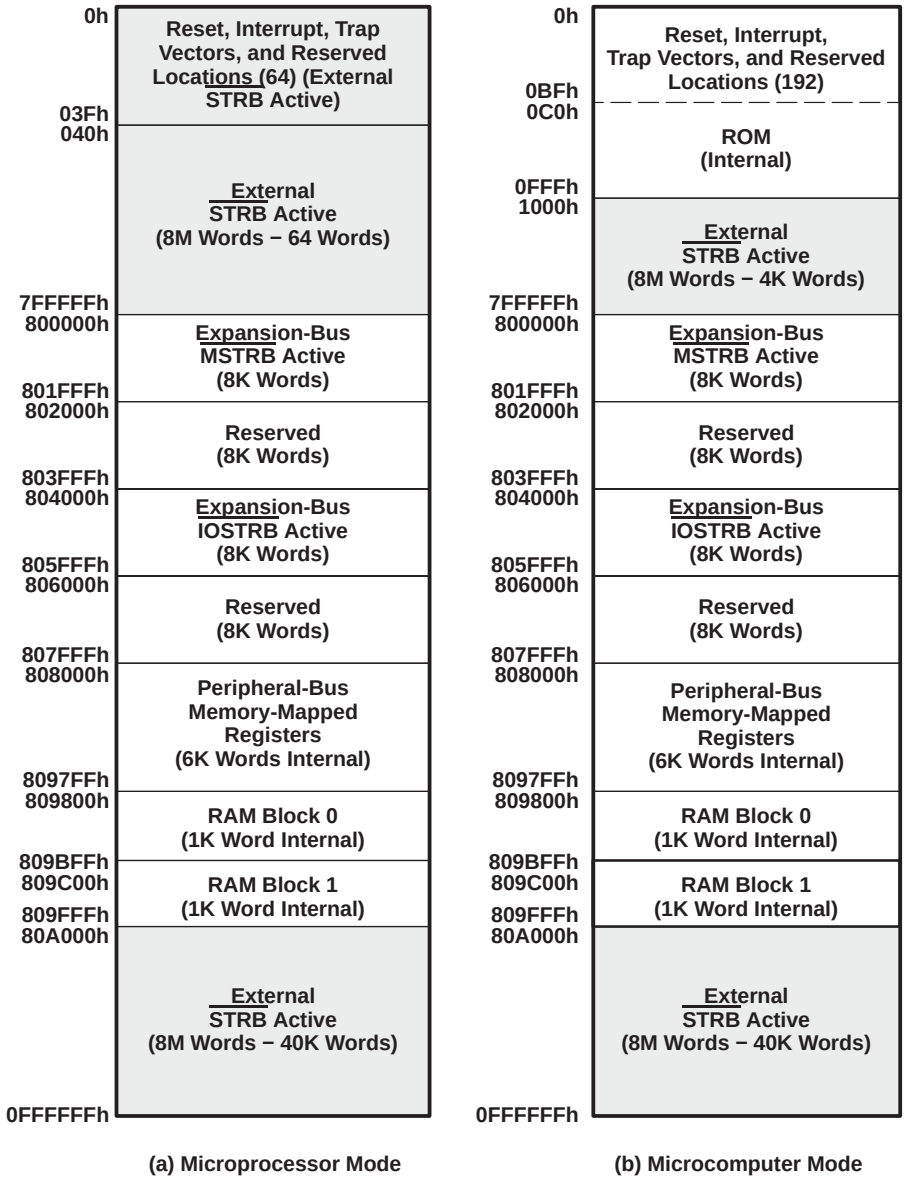


Figure 1. Memory Map

memory map (continued)

00h	Reset
01h	$\overline{\text{INT0}}$
02h	$\overline{\text{INT1}}$
03h	$\overline{\text{INT2}}$
04h	$\overline{\text{INT3}}$
05h	XINT0
06h	RINT0
07h	XINT1
08h	RINT1
09h	TINT0
0Ah	TINT1
0Bh	DINT
0Ch 1Fh	Reserved
20h	TRAP 0
	. . .
3Bh	TRAP 27
3Ch 3Fh	Reserved

(a) Microprocessor Mode

00h	Reset
01h	$\overline{\text{INT0}}$
02h	$\overline{\text{INT1}}$
03h	$\overline{\text{INT2}}$
04h	$\overline{\text{INT3}}$
05h	XINT0
06h	RINT0
07h	XINT1
08h	RINT1
09h	TINT0
0Ah	TINT1
0Bh	DINT
0Ch 1Fh	Reserved
20h	TRAP 0
	. . .
3Bh	TRAP 27
3Ch BFh	Reserved

(a) Microcomputer Mode

Figure 2. Reset, Interrupt, and Trap Vector/Branches Memory-Map Locations

memory map (continued)

808000h	DMA Global Control
808004h	DMA Source Address
808006h	DMA Destination Address
808008h	DMA Transfer Counter
808020h	Timer 0 Global Control
808024h	Timer 0 Counter
808028h	Timer 0 Period
808030h	Timer 1 Global Control
808034h	Timer 1 Counter
808038h	Timer 1 Period Register
808040h	Serial Port 0 Global Control
808042h	FSX/DX/CLKX Serial Port 0 Control
808043h	FSR/DR/CLKR Serial Port 0 Control
808044h	Serial Port 0 R/X Timer Control
808045h	Serial Port 0 R/X Timer Counter
808046h	Serial Port 0 R/X Timer Period
808048h	Serial Port 0 Data Transmit
80804Ch	Serial Port 0 Data Receive
808050h	Serial Port 1 Global Control
808052h	FSX/DX/CLKX Serial Port 1 Control
808053h	FSR/DR/CLKR Serial Port 1 Control
808054h	Serial Port 1 R/X Timer Control
808055h	Serial Port 1 R/X Timer Counter
808056h	Serial Port 1 R/X Timer Period
808058h	Serial Port 1 Data Transmit
80805Ch	Serial Port 1 Data Receive
808060h	Expansion-Bus Control
808064h	Primary-Bus Control

†Shading denotes reserved address locations

Figure 3. Peripheral Bus Memory-Mapped Registers†

pin functions

This section gives signal descriptions for the SMJ320C30 devices in the microprocessor mode. The following tables list each signal, the number of pins, type of operating mode(s) (that is, input, output, or high-impedance state as indicated by I, O, or Z, respectively), and a brief function description. All pins labeled NC have special functions and should not be connected by the user. A line over a signal name (for example, $\overline{\text{RESET}}$) indicates that the signal is active low (true at logic-0 level). The signals are grouped according to functions.

Pin Functions

PIN NAME	PIN QTY‡	TYPE†	DESCRIPTION	CONDITIONS WHEN SIGNAL IS Z TYPE§		
PRIMARY BUS INTERFACE						
D31−D0	32	I/O/Z	32-bit data port of the primary bus interface	S	H	
A23−A0	24	O/Z	24-bit address port of the primary bus interface	S	H	R
R/$\overline{\text{W}}$	1	O/Z	Read/write for primary bus interface. R/$\overline{\text{W}}$ is high when a read is performed and low when a write is performed over the parallel interface.	S	H	R
$\overline{\text{STRB}}$	1	O/Z	External access strobe for the primary bus interface	S	H	
$\overline{\text{RDY}}$	1	I	Ready. $\overline{\text{RDY}}$ indicates that the external device is prepared for a primary bus interface transaction to complete.			
$\overline{\text{HOLD}}$	1	I	Hold for primary bus interface. When $\overline{\text{HOLD}}$ is a logic low, any ongoing transaction is completed. A23−A0, D31−D0, $\overline{\text{STRB}}$, and R/$\overline{\text{W}}$ are in the high-impedance state and all transactions over the primary bus interface are held until $\overline{\text{HOLD}}$ becomes a logic high or the NOHOLD bit of the primary bus control register is set.			
$\overline{\text{HOLDA}}$	1	O/Z	Hold acknowledge for primary bus interface. $\overline{\text{HOLDA}}$ is generated in response to a logic low on $\overline{\text{HOLD}}$. $\overline{\text{HOLDA}}$ indicates that A23−A0, D31−D0, $\overline{\text{STRB}}$, and R/$\overline{\text{W}}$ are in the high-impedance state and that all transactions over the bus are held. $\overline{\text{HOLDA}}$ is high in response to a logic high of $\overline{\text{HOLD}}$ or when the NOHOLD bit of the primary bus control register is set.	S		
EXPANSION BUS INTERFACE						
XD31−XD0	32	I/O/Z	32-bit data port of the expansion bus interface	S		R
XA12−XA0	13	O/Z	13-bit address port of the expansion bus interface	S		R
XR/$\overline{\text{W}}$	1	O/Z	Read/write signal for expansion bus interface. When a read is performed, XR/$\overline{\text{W}}$ is held high; when a write is performed, XR/$\overline{\text{W}}$ is low.	S		R
$\overline{\text{MSTRB}}$	1	O/Z	External memory access strobe for the expansion bus interface	S		
$\overline{\text{IOSTRB}}$	1	O/Z	External I/O access strobe for the expansion bus interface	S		
$\overline{\text{XRDY}}$	1	I	Ready signal. $\overline{\text{XRDY}}$ indicates that the external device is prepared for an expansion bus interface transaction to complete.			
CONTROL SIGNALS						
$\overline{\text{RESET}}$	1	I	Reset. When $\overline{\text{RESET}}$ is a logic low, the device is in the reset condition. When $\overline{\text{RESET}}$ becomes a logic high, execution begins from the location specified by the reset vector.			
$\overline{\text{INT3}}$−$\overline{\text{INT0}}$	4	I	External interrupts			
$\overline{\text{IACK}}$	1	O/Z	Interrupt acknowledge. $\overline{\text{IACK}}$ is set to a logic high by the IACK instruction. $\overline{\text{IACK}}$ can be used to indicate the beginning or end of an interrupt-service routine.	S		
MC/$\overline{\text{MP}}$	1	I	Microcomputer/microprocessor mode			
XF1, XF0	2	I/O/Z	External flags. XF1 and XF0 are used as general-purpose I/Os or to support interlocked processor instructions.	S		R

† I = input, O = output, Z = high-impedance state, NC = no connect
‡ For GB package
§ S = $\overline{\text{SHZ}}$ active, H = $\overline{\text{HOLD}}$ active, R = $\overline{\text{RESET}}$ active

Pin Functions (Continued)

PIN NAME	PIN QTY‡	TYPE†	DESCRIPTION	CONDITIONS WHEN SIGNAL IS Z TYPE§	
SERIAL PORT 0 SIGNALS					
CLKX0	1	I/O/Z	Serial port 0 transmit clock. CLKX0 is the serial-shift clock for the serial port 0 transmitter.	S	R
DX0	1	I/O/Z	Data transmit output. Serial port 0 transmits serial data on DX0.	S	R
FSX0	1	I/O/Z	Frame synchronization pulse for transmit. The FSX0 pulse initiates the transmit-data process over DX0.	S	R
CLKR0	1	I/O/Z	Serial port 0 receive clock. CLKR0 is the serial-shift clock for the serial port 0 receiver.	S	R
DR0	1	I/O/Z	Data receive. Serial port 0 receives serial data on DR0.	S	R
FSR0	1	I/O/Z	Frame synchronization pulse for receive. The FSR0 pulse initiates the receive-data process over DR0.	S	R
SERIAL PORT 1 SIGNALS					
CLKX1	1	I/O/Z	Serial port 1 transmit clock. CLKX1 is the serial-shift clock for the serial port 1 transmitter.	S	R
DX1	1	I/O/Z	Data transmit output. Serial port 1 transmits serial data on DX1.	S	R
FSX1	1	I/O/Z	Frame synchronization pulse for transmit. The FSX1 pulse initiates the transmit-data process over DX1.	S	R
CLKR1	1	I/O/Z	Serial port 1 receive clock. CLKR1 is the serial-shift clock for the serial port 1 receiver.	S	R
DR1	1	I/O/Z	Data receive. Serial port 1 receives serial data on DR1.	S	R
FSR1	1	I/O/Z	Frame synchronization pulse for receive. The FSR1 pulse initiates the receive-data process over DR1.	S	R
TIMER 0 SIGNALS					
TCLK0	1	I/O/Z	Timer clock 0. As an input, TCLK0 is used by timer 0 to count external pulses. As an output, TCLK0 outputs pulses generated by timer 0.	S	R
TIMER 1 SIGNALS					
TCLK1	1	I/O/Z	Timer clock 1. As an input, TCLK1 is used by timer 1 to count external pulses. As an output, TCLK1 outputs pulses generated by timer 1.	S	R
SUPPLY AND OSCILLATOR SIGNALS (see Note 1)					
V_{DD}	4	I	5-V supply¶		
$IODV_{DD}$	2	I	5-V supply¶		
ADV_{DD}	2	I	5-V supply¶		
PDV_{DD}	1	I	5-V supply¶		
DDV_{DD}	2	I	5-V supply¶		
MDV_{DD}	1	I	5-V supply¶		
V_{SS}	4	I	Ground		
DV_{SS}	4	I	Ground		
CV_{SS}	2	I	Ground		

† I = input, O = output, Z = high-impedance state, NC = no connect
‡ For GB package
§ S = $\overline{SHZ}$ active, H = $\overline{HOLD}$ active, R = $\overline{RESET}$ active
¶ Recommended decoupling capacitor is 0.1 μF.
NOTE 1: CV_{SS}, V_{SS}, and IV_{SS} are on the same plane.

Pin Functions (Continued)

PIN NAME	PIN QTY‡	TYPE†	DESCRIPTION	CONDITIONS WHEN SIGNAL IS Z TYPE§
SUPPLY AND OSCILLATOR SIGNALS (see Note 1) (CONTINUED)				
IV_{SS}	1	I	Ground	
V_{BBP}	1	NC	V_{BB} pump oscillator output	
V_{SUBS}	1	I	Substrate pin. Tie to ground	
X1	1	O	Output from the internal oscillator for the crystal. If a crystal is not used, X1 must be left unconnected.	
X2/CLKIN	1	I	Input to the internal oscillator from the crystal or a clock	
H1	1	O/Z	External H1 clock. H1 has a period equal to twice CLKIN.	S
H3	1	O/Z	External H3 clock. H3 has a period equal to twice CLKIN.	S
RESERVED (see Note 2)				
EMU0−EMU2	3	I	Reserved. Use pullup resistors to 5 V	
EMU3	1	O/Z	Reserved	S
EMU4/$\overline{SHZ}$	1	I	Shutdown high impedance. When active, EMU4/$\overline{SHZ}$ shuts down the SMJ320C30 and places all pins in the high-impedance state. EMU4/$\overline{SHZ}$ is used for board-level testing to ensure that no dual-drive conditions occur. **CAUTION:** A low on $\overline{SHZ}$ corrupts SMJ320C30 memory and register contents. Reset the device with $\overline{SHZ}$ high to restore it to a known operating condition.	
EMU5, EMU6	2	NC	Reserved	
RSV0−RSV4	5	I	Reserved. Tie pins directly to 5 V	
RSV5−RSV10	6	I/O	Reserved. Use pullups on each pin to 5 V	
Locator	1	NC	Reserved	

† I = input, O = output, Z = high-impedance state, NC = No Connect
‡ For GB package
§ S = $\overline{SHZ}$ active, H = $\overline{HOLD}$ active, R = $\overline{RESET}$ active

NOTES: 1. CV_{SS}, V_{SS}, IV_{SS} are on the same plane.
2. The connections specified for the reserved pins must be followed. For best results, 18-kΩ−22-kΩ pullup resistors are recommended. All 5-V supply pins must be connected to a common supply plane, and all ground pins must be connected to a common ground plane.

Pin Assignments

PIN NUMBER			PIN NUMBER			PIN NUMBER			PIN NUMBER			PIN NUMBER		
GB PKG	HFG PKG	NAME	GB PKG	HFG PKG	NAME	GB PKG	HFG PKG	NAME	GB PKG	HFG PKG	NAME	GB PKG	HFG PKG	NAME
F15	82	A0	C5	139	D5	P2	195	DX1	L2	185	RSV6	R8	29	XD11
G12	81	A1	D6	138	D6	F14	83	EMU0	K4	186	RSV7	R9	30	XD12
G13	80	A2	A4	137	D7	E15	84	EMU1	M1	187	RSV8	P9	31	XD13
G14	79	A3	B5	136	D8	F13	85	EMU2	L3	188	RSV9	N9	32	XD14
G15	78	A4	C6	135	D9	E14	86	EMU3	M2	189	RSV10	R10	33	XD15
H15	77	A5	A5	134	D10	F12	87	EMU4/$\overline{SHZ}$	D12	100	ADV_{DD}†	M9	34	XD16
H14	72	A6	B6	133	D11	C1	155	EMU5	H11	64	ADV_{DD}†	P10	35	XD17
J15	71	A7	D7	132	D12	M6	11	EMU6	D4	114	DDV_{DD}†	R11	36	XD18
J14	70	A8	A6	131	D13	B3	145	H1	E8	147	DDV_{DD}†	N10	37	XD19
J13	69	A9	C7	130	D14	A1	146	H3	L8	15	$IODV_{DD}$†	P11	38	XD20
K15	68	A10	B7	129	D15	C2	152	X1	M12	16	$IODV_{DD}$†	R12	39	XD21
J12	67	A11	A7	128	D16	B1	151	X2/CLKIN		49	$IODV_{DD}$†	M10	40	XD22
K14	66	A12	A8	127	D17	P4	9	TCLK0	H5	162	MDV_{DD}†	N11	41	XD23
L15	65	A13	B8	122	D18	N5	10	TCLK1		163	MDV_{DD}†	P12	42	XD24
K13	63	A14	A9	121	D19	G2	169	XF0	M4	1	PDV_{DD}†	R13	43	XD25
L14	62	A15	B9	120	D20	G3	168	XF1	B2	51	CV_{SS}§	R14	44	XD26
M15	61	A16	C9	119	D21	D3	154	V_{BBP}	P14	52	CV_{SS}§	M11	45	XD27
K12	60	A17	A10	118	D22	E4	153	V_{SUBS}		25	V_{DD}‡	N12	46	XD28
L13	59	A18	D9	117	D23	H4	123	V_{DD}‡		26	V_{DD}‡	P13	47	XD29
M14	58	A19	B10	116	D24	D8	73	V_{DD}‡		172	V_{DD}‡	R15	48	XD30
N15	57	A20	A11	115	D25	M8	74	V_{DD}‡		173	V_{DD}‡	P15	53	XD31
M13	56	A21	C10	113	D26	H12	124	V_{DD}‡	C8	28	V_{SS}§		2	DV_{DD}
L12	55	A22	B11	112	D27	N8	27	V_{SS}§	H3	75	V_{SS}§		101	DV_{DD}
N14	54	A23	A12	111	D28	A13	107	XA0	H13	76	V_{SS}§	C3	50	DV_{SS}¶
E5		LOCATOR/NC	D10	110	D29	A14	106	XA1		125	V_{SS}§	C13	98	DV_{SS}¶
G1	170	$\overline{IACK}$	C11	109	D30	D11	105	XA2		126	V_{SS}§	N3	148	DV_{SS}¶
H2	171	$\overline{INT0}$	B12	108	D31	C12	104	XA3		149	V_{SS}§	N13	196	DV_{SS}¶
H1	176	$\overline{INT1}$	F3	161	$\overline{HOLD}$	B13	103	XA4		150	V_{SS}§	B14	96	IV_{SS}§
J1	177	$\overline{INT2}$	E2	160	$\overline{HOLDA}$	A15	102	XA5		174	V_{SS}§		97	IV_{SS}§
J2	178	$\overline{INT3}$	D2	156	$\overline{XRDY}$	B15	95	XA6		175	V_{SS}§			
D15	88	MC/$\overline{MP}$	D1	159	XR/$\overline{W}$	C14	94	XA7		99	V_{SUBS}			
E3	157	$\overline{MSTRB}$	P3	4	FSR0	E12	93	XA8	R4	12	XD0			
E1	164	$\overline{RDY}$	R2	7	FSX0	D13	92	XA9	P5	13	XD1			
F1	167	$\overline{RESET}$	N4	5	CLKR0	C15	91	XA10	N6	14	XD2			
G4	166	R/$\overline{W}$	M5	6	CLKX0	D14	90	XA11	R5	17	XD3			
F2	165	$\overline{STRB}$	R1	3	DR0	E13	89	XA12	P6	18	XD4			
F4	158	$\overline{IOSTRB}$	R3	8	DX0	J3	179	RSV0	M7	19	XD5			
C4	144	D0	M3	191	FSR1	J4	180	RSV1	R6	20	XD6			
D5	143	D1	P1	194	FSX1	K1	181	RSV2	N7	21	XD7			
A2	142	D2	L4	192	CLKR1	K2	182	RSV3	P7	22	XD8			
A3	141	D3	N2	193	CLKX1	L1	183	RSV4	R7	23	XD9			
B4	140	D4	N1	190	DR1	K3	184	RSV5	P8	24	XD10			

† ADV_{DD}, DDV_{DD}, $IODV_{DD}$, MDV_{DD}, and PDV_{DD} are on a common plane internal to the device.
‡ V_{DD} is on a common plane internal to the device.
§ V_{SS}, CV_{SS}, and IV_{SS} are on a common plane internal to the device.
¶ DV_{SS} is on a common plane internal to the device.

absolute maximum ratings over operating case temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 3) . . . . . −0.3 V to 7 V
Input voltage range, V_I . . . . . − 0.3 V to 7 V
Output voltage range, V_O . . . . . −0.3 V to 7 V
Continuous power dissipation (see Note 4) . . . . . 3.15 W
Operating case temperature range, T_C . . . . . − 55°C to 125°C
Storage temperature range, T_{stg} . . . . . − 65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 3. All voltage values are with respect to V_{SS}.
4. Actual operating power is less. This value was obtained under specially produced worst-case test conditions, which are not sustained during normal device operation. These conditions consist of continuous parallel writes of a checkerboard pattern to both primary and extension buses at the maximum rate possible. See normal (I_{CC}) current specification in the electrical characteristics table and also read *Calculation of TMS320C30 Power Dissipation Application Report* (literature number SPRA020).

recommended operating conditions (see Note 5)

		MIN	NOM‡	MAX	UNIT
V_{DD}	Supply voltage (AV_{DD}, etc.)	4.75	5	5.25	V
V_{SS}	Supply voltage (CV_{SS}, etc.)		0		V
V_{IH}	High-level input voltage	2.1		V_{DD} + 0.3*	V
V_{TH}	High-level input voltage for CLKIN	3		V_{DD} + 0.3*	V
V_{IL}	Low-level input voltage	− 0.3*		0.8	V
I_{OH}	High-level output current			− 300	µA
I_{OL}	Low-level output current			2	mA
T_C	Operating case temperature (see Note 6)	− 55		125	°C

‡ All nominal values are at V_{DD} = 5 V, T_A (ambient-air temperature)= 25°C.
* This parameter is not production tested.
NOTE 5: All input and output voltage levels are TTL compatible.
NOTE 6: T_C MAX at maximum rated operating conditions at any point on the case, T_C MIN at initial (time zero) power up

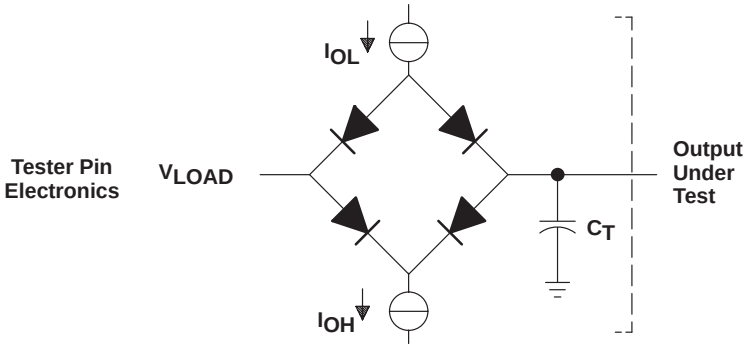
electrical characteristics over recommended ranges of supply voltage (unless otherwise noted) (see Note 5)

PARAMETER			TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{OH}	High-level output voltage		V_{DD} = MIN, I_{OH} = MAX	2.4	3		V
V_{OL}	Low-level output voltage	For XA12−XA0	V_{DD} = MIN, I_{OL} = MAX			0.6*	V
		All others	V_{DD} = MIN, I_{OL} = MAX		0.3	0.6	V
I_Z	High-impedance current		V_{DD} = MAX			± 20	µA
I_I	Input current		V_I = V_{SS} to V_{DD}			± 10	µA
I_{IP}	Input current		Inputs with internal pullups (see Note 7)	− 600		20	µA
I_{IC}	Input current (X2/CLKIN)		V_I = V_{SS} to V_{DD}			± 50	µA
I_{CC}	Supply current		V_{DD} = MAX, T_A = 25°C, $t_{c(CI)}$ = MIN, See Note 8		200	600	mA
I_{DD}	Supply current, standby; IDLE2, clock shut off		V_{DD} = 5 V, T_A = 25°C		50		mA
C_i	Input capacitance					15*	pF
C_o	Output capacitance					20*	pF
C_x	X2/CLKIN capacitance					25*	pF

† For conditions shown as MIN/MAX, use the appropriate value specified in recommended operating conditions.
‡ All typical values are at V_{DD} = 5 V, T_A = 25°C.
* This parameter is not production tested.

NOTES: 5. All input and output voltage levels are TTL compatible.
7. Pins with internal pullup devices: INT0−INT3, MC/MP, RSV0−RSV10. Although RSV0−RSV10 have internal pullup devices, external pullups should be used on each pin as identified in the pin function tables.
8. Actual operating current is less than this maximum value. This value was obtained under specially produced worst-case test conditions, which are not sustained during normal device operation. These conditions consist of continuous parallel writes of a checkerboard pattern to both primary and expansion buses at the maximum rate possible. See *Calculation of TMS320C30 Power Dissipation Application Report* (literature number SPRA020).

PARAMETER MEASUREMENT INFORMATION



Where: I_{OL} = 2 mA (all outputs)
I_{OH} = 300 µA (all outputs)
V_{LOAD} = Selected to emulate 50 Ω termination (typical value = 1.54 V).
C_T = 80-pF typical load-circuit capacitance

Figure 4. Test Load Circuit

PARAMETER MEASUREMENT INFORMATION (CONTINUED)

signal transition levels

TTL-level outputs are driven to a minimum logic-high level of 2.4 V and to a maximum logic-low level of 0.6 V. Output transition times are specified as follows:

- For a high-to-low transition on a TTL-compatible output signal, the level at which the output is said to be no longer high is 2 V and the level at which the output is said to be low is 1 V.
- For a low-to-high transition, the level at which the output is said to be no longer low is 1 V and the level at which the output is said to be high is 2 V.

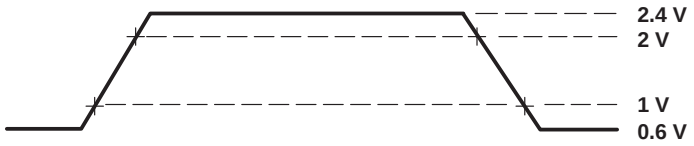


Figure 5. TTL-Level Outputs

Transition times for TTL-compatible inputs are specified as follows:

- For a high-to-low transition on an input signal, the level at which the input is said to be no longer high is 2.1 V and the level at which the input is said to be low is 0.8 V.
- For a low-to-high transition on an input signal, the level at which the input is said to be no longer low is 0.8 V and the level at which the input is said to be high is 2.1 V.

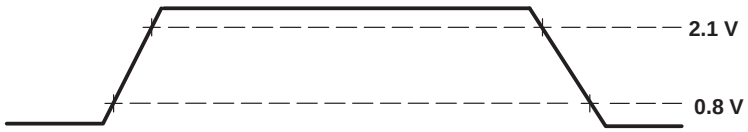


Figure 6. TTL-Level Inputs

PARAMETER MEASUREMENT INFORMATION (CONTINUED)

timing parameter symbology

Timing parameter symbols used herein were created in accordance with JEDEC Standard 100-A. To shorten the symbols, some of the terminal names and other related terminology have been abbreviated as follows, unless otherwise noted:

A	A23−A0	IACK	$\overline{\text{IACK}}$
ASYNCH	Asynchronous reset signals include XF0, XF1, CLKX0, DX0, FSX0, CLKR0, DR0, FSR0, CLKX1, DX1, FSX1, CLKR1, DR1, FSR1, TCLK0, and TCLK1	INT	$\overline{\text{INT3}}$−$\overline{\text{INT0}}$
CH	CLKX includes CLKX0 and CLKX1	IOS	$\overline{\text{IOSTRB}}$
CI	CLKIN	(M)S	$\overline{\text{(M)STRB}}$ includes $\overline{\text{MSTRB}}$ and $\overline{\text{STRB}}$
CONTROL	Control signals include $\overline{\text{STRB}}$, $\overline{\text{MSTRB}}$, and $\overline{\text{IOSTRB}}$	RDY	$\overline{\text{RDY}}$
D	D31−D0	RESET	$\overline{\text{RESET}}$
DR	Includes DR0, DR1	RW	R/$\overline{\text{W}}$
DX	Includes DX0, DX1	S	$\overline{\text{STRB}}$
FS	FSX/R includes FSX0, FSX1, FSR0, and FSR1	SCK	CLKX/R includes CLKX0, CLKX1, CLKR0, and CLKR1
FSR	Includes FSR0, FSR1	TCLK	TCLK0, TCLK1
FSX	Includes FSX0, FSX1	(X)A	Includes A23−A0 and XA12−XA0
GPIO	General-purpose input/output; peripheral pins include CLKX0/1, CLKR0/1, DX0/1, DR0/1, FSX0/1, FSR0/1, and TCLK0/1	(X)D	Includes D31−D0 and XD31−XD0
H	Includes H1, H3	XF	XFx includes XF0 and XF1
H1	H1	XF0	XF0
H3	H3	XF1	XF1
HOLD	$\overline{\text{HOLD}}$	(X)RDY	Includes $\overline{\text{RDY}}$ and $\overline{\text{XRDY}}$
HOLDA	$\overline{\text{HOLDA}}$	(X)RW	(X)R/$\overline{\text{W}}$ includes R/$\overline{\text{W}}$ and XR/$\overline{\text{W}}$

X2/CLKIN, H1, and H3 timing

The following table defines the timing parameters for the X2/CLKIN, H1, and H3 interface signals. See the $\overline{\text{RESET}}$ timing in Figure 20 for CLKIN to H1 and H3 delay specification.

timing parameters for X2/CLKIN, H1, H3 (see Note 5, Figure 7, Figure 8, and Figure 9)

NO.†			320C30-40		320C30-50		UNIT
			MIN	MAX	MIN	MAX	
1	$t_{f(CI)}$	Fall time, CLKIN		5*		5*	ns
2	$t_{w(CIL)}$	Pulse duration, CLKIN low, $t_{c(CI)}$ = MIN (see Note 9)	9		7		ns
3	$t_{w(CIH)}$	Pulse duration, CLKIN high, $t_{c(CI)}$ = MIN (see Note 9)	9		7		ns
4	$t_{r(CI)}$	Rise time, CLKIN		5*		5*	ns
5	$t_{c(CI)}$	Cycle time, CLKIN	25	303	20	303	ns
6	$t_{f(H)}$	Fall time, H1/H3		3		3	ns
7	$t_{w(HL)}$	Pulse duration, H1/H3 low (see Note 10)	P − 5		P − 5		ns
8	$t_{w(HH)}$	Pulse duration, H1/H3 high (see Note 10)	P − 6		P − 6		ns
9	$t_{r(H)}$	Rise time, H1/H3		3		3	ns
9.1	$t_{d(HL-HH)}$	Delay time, from H1 low to H3 high or from H3 low to H1 high	0	4	0	4	ns
10	$t_{c(H)}$	Cycle time, H1/H3	50	606	40	606	ns

† Numbers in this column match those used in Figure 7, Figure 8, and Figure 9.

* This parameter is not production tested.

NOTES: 5. All input and output voltage levels are TTL compatible.

9. Rise and fall times, assuming a 35 − 65% duty cycle, are incorporated within this specification (see Figure 6).

10. P = $t_{c(CI)}$

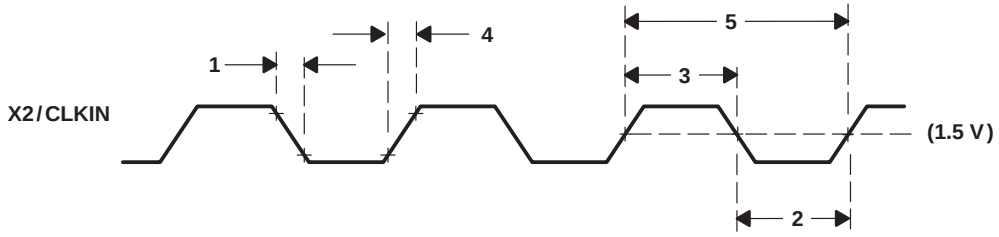


Figure 7. X2/CLKIN Timing

timing parameters for X2/CLKIN, H1, H3 (see Note 5, Figure 7, Figure 8, and Figure 9) (continued)

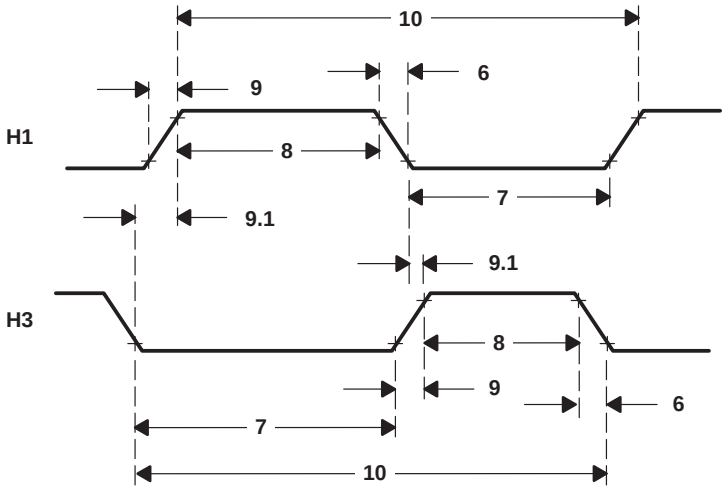


Figure 8. H1/H3 Timings

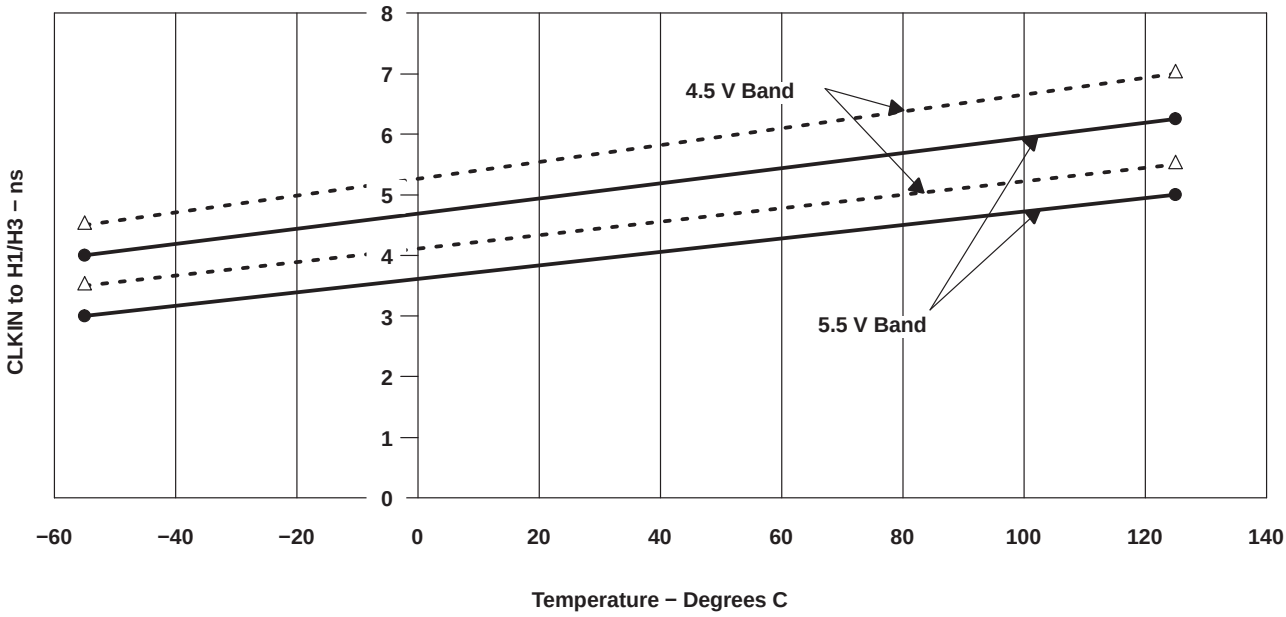


Figure 9. CLKIN to H1/H3 as a Function of Temperature (Typical)

memory read/write timing

The following table defines memory read/write timing parameters for $\overline{(M)STRB}$.

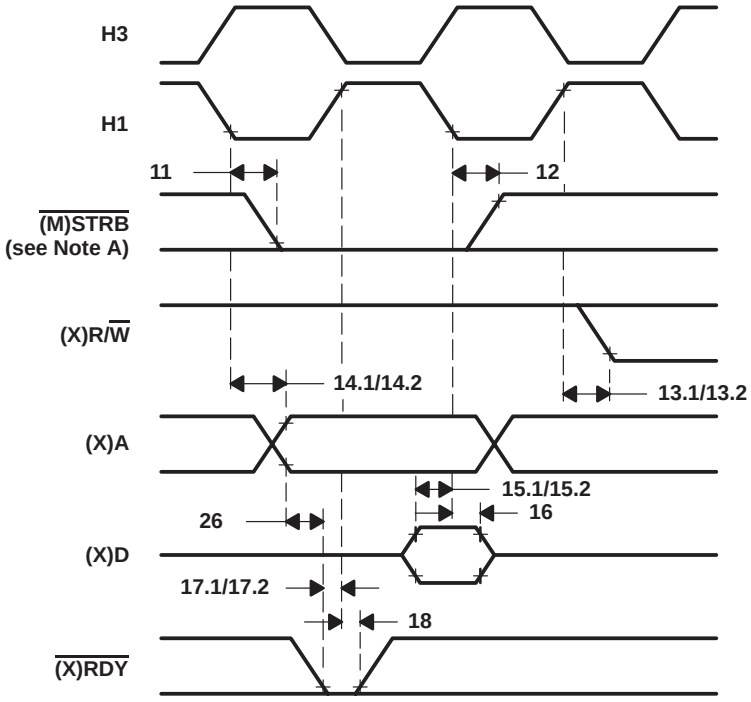
timing parameters for a memory [$\overline{(M)STRB}$ = 0] read/write (see Figure 10 and Figure 11)

NO.†			320C30-40		320C30-50		UNIT
			MIN	MAX	MIN	MAX	
11	$t_{d[H1L-(M)SL]}$	Delay time, H1 low to $\overline{(M)STRB}$ low	0*	10	0*	4	ns
12	$t_{d[H1L-(M)SH]}$	Delay time, H1 low to $\overline{(M)STRB}$ high	0*	6	0*	4	ns
13.1	$t_{d(H1H-RWL)}$	Delay time, H1 high to R/$\overline{W}$ low	0*	9	0*	7	ns
13.2	$t_{d[H1H-(X)RWL]}$	Delay time, H1 high to (X)R/$\overline{W}$ low	0*	13	0*	11	ns
14.1	$t_{d(H1L-A)}$	Delay time, H1 low to A valid	0*	11	0*	9	ns
14.2	$t_{d[H1L-(X)A]}$	Delay time, H1 low to (X)A valid	0*	9	0*	8	ns
15.1	$t_{su(D-H1L)R}$	Setup time, D valid before H1 low (read)	14		10		ns
15.2	$t_{su[(X)DR-H1L]R}$	Setup time, (X)D before H1 low (read)	16		14		ns
16	$t_{h[H1L-(X)D]R}$	Hold time, (X)D after H1 low (read)	0*		0*		ns
17.1	$t_{su(RDY-H1H)}$	Setup time, $\overline{RDY}$ before H1 high	8		6		ns
17.2	$t_{su[(X)RDY-H1H]}$	Setup time, $\overline{(X)RDY}$ before H1 high	9		8		ns
18	$t_{h[H1H-(X)RDY]}$	Hold time, $\overline{(X)RDY}$ after H1 high	0		0		ns
19	$t_{d[H1H-(X)RWH]W}$	Delay time, H1 high to (X)R/$\overline{W}$ high (write)		9		7	ns
20	$t_{v[H1L(X)D]W}$	Valid time, (X)D after H1 low (write)		17		14	ns
21	$t_{h[H1H-(X)D]W}$	Hold time, (X)D after H1 high (write)	0*		0*		ns
22.1	$t_{d(H1H-A)}$	Delay time, H1 high to A valid on back-to-back write cycles (write)		15		12	ns
22.2	$t_{d[H1H-(X)A]}$	Delay time, H1 high to (X)A valid on back-to-back write cycles (write)		21		18	ns
26	$t_{d[A-(X)RDY]}$	Delay time, $\overline{(X)RDY}$ from A valid		7*		6*	ns

† Numbers in this column match those used in Figure 10 and Figure 11.

* This parameter is not production tested.

memory read/write timing (continued)



NOTE A: (M)STRB remains low during back-to-back read operations.

Figure 10. Timing for Memory [(M)STRB = 0] Read

memory read/write timing (continued)

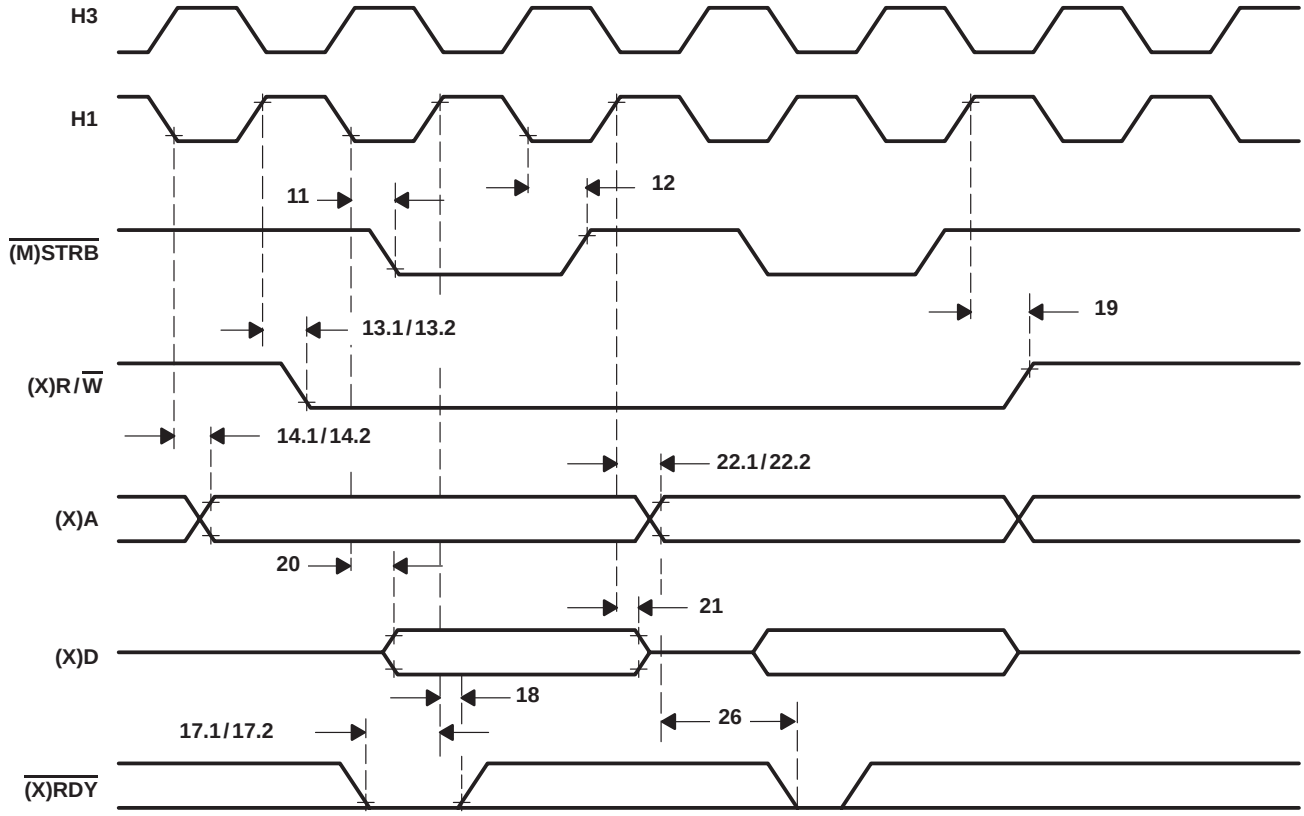


Figure 11. Timing for Memory [(M)STRB = 0] Write

memory read/write timing (continued)

The following table defines memory read timing parameters for $\overline{\text{IOSTRB}}$.

timing parameters for a memory ($\overline{\text{IOSTRB}}$ = 0) read (see Figure 12)

NO.†			320C30-40		320C30-50		UNIT
			MIN	MAX	MIN	MAX	
27	$t_{d(H1H-IOSL)}$	Delay time, H1 high to $\overline{\text{IOSTRB}}$ low	0*	9	0*	8	ns
28	$t_{d(H1H-IOSH)}$	Delay time, H1 high to $\overline{\text{IOSTRB}}$ high	0*	9	0*	8	ns
29	$t_{d[H1L-(X)RWH]}$	Delay time, H1 low to (X)R/$\overline{\text{W}}$ high	0*	9	0*	8	ns
30	$t_{d[H1L-(X)A]}$	Delay time, H1 low to (X)A valid	0*	9	0*	8	ns
31	$t_{su[(X)D-H1H]R}$	Setup time, (X)D before H1 high	13		11		ns
32	$t_{h[H1H-(X)D]R}$	Hold time, (X)D after H1 high	0*		0*		ns
33	$t_{su[(X)RDY-H1H]}$	Setup time, $\overline{\text{(X)RDY}}$ before H1 high	9		8		ns
34	$t_{h[H1H-(X)RDY]}$	Hold time, $\overline{\text{(X)RDY}}$ after H1 high	0		0		ns

† Numbers in this column match those used in Figure 12.
* This parameter is not production tested.

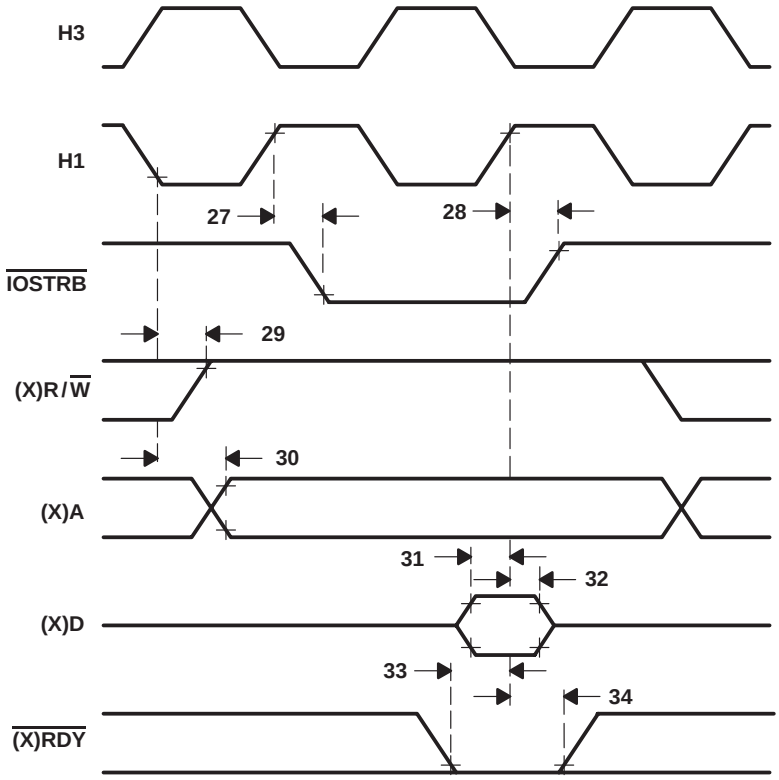


Figure 12. Timing for Memory ($\overline{\text{IOSTRB}}$ = 0) Read

memory read/write timing (continued)

The following table defines memory write timing parameters for $\overline{\text{IOSTRB}}$.

timing parameters for a memory ($\overline{\text{IOSTRB}}$ = 0) write (see Figure 13)

NO.†			320C30-40		320C30-50		UNIT
			MIN	MAX	MIN	MAX	
27	$t_{d(H1H-IOSL)}$	Delay time, H1 high to $\overline{\text{IOSTRB}}$ low	0*	9	0*	8	ns
28	$t_{d(H1H-IOSH)}$	Delay time, H1 high to $\overline{\text{IOSTRB}}$ high	0*	9	0*	8	ns
29	$t_{d[H1L-(X)RWH]}$	Delay time, H1 low to (X)R/$\overline{\text{W}}$ high	0*	9	0*	8	ns
30	$t_{d[H1L-(X)A]}$	Delay time, H1 low to (X)A valid	0*	9	0*	8	ns
33	$t_{su[(X)RDY-H1H]}$	Setup time, $\overline{\text{(X)RDY}}$ before H1 high	9		8		ns
34	$t_{h[H1H-(X)RDY]}$	Hold time, $\overline{\text{(X)RDY}}$ after H1 high	0		0		ns
35	$t_{d(H1L-XRWL)}$	Delay time, H1 low to XR/$\overline{\text{W}}$ low	0*	13	0*	11	ns
36	$t_{v[H1H(X)D]W}$	Valid time, (X)D after H1 high		25		20	ns
37	$t_{h[H1L-(X)D]W}$	Hold time, (X)D after H1 low	0		0		ns

† Numbers in this column match those used in Figure 13.
* This parameter is not production tested.

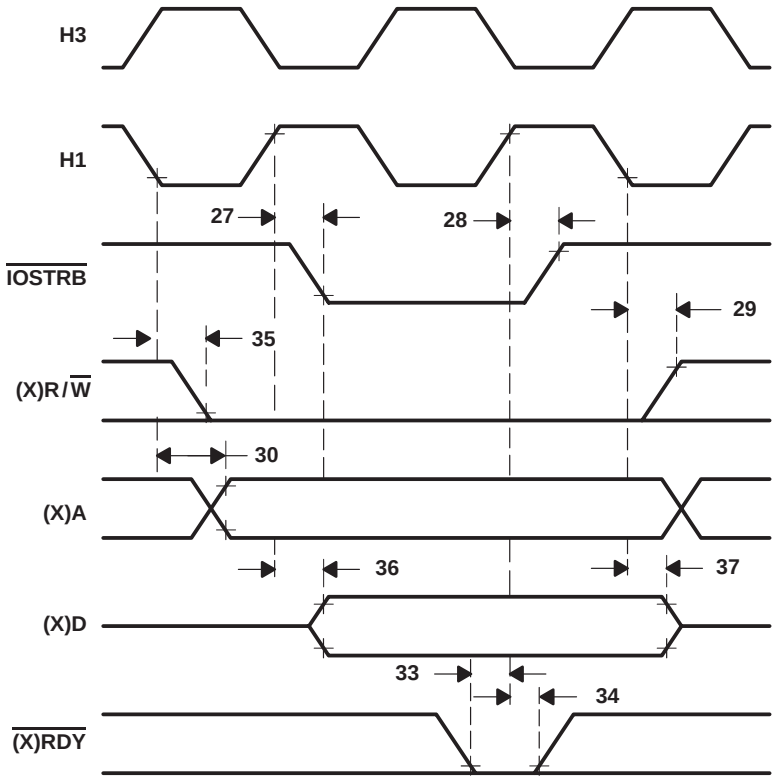


Figure 13. Timing for Memory ($\overline{\text{IOSTRB}}$ = 0) Write

XF0 and XF1 timing when executing LDFI or LDII

The following table defines the timing parameters for XF0 and XF1 during execution of LDFI or LDII.

timing parameters for XF0 and XF1 when executing LDFI or LDII (see Figure 14)

NO.†			320C30-40		320C30-50		UNIT
			MIN	MAX	MIN	MAX	
38	$t_{d(H3H-XF0L)}$	Delay time, H3 high to XF0 low		13		12	ns
39	$t_{su(XF1-H1L)}$	Setup time, XF1 valid before H1 low	9		9		ns
40	$t_{h(H1L-XF1)}$	Hold time, XF1 after H1 low	0		0		ns

† Numbers in this column match those used in Figure 14.

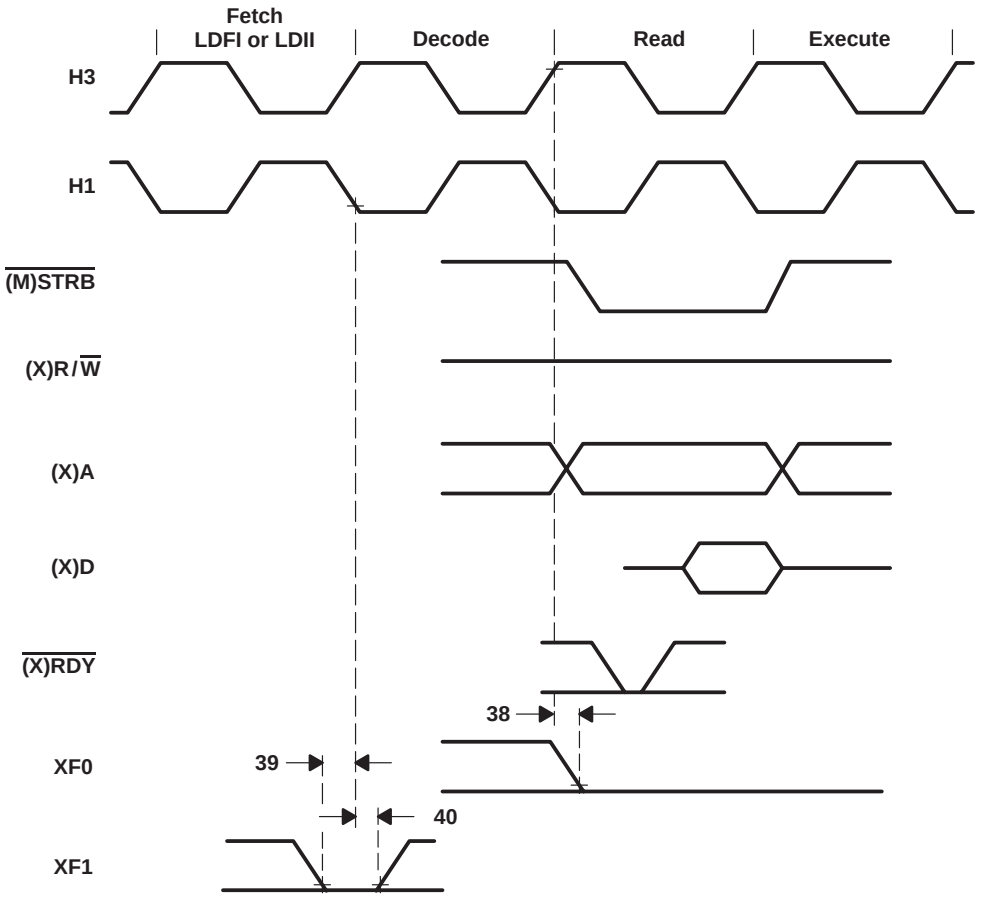


Figure 14. Timing for XF0 and XF1 When Executing LDFI or LDII

XF0 timing when executing STFI and STII

The following table defines the timing parameters for the XF0 pin during execution of STFI or STII.

timing parameters for XF0 when executing STFI or STII (see Figure 15)

NO.†		320C30-40		320C30-50		UNIT
		MIN	MAX	MIN	MAX	
41	$t_{d(H3H-XF0H)}$ Delay time, H3 high to XF0 high		13		12	ns

† The number in this column matches that used in Figure 15.

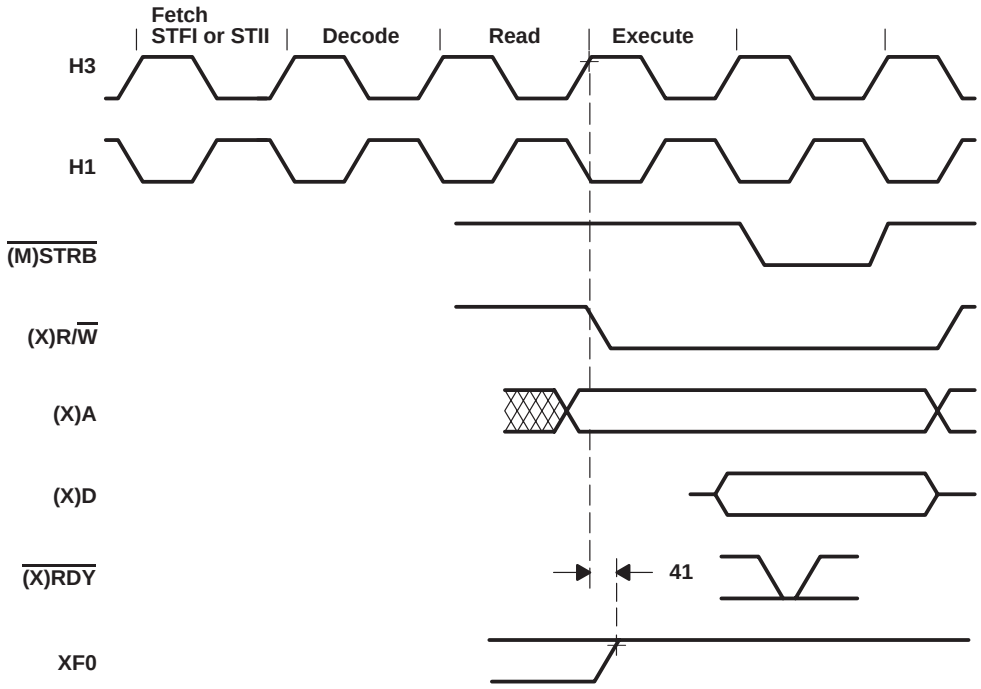


Figure 15. Timing for XF0 When Executing an STFI or STII

XF0 and XF1 timing when executing SIGI

The following table defines the timing parameters for the XF0 and XF1 pins during execution of SIGI.

timing parameters for XF0 and XF1 when executing SIGI (see Figure 16)

NO.†			320C30-40		320C30-50		UNIT
			MIN	MAX	MIN	MAX	
41.1	$t_{d(H3H-XF0L)}$	Delay time, H3 high to XF0 low		13		12	ns
42	$t_{d(H3H-XF0H)}$	Delay time, H3 high to XF0 high		13		12	ns
43	$t_{su(XF1-H1L)}$	Setup time, XF1 valid before H1 low	9		9		ns
44	$t_{h(H1L-XF1)}$	Hold time, XF1 after H1 low	0		0		ns

† Numbers in this column match those used in Figure 16.

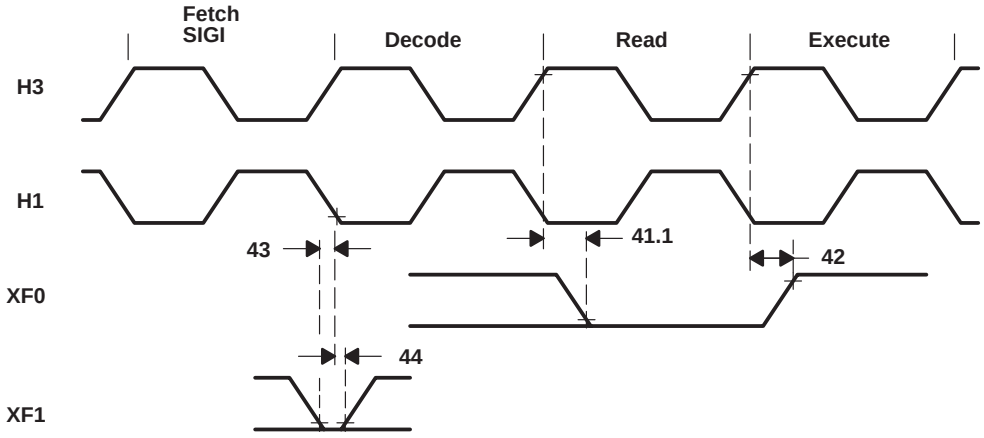


Figure 16. Timing for XF0 and XF1 When Executing SIGI

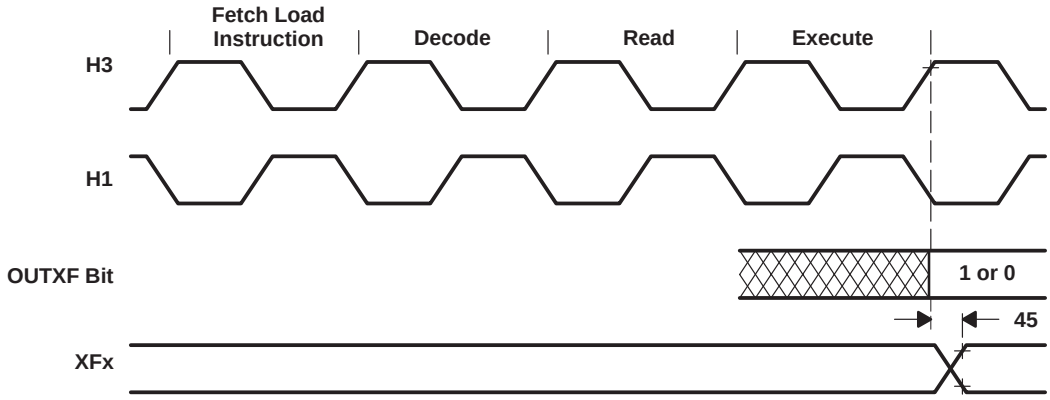
loading when XFx is configured as an output

The following table defines the timing parameter for loading the XF register when the XFx pin is configured as an output.

timing parameters for loading the XFx register when configured as an output pin (see Figure 17)

NO.†		320C30-40		320C30-50		UNIT
		MIN	MAX	MIN	MAX	
45	$t_{v(H3H-XF)}$ Valid time, H3 high to XF valid		13		12	ns

† The number in this column matches that used in Figure 17.



NOTE A: OUTXFx represents either bit 2 or 6 of the IOF register.

Figure 17. Timing for Loading XFx Register When Configured as an Output Pin

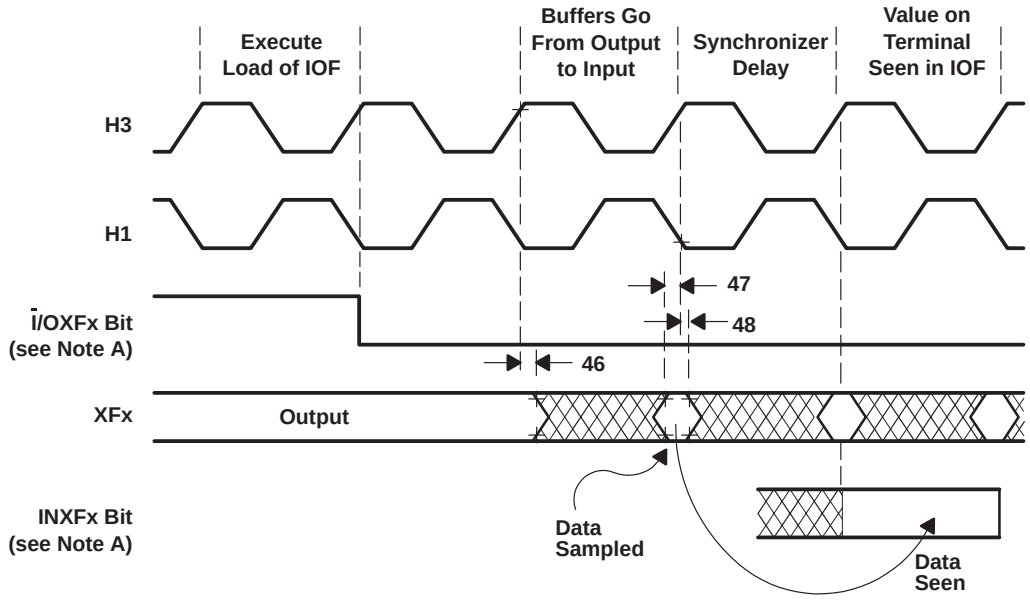
changing XFx from an output to an input

The following table defines the timing parameters for changing the XFx pin from an output pin to an input pin.

timing parameters of XFx changing from output to input mode (see Figure 18)

NO.†			320C30-40		320C30-50		UNIT
			MIN	MAX	MIN	MAX	
46	$t_{d(H3H-XFx)}$	Delay time, XFx after H3 high		13*		12*	ns
47	$t_{su(XFx-H1L)}$	Setup time, XFx before H1 low	9		9		ns
48	$t_{h(H1L-XFx)}$	Hold time, XFx after H1 low	0		0		ns

† Numbers in this column match those used in Figure 18.
* This parameter is not production tested.



NOTE A: Ī/OXFx represents either bit 1 or bit 5 of the IOF register, and INXFx represents either bit 3 or bit 7 of the IOF register depending on whether XF0 or XF1, respectively, is being affected.

Figure 18. Timing for Change of XFx From Output to Input Mode

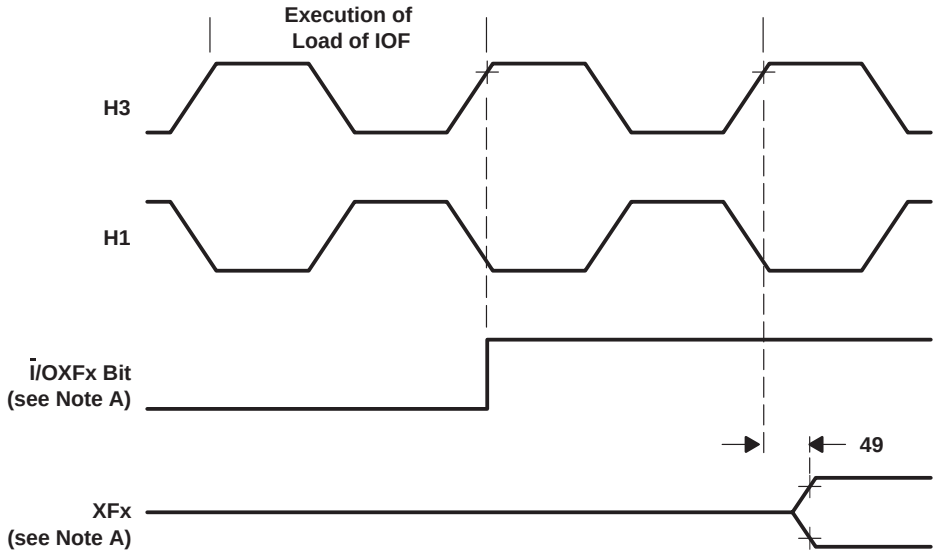
changing XFx from an input to an output

The following table defines the timing parameter for changing the XFx pin from an input pin to an output pin.

timing parameters of XFx changing from input to output mode (see Figure 19)

NO.†			320C30-40		320C30-50		UNIT
			MIN	MAX	MIN	MAX	
49	$t_{d(H3H-XFIO)}$	Delay time, H3 high to XF switching from input to output		17		17	ns

† The number in this column matches that used in Figure 19.



NOTE A: $\overline{I}$/OXFx represents either bit 1 or bit 5 of the IOF register, and INXFx represents either bit 3 or bit 7 of the IOF register depending on whether XF0 or XF1, respectively, is being affected.

Figure 19. Timing for Change of XFx From Input to Output Mode

reset timing

$\overline{\text{RESET}}$ is an asynchronous input that can be asserted at any time during a clock cycle. If the specified timings are met, the exact sequence shown in Figure 20 occurs; otherwise, an additional delay of one clock cycle can occur. R/$\overline{\text{W}}$ and XR/$\overline{\text{W}}$ are in the high-impedance state during reset and can be provided with a resistive pullup, nominally 18 kΩ to 22 kΩ, to prevent spurious writes from occurring. The asynchronous reset signals include XF0/1, CLKX0/1, DX0/1, FSX0/1, CLKR0/1, DR0/1, FSR0/1, and TCLK0/1. $\overline{\text{HOLD}}$ is an asynchronous input and can be asserted during reset.

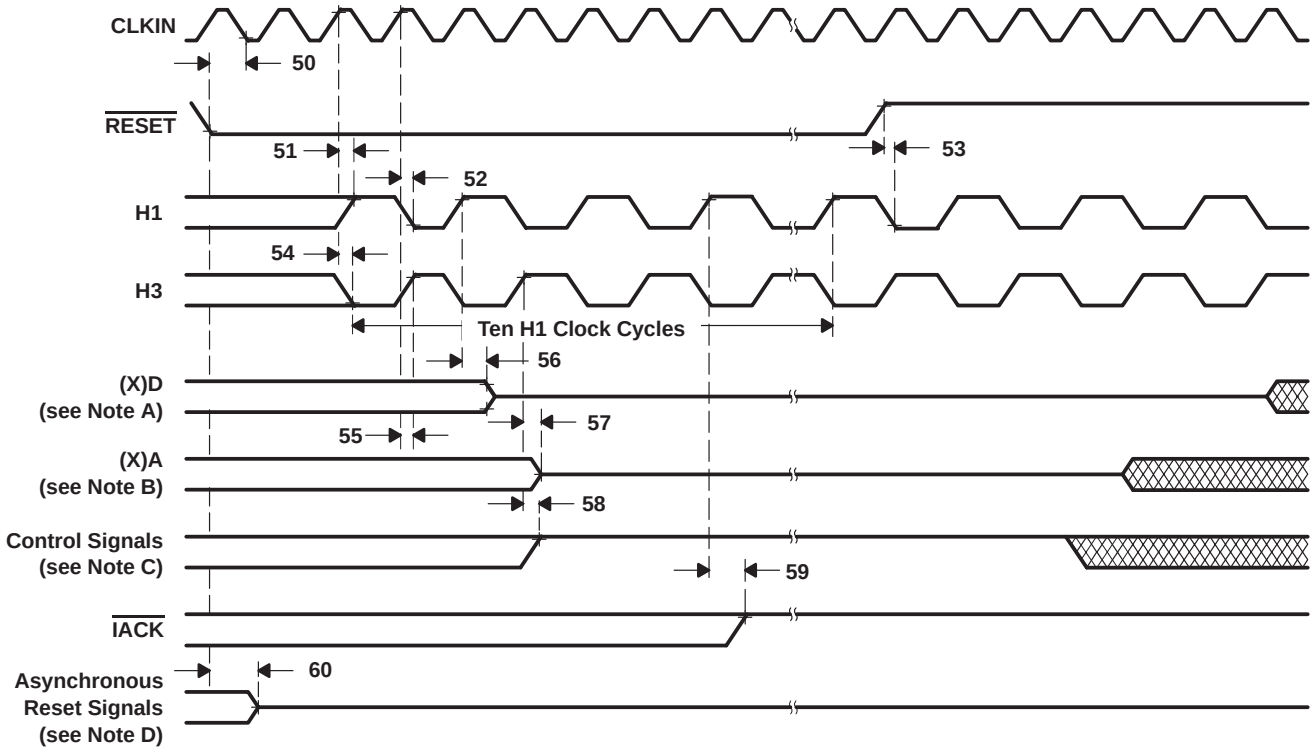
Resetting the device initializes the primary- and expansion-bus control registers to seven software wait states and, therefore, results in slow external accesses until these registers are initialized.

timing parameters for $\overline{\text{RESET}}$ [P = $t_{c(CI)}$] (see Figure 9 and Figure 20)

NO.			320C30-40		320C30-50		UNIT
			MIN	MAX	MIN	MAX	
50	$t_{su(RESET)}$	Setup time, $\overline{\text{RESET}}$ before CLKIN low	10	P*	10	P*	ns
51	$t_{d(CLKINH-H1H)}$	Delay time, CLKIN high to H1 high†	2	14	2	10	ns
52	$t_{d(CLKINH-H1L)}$	Delay time, CLKIN high to H1 low†	2	14	2	10	ns
53	$t_{su(RESETH-H1L)}$	Setup time, $\overline{\text{RESET}}$ high before H1 low after ten H1 clock cycles	9		7		ns
54	$t_{d(CLKINH-H3L)}$	Delay time, CLKIN high to H3 low†	2	14	2	10	ns
55	$t_{d(CLKINH-H3H)}$	Delay time, CLKIN high to H3 high†	2	14	2	10	ns
56	$t_{dis(H1H-XD)}$	Disable time, H1 high to (X)D high-impedance state		15*		12*	ns
57	$t_{dis(H3H-XA)}$	Disable time, H3 high to (X)A high-impedance state		9*		8*	ns
58	$t_{d(H3H-CONTROLH)}$	Delay time, H3 high to control signals high		9*		8*	ns
59	$t_{d(H1H-IACKH)}$	Delay time, H1 high to $\overline{\text{IACK}}$ high		9*		8*	ns
60	$t_{dis(RESETL-ASYNCH)}$	Disable time, $\overline{\text{RESET}}$ low to asynchronous reset signals in the high-impedance state		21*		17*	ns

† See Figure 9 for temperature dependence for the 40-MHz SMJ320C30.
* This parameter is not production tested.

reset timing (continued)



NOTES: A. In this diagram X(D) includes D31−D0 and XD31−XD0.
B. In this diagram, (X)A includes A23−A0 and XA12−XA0.
C. Control signals include STRB, MSTRB, and IOSTRB.
D. Asynchronous reset signals include XF1, XF0, CLKX0, DX0, FSX0, CLKR0, DR0, FSR0, CLKX1, DX1, FSX1, CLKR1, DR1, FSR1, TCLK0, and TCLK1.
E. In microprocessor mode, the reset vector is fetched twice, with seven software wait states each time. In micromputer mode, the reset vector is fetched twice, with no software wait states.

Figure 20. Timing for $\overline{\text{Reset}}$ [P=$t_{c(Cl)}$]

interrupt-response timing

The following table defines the timing parameters for the $\overline{INT}$ signals.

timing parameters for $\overline{INT3}$–$\overline{INT0}$ [Q = $t_{C(H)}$] (see Figure 21)

NO.			320C30-40		320C30-50		UNIT
			MIN	MAX	MIN	MAX	
61	$t_{su(INT)}$	Setup time, $\overline{INT3}$–$\overline{INT0}$ before H1 low	13		10		ns
62	$t_{w(INT)}$	Pulse duration, $\overline{INT3}$–$\overline{INT0}$, to assure only one interrupt seen	Q	< 2Q*	Q	< 2Q*	ns

* This parameter is not production tested.

The interrupt ($\overline{INT}$) pins are asynchronous inputs that can be asserted at any time during a clock cycle. The SMJ320C30 interrupts are level-sensitive, not edge-sensitive. Interrupts are detected on the falling edge of H1. Therefore, interrupts must be set up and held to the falling edge of H1 for proper detection. The CPU and DMA respond to detected interrupts on instruction-fetch boundaries only.

For the processor to recognize only one interrupt on a given input, an interrupt pulse must be set up and held to:

- A minimum of one H1 falling edge
- No more than two H1 falling edges

The SMJ320C30 can accept an interrupt from the same source every two H1 clock cycles.

If the specified timings are met, the exact sequence shown in Figure 21 occurs; otherwise, an additional delay of one clock cycle is possible.

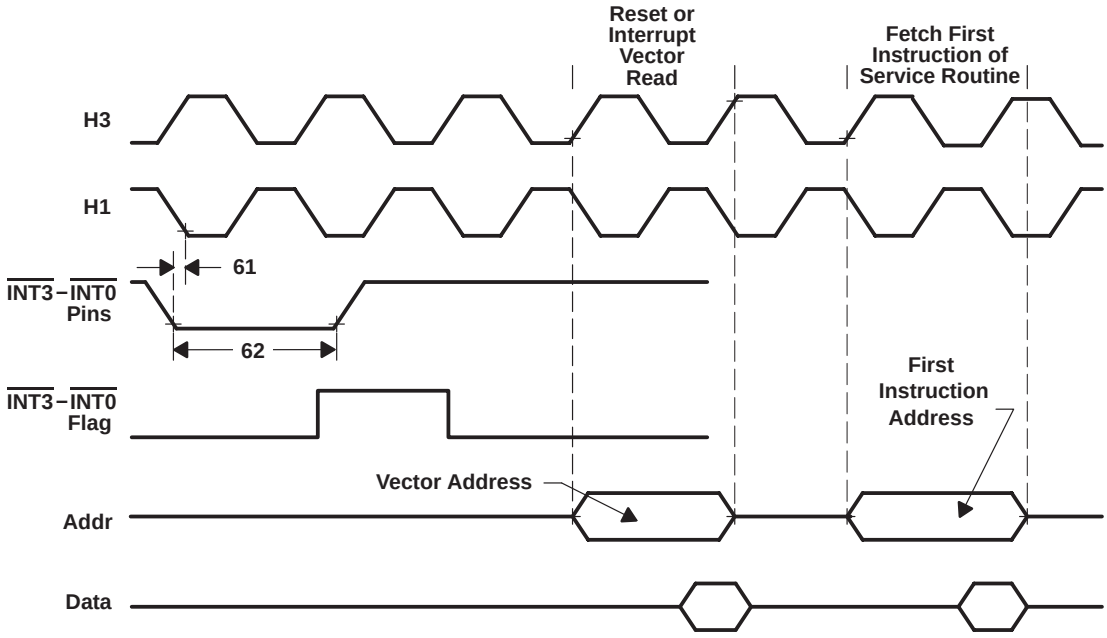


Figure 21. Timing for $\overline{INT3}$–$\overline{INT0}$ Response [Q=$t_{C(H)}$]

interrupt-acknowledge timing

The $\overline{\text{IACK}}$ output goes active on the first half-cycle (H1 rising) of the decode phase of the IACK instruction and goes inactive at the first half-cycle (H1 rising) of the read phase of the IACK instruction.

The following table defines the timing parameters for the $\overline{\text{IACK}}$ signal.

timing parameters for $\overline{\text{IACK}}$ (see Figure 22)

NO.†			320C30-40		320C30-50		UNIT
			MIN	MAX	MIN	MAX	
63	$t_{d(H1H-IACKL)}$	Delay time, H1 high to $\overline{\text{IACK}}$ low		9		7	ns
64	$t_{d(H1H-IACKH)}$	Delay time, H1 high to $\overline{\text{IACK}}$ high		9		7	ns

† Numbers in this column match those used in Figure 22.

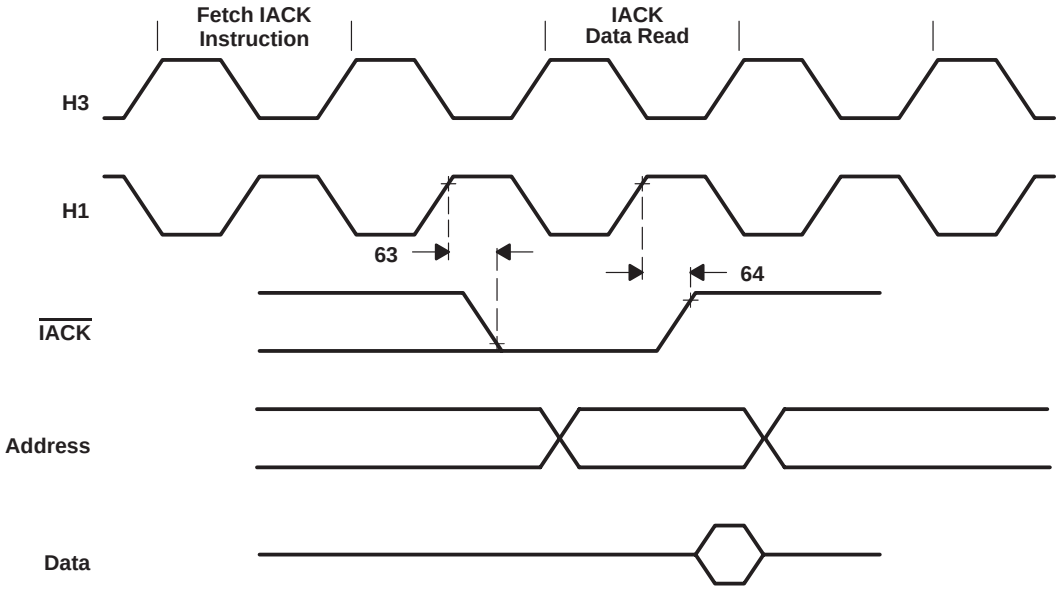


Figure 22. Timing for Interrupt-Acknowledge ($\overline{\text{IACK}}$)

serial-port timing parameters (see Figure 23 and Figure 24)

NO.			CLOCK SOURCE	320C30-40		320C30-50		UNIT
				MIN	MAX	MIN	MAX	
65	$t_{d(H1-SCK)}$	Delay time, H1 high to internal CLKX/R			13		10	ns
66	$t_{c(SCK)}$	Cycle time, CLKX/R	CLKX/R ext	$t_{c(H)}\times 2.5$*		$t_{c(H)}\times 2.6$*		ns
			CLKX/R int	$t_{c(H)}\times 2$	$t_{c(H)}\times 2^{32}$*	$t_{c(H)}\times 2$	$t_{c(H)}\times 2^{32}$*	
67	$t_{w(SCK)}$	Pulse duration, CLKX/R high/low	CLKX/R ext	$t_{c(H)}+12$*		$t_{c(H)}+10$*		ns
			CLKX/R int	$[t_{c(SCK)}/2]-15$	$[t_{c(SCK)}/2]+5$	$[t_{c(SCK)}/2]-5$	$[t_{c(SCK)}/2]+5$	
68	$t_{r(SCK)}$	Rise time, CLKX/R			7*		6*	ns
69	$t_{f(SCK)}$	Fall time, CLKX/R			7*		6*	ns
70	$t_{d(DX)}$	Delay time, CLKX to DX valid	CLKX ext		30		24	ns
			CLKX int		17		16	
71	$t_{su(DR)}$	Setup time, DR before CLKR low	CLKR ext	9		9		ns
			CLKR int	21		17		
72	$t_{h(DR)}$	Hold time, DR from CLKR low	CLKR ext	9		7		ns
			CLKR int	0		0		
73	$t_{d(FSX)}$	Delay time, CLKX to internal FSX high/low	CLKX ext		27		22	ns
			CLKX int		15		15	
74	$t_{su(FSR)}$	Setup time, FSR before CLKR low	CLKR ext	9		7		ns
			CLKR int	9		7		
75	$t_{h(FS)}$	Hold time, FSX/R input from CLKX/R low	CLKX/R ext	9		7		ns
			CLKX/R int	0		0		
76	$t_{su(FSX)}$	Setup time, external FSX before CLKX high	CLKX ext	$-[t_{c(H)}-8]$	$[t_{c(SCK)}/2]-10$*	$-[t_{c(H)}-8]$	$[t_{c(SCK)}/2]-10$*	ns
			CLKX int	$-[t_{c(H)}-21]$	$t_{c(SCK)}/2$*	$-[t_{c(H)}-21]$	$t_{c(SCK)}/2$*	
77	$t_{d(CH-DX)V}$	Delay time, CLKX to first DX bit, FSX precedes CLKX high	CLKX ext		30		24	ns
			CLKX int		18		14	
78	$t_{d(FSX-DX)V}$	Delay time, FSX to first DX bit, CLKX precedes FSX			30		24	ns
79	t_{dDXZ}	Delay time, CLKX high to DX high impedance following last data bit			17*		14*	ns

* This parameter is not production tested.

serial-port timing parameters (continued)

Unless otherwise indicated, the data-rate timings shown in Figure 23 and Figure 24 are valid for all serial-port modes, including handshake. See serial-port timing parameter tables.

Timing diagrams shown in Figure 23 and Figure 24 show operations with the serial port global-control register bits CLKXP = CLKRP = FSXP = FSRP = 0.

Timing diagrams shown in Figure 23 and Figure 24 depend upon the length of the serial-port word, n, where n = 8, 16, 24, or 32 bits, respectively.

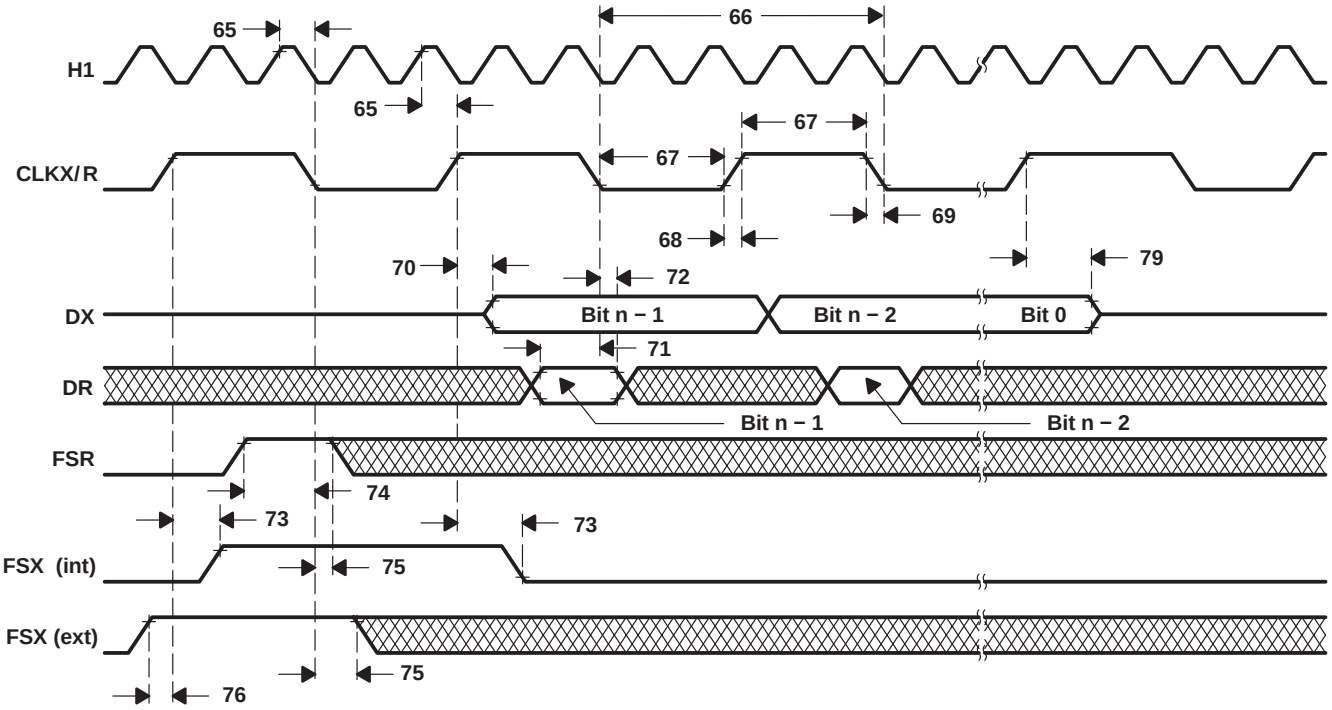
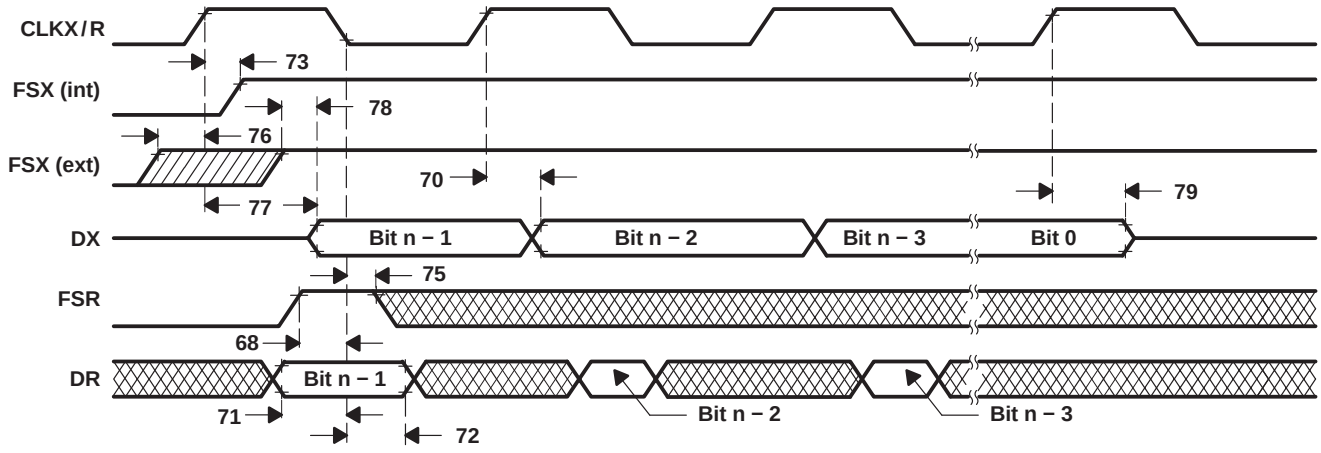


Figure 23. Serial-Port Timing for Fixed-Data-Rate Mode



NOTE A: Timings not expressly specified for variable-data-rate mode are the same as those for fixed-data-rate mode.

Figure 24. Serial-Port Timing for Variable-Data-Rate Mode

$\overline{\text{HOLD}}$ timing

$\overline{\text{HOLD}}$ is an asynchronous input that can be asserted at any time during a clock cycle. If the specified timings are met, the exact sequence shown in Figure 25 occurs; otherwise, an additional delay of one clock cycle is possible.

The “timing parameters for $\overline{\text{HOLD}}$/$\overline{\text{HOLDA}}$” table defines the timing parameters for the $\overline{\text{HOLD}}$ and $\overline{\text{HOLDA}}$ signals.

The NOHOLD bit of the primary bus control register overrides the $\overline{\text{HOLD}}$ signal. When this bit is set, the device comes out of hold and prevents future hold cycles.

Asserting $\overline{\text{HOLD}}$ prevents the processor from accessing the primary bus. Program execution continues until a read from or a write to the primary bus is requested. In certain circumstances, the first write is pending, allowing the processor to continue until a second write is encountered.

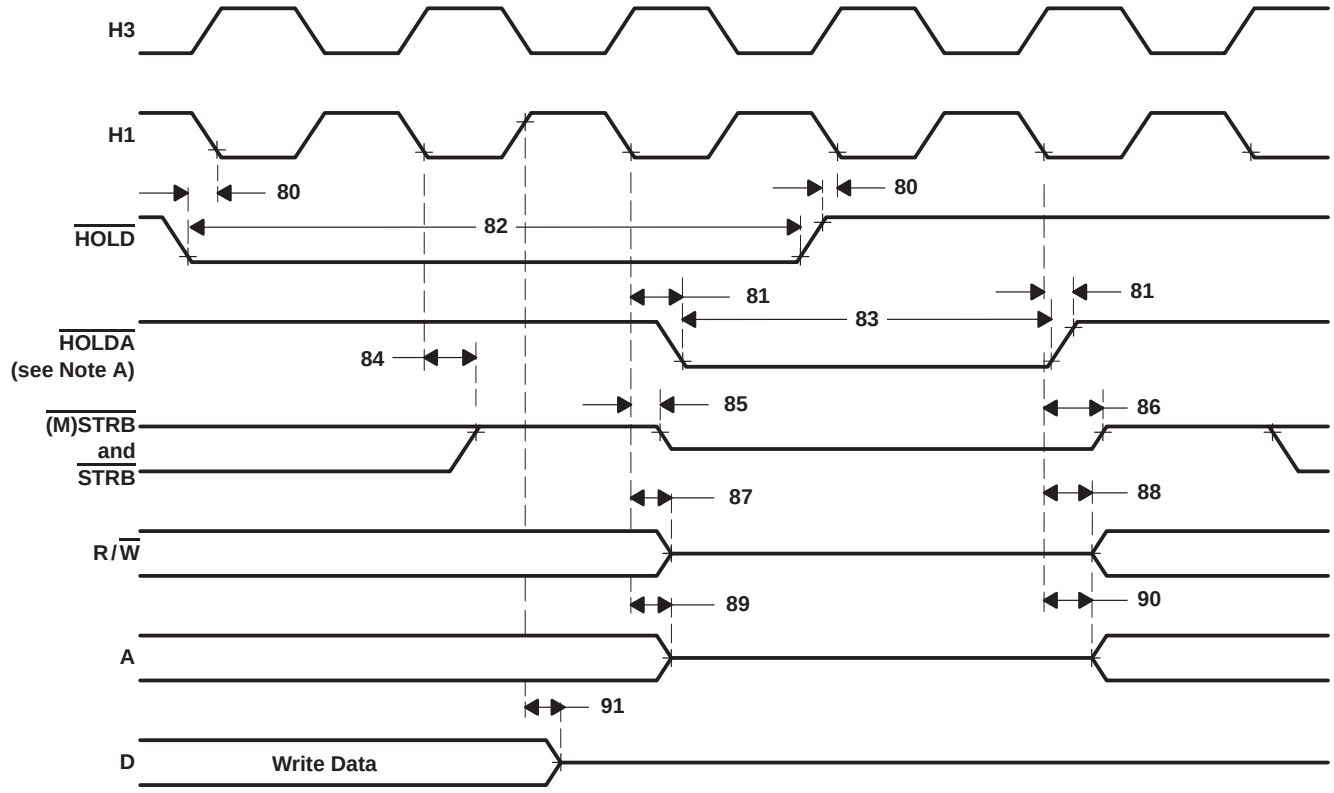
$\overline{\text{HOLD}}$/$\overline{\text{HOLDA}}$ timing (see Figure 25)

NO.†			320C30-40		320C30-50		UNIT
			MIN	MAX	MIN	MAX	
80	$t_{su(HOLD)}$	Setup time, $\overline{\text{HOLD}}$ before H1 low	13		10		ns
81	$t_{v(HOLDA)}$	Valid time, $\overline{\text{HOLDA}}$ after H1 low	0*	9	0*	7	ns
82	$t_{w(HOLD)}$	Pulse duration, $\overline{\text{HOLD}}$ low	$2t_{C(H)}$		$2t_{C(H)}$		ns
83	$t_{w(HOLDA)}$	Pulse duration, $\overline{\text{HOLDA}}$ low	$t_{C(H)}-5$*		$t_{C(H)}-5$*		ns
84	$t_{d(H1L-SH)H}$	Delay time, H1 low to $\overline{\text{STRB}}$ high for a $\overline{\text{HOLD}}$	0*	9*	0*	7*	ns
85	$t_{dis(H1L-S)}$	Disable time, H1 low to $\overline{\text{STRB}}$ high impedance	0*	9*	0*	8*	ns
86	$t_{en(H1L-S)}$	Enable time, H1 low to $\overline{\text{STRB}}$ active	0*	9*	0*	7*	ns
87	$t_{dis(H1L-RW)}$	Disable time, H1 low to R/$\overline{\text{W}}$ high impedance	0*	9*	0*	8*	ns
88	$t_{en(H1L-RW)}$	Enable time, H1 low to R/$\overline{\text{W}}$ active	0*	9*	0*	7*	ns
89	$t_{dis(H1L-A)}$	Disable time, H1 low to address high impedance	0*	9*	0*	8*	ns
90	$t_{en(H1L-A)}$	Enable time, H1 low to address valid	0*	13*	0*	12*	ns
91	$t_{dis(H1H-D)}$	Disable time, H1 high to data high impedance	0*	12*	0*	8*	ns

† Numbers in this column are used in Figure 25.

* This parameter is not production tested.

$\overline{\text{HOLD}}$/$\overline{\text{HOLDA}}$ timing (continued)



NOTE A: $\overline{\text{HOLDA}}$ goes low in response to $\overline{\text{HOLD}}$ going low and continues to remain low through one H1 cycle after $\overline{\text{HOLD}}$ returns to high.

Figure 25. Timing for $\overline{\text{HOLD}}$/$\overline{\text{HOLDA}}$

general-purpose I/O timing

Peripheral pins include CLKX0/1, CLKR0/1, DX0/1, DR0/1, FSX0/1, FSR0/1, and TCLK0/1. The contents of the internal-control registers associated with each peripheral define the modes for these pins.

peripheral pin I/O timing

The following table defines peripheral pin general-purpose I/O timing parameters.

timing parameters for peripheral pin general-purpose I/O (see Note 11 and Figure 26)

NO.†			320C30-40		320C30-50		UNIT
			MIN	MAX	MIN	MAX	
92	$t_{su(GPIOH1L)}$	Setup time, general-purpose input before H1 low	10*		9*		ns
93	$t_{h(GPIOH1L)}$	Hold time, general-purpose input after H1 low	0*		0*		ns
94	$t_{d(GPIOH1H)}$	Delay time, general-purpose output after H1 high		13*		10*	ns

† Numbers in this column are used in Figure 26.
* This parameter is not production tested.
NOTE 11: Peripheral pins include CLKX0/1, CLKR0/1, DX0/1, DR0/1, FSX0/1, FSR0/1, and TCLK0/1. The modes of these pins are defined by the contents of internal control registers associated with each peripheral.

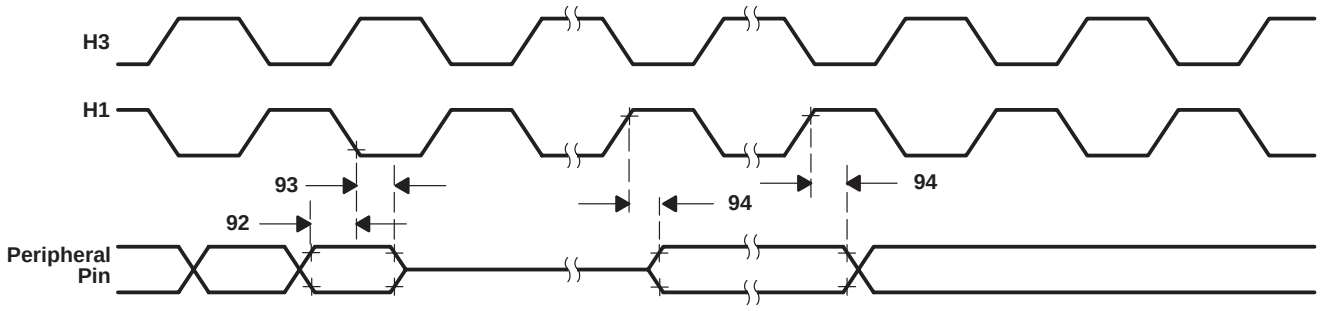


Figure 26. Timing for Peripheral Pin General-Purpose I/O

changing the peripheral pin I/O modes

The following tables show the timing parameters for changing the peripheral pin from a general-purpose output pin to a general-purpose input pin and the reverse.

timing parameters for peripheral pin changing from general-purpose output to input mode (see Note 12 and Figure 27)

NO.†			320C30-40		320C30-50		UNIT
			MIN	MAX	MIN	MAX	
95	$t_{h(H1H)}$	Hold time after H1 high		13		10	ns
96	$t_{su(GPIOH1L)}$	Setup time, peripheral pin before H1 low	9		9		ns
97	$t_{h(GPIOH1L)}$	Hold time, peripheral pin after H1 low	0		0		ns

† Numbers in this column are used in Figure 27.

NOTE 12: Peripheral pins include CLKX0/1, CLKR0/1, DX0/1, DR0/1, FSX0/1, FSR0/1, and TCLK0/1. The modes of these pins are defined by the contents of internal control registers associated with each peripheral.

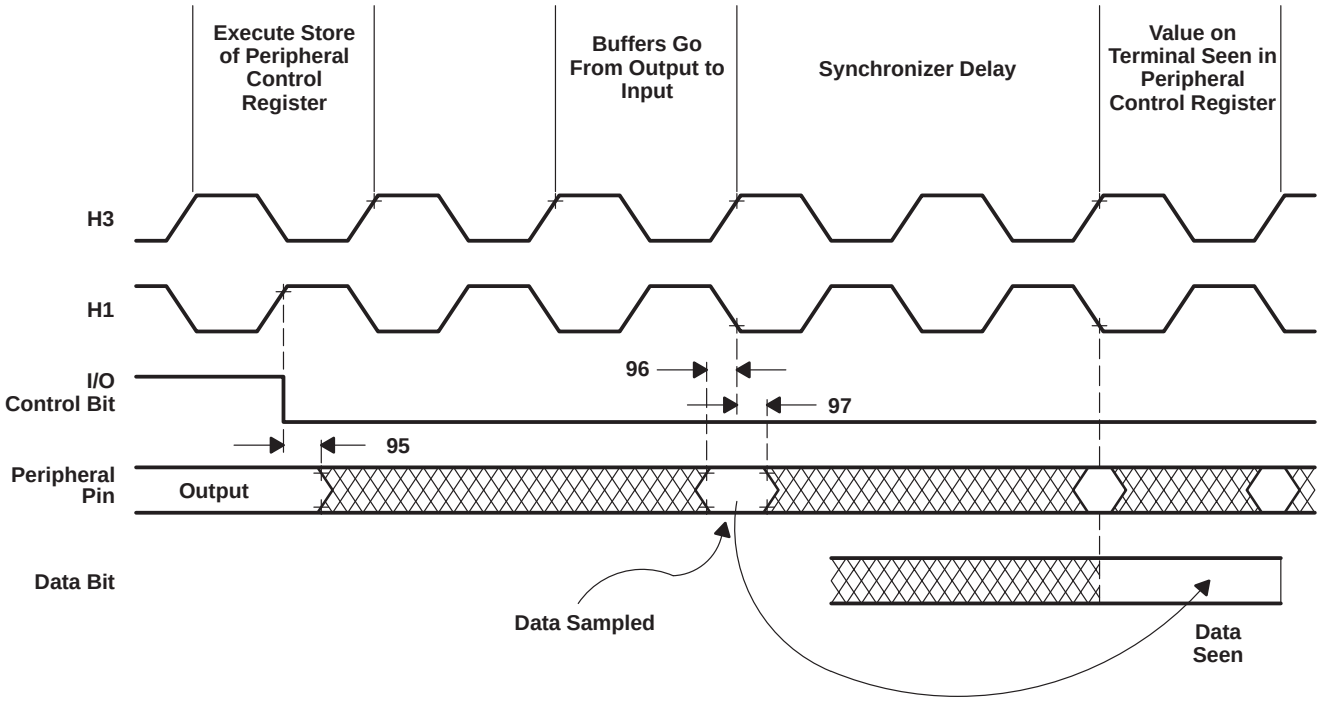


Figure 27. Timing for Change of Peripheral Pin From General-Purpose Output to Input Mode

timing parameters for peripheral pin changing from general-purpose input to output mode (see Figure 28)

NO.			320C30-40		320C30-50		UNIT
			MIN	MAX	MIN	MAX	
98	$t_{d(GPIOH1H)}$	Delay time, H1 high to peripheral pin switching from input to output		13		10	ns

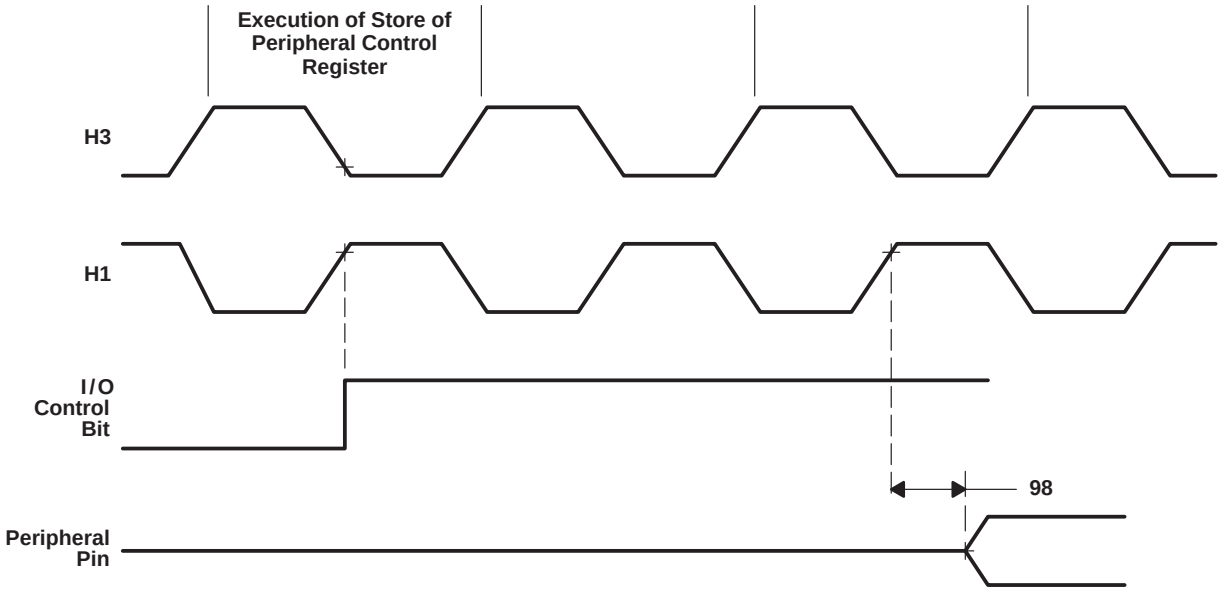


Figure 28. Timing for Change of Peripheral Pin From General-Purpose Input to Output Mode

timer pin (TCLK0 and TCLK1) timing

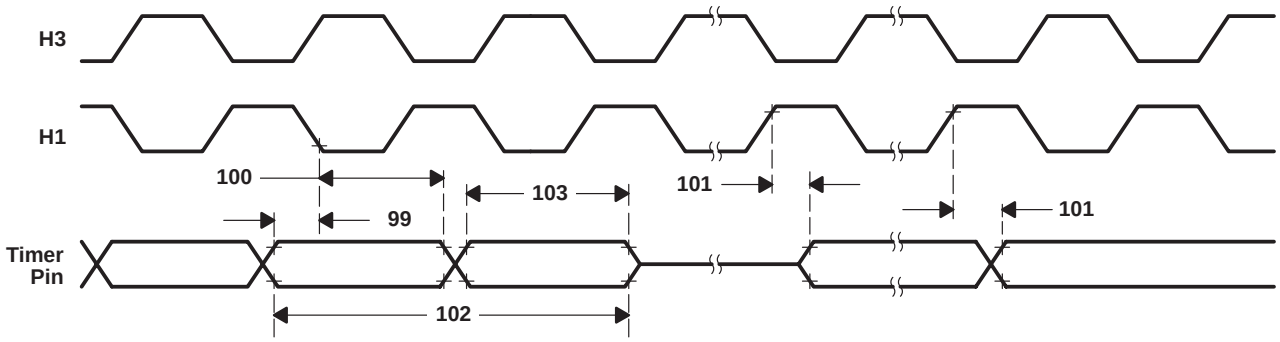
Valid logic-level periods and polarity are specified by the contents of the internal control registers.

The following table defines the timing parameters for the timer pin.

timing parameters for timer pin (TCLK0 and TCLK1) (see Figure 29)

NO.				320C30-40‡		320C30-50‡		UNIT
				MIN	MAX	MIN	MAX	
99	$t_{su(TCLK-H1L)}$	Setup time, TCLK ext before H1 low	TCLK ext	10		8		ns
100	$t_{h(TCLK-H1L)}$	Hold time, TCLK ext after H1 low	TCLK ext	0		0		ns
101	$t_{d(TCLK-H1H)}$	Delay time, H1 high to TCLK int valid	TCLK int		9		9	ns
102	$t_{c(TCLK)}$	Cycle time, TCLK	TCLK ext	$t_{c(H)} \times 2.6$*		$t_{c(H)} \times 2.6$*		ns
			TCLK int	$t_{c(H)} \times 2$	$t_{c(H)} \times 2^{32}$*	$t_{c(H)} \times 2$	$t_{c(H)} \times 2^{32}$*	ns
103	$t_{w(TCLK)}$	Pulse duration, TCLK high/low	TCLK ext	$t_{c(H)}$ + 12*		$t_{c(H)}$ + 10*		ns
			TCLK int	$[t_{c(TCLK)}/2]-5$	$[t_{c(TCLK)}/2]+5$	$[t_{c(TCLK)}/2]-5$	$[t_{c(TCLK)}/2]+5$	ns

† Numbers in this column are used in Figure 29.
‡ Timing parameters 99 and 100 are applicable for a synchronous input clock. Timing parameters 102 and 103 are applicable for an asynchronous input clock.
* This parameter is not production tested.



NOTE A: Period and polarity of valid logic level are specified by contents of internal control registers.

Figure 29. Timing for Timer Pin

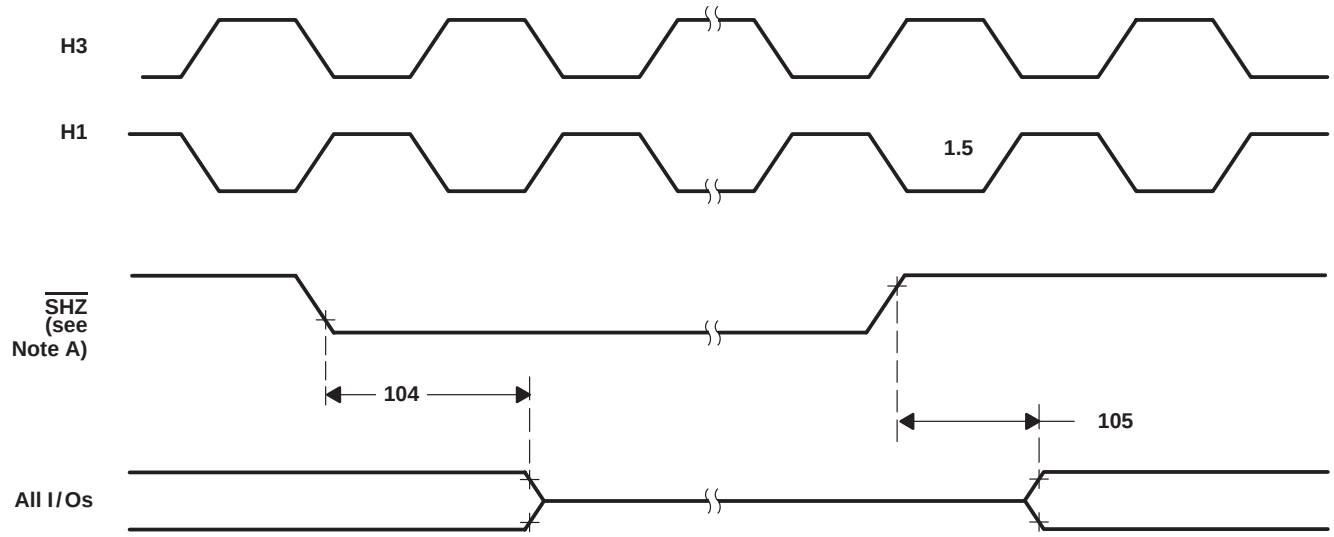
$\overline{\text{SHZ}}$ pin timing

The following table defines the timing parameter for the $\overline{\text{SHZ}}$ pin.

timing parameters for $\overline{\text{SHZ}}$ pin (see Figure 30)

NO.†			320C30-40 320C30-50		UNIT
			MIN	MAX	
104	$t_{dis(SHZ)}$	Disable time, $\overline{\text{SHZ}}$ low to all O, I/O high impedance	0*	3P + 15*	ns
105	$t_{en(SHZ)}$	Enable time, $\overline{\text{SHZ}}$ high to all O, I/O active	0*	2P*	ns

† Numbers in this column are used in Figure 30.
* This parameter is not production tested.



NOTE A: Enabling $\overline{\text{SHZ}}$ destroys SMJ320C30 register and memory contents. Assert $\overline{\text{SHZ}}$ and reset the SMJ320C30 to restore it to a known condition.

Figure 30. Timing for $\overline{\text{SHZ}}$

SMJ320C30 part order information

DEVICE	TECHNOLOGY	POWER SUPPLY	OPERATING FREQUENCY	PACKAGE TYPE	PROCESSING LEVEL
SMJ320C30GBM40	0.7-µm CMOS	5 V ± 5%	40 MHz	Ceramic 181-pin PGA	QML
SM320C30GBM40	0.7-µm CMOS	5 V ± 5%	40 MHz	Ceramic 181-pin PGA	Standard
SMJ320C30HFGM40	0.7-µm CMOS	5 V ± 5%	40 MHz	Ceramic 196-pin quad flatpack with nonconductive tie bar	QML
SM320C30HFGM40	0.7-µm CMOS	5 V ± 5%	40 MHz	Ceramic 196-pin quad flatpack with nonconductive tie bar	Standard
5962−9052604MXA	0.7-µm CMOS	5 V ± 5%	40 MHz	Ceramic 181-pin PGA	DESC SMD
5962−9052604MUA	0.7-µm CMOS	5 V ± 5%	40 MHz	Ceramic 196-pin quad flatpack with nonconductive tie bar	DESC SMD
SMJ320C30GBM50	0.7-µm CMOS	5 V ± 5%	50 MHz	Ceramic 181-pin PGA	QML
SM320C30GBM50	0.7-µm CMOS	5 V ± 5%	50 MHz	Ceramic 181-pin PGA	Standard
SMJ320C30HFGM50	0.7-µm CMOS	5 V ± 5%	50 MHz	Ceramic 196-pin quad flatpack with nonconductive tie bar	QML
SM320C30HFGM50	0.7-µm CMOS	5 V ± 5%	50 MHz	Ceramic 196-pin quad flatpack with nonconductive tie bar	Standard
5962−9052605MXA	0.7-µm CMOS	5 V ± 5%	50 MHz	Ceramic 181-pin PGA	DESC SMD
5962−9052605MUA	0.7-µm CMOS	5 V ± 5%	50 MHz	Ceramic 196-pin quad flatpack with nonconductive tie bar	DESC SMD

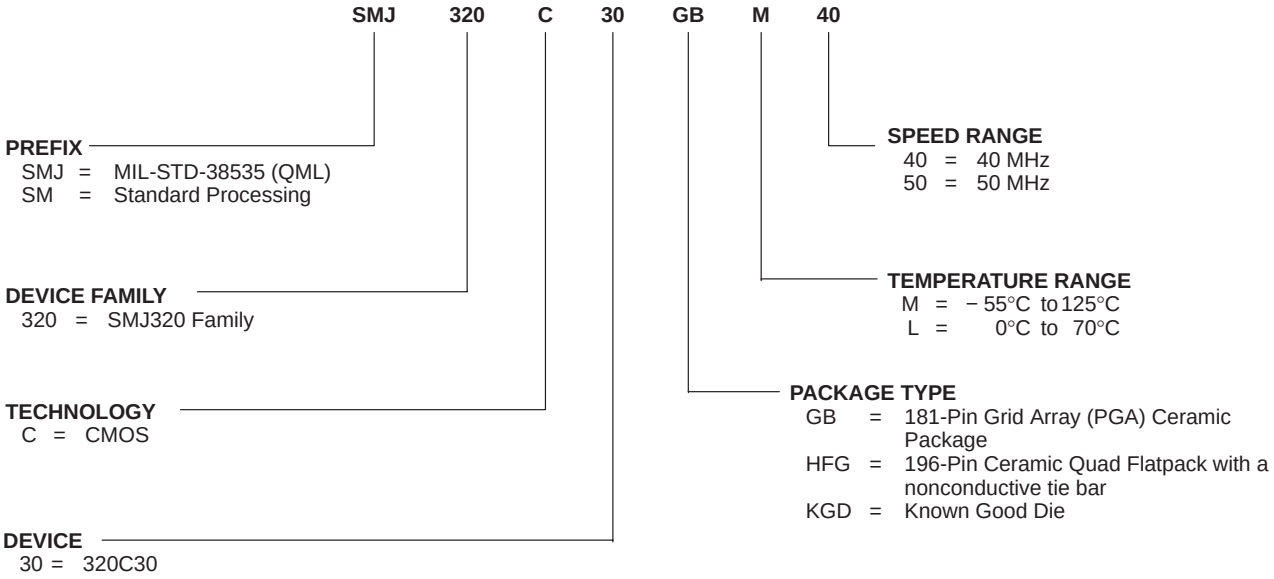
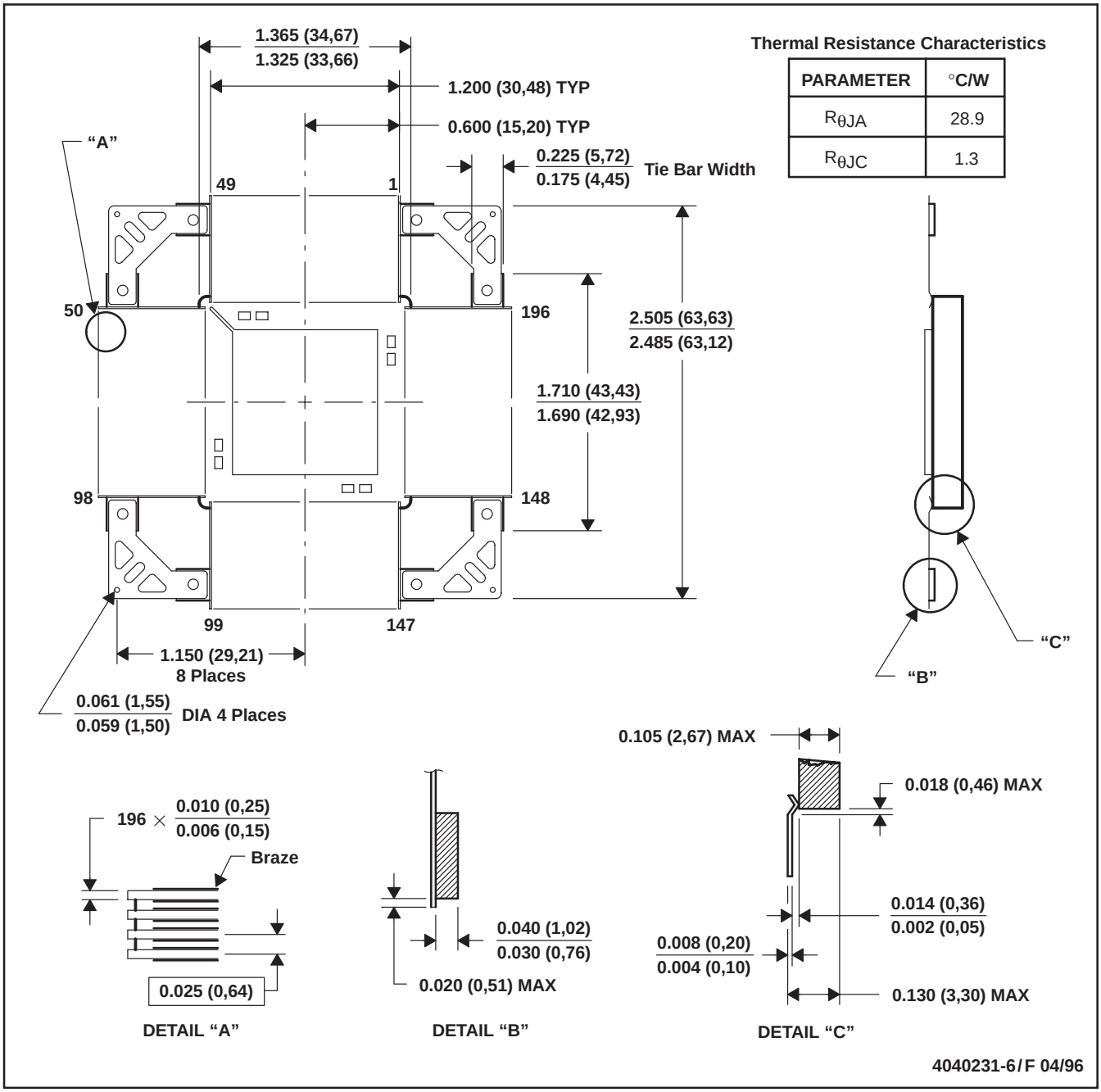


Figure 31. SMJ320C30 Device Nomenclature

SOURCED FROM: SGUS014H − FEBRUARY 1991 − REVISED JUNE 2004

MECHANICAL DATA

HFG (S-CQFP-F196) **CERAMIC QUAD FLATPACK WITH TIE BAR**



Thermal Resistance Characteristics

PARAMETER	°C/W
$R_{\theta JA}$	28.9
$R_{\theta JC}$	1.3

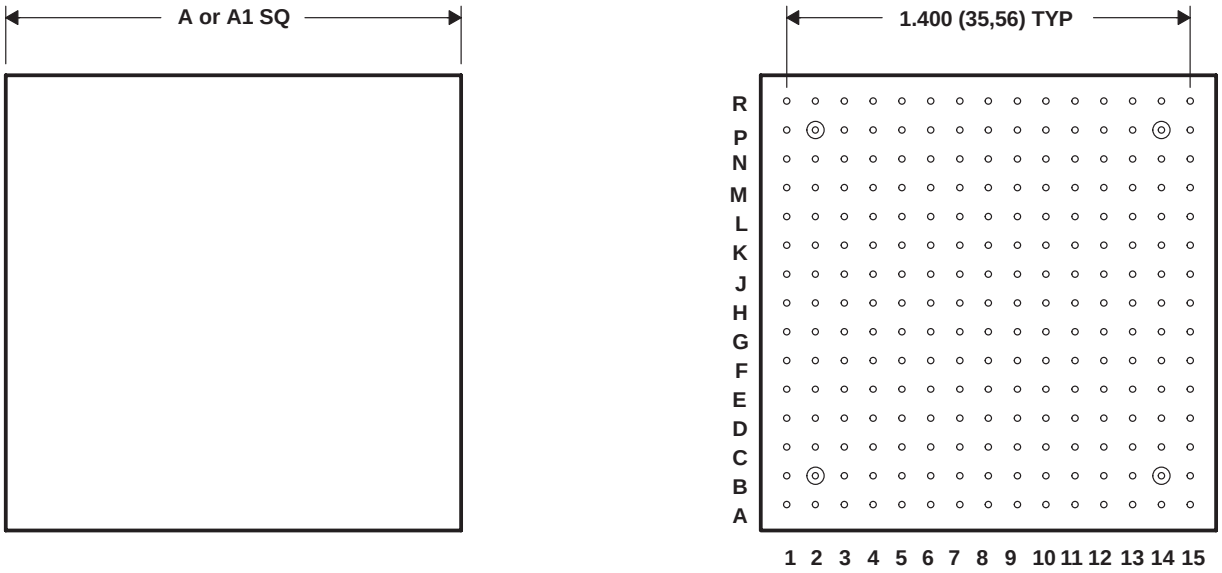
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Ceramic quad flatpack with flat leads brazed to nonconductive tie-bar carrier
D. This package can be hermetically sealed with a metal lid.
E. The terminals will be gold plated.
F. Falls within JEDEC MO-113 AB

The above data applies to the SMJ320C30 196-pin QFP.

SOURCED FROM: SGUS014H − FEBRUARY 1991 − REVISED JUNE 2004

MECHANICAL DATA (CONTINUED)

GA-GB (S-CPGA-P15 X 15) **CERAMIC PIN GRID ARRAY PACKAGE**



DIM	MIN	MAX	Notes
A	1.540 (39,12)	1.590 (40,38)	Large Outline
A1	1.480 (37,59)	1.535 (38,99)	Small Outline
B	0.110 (2,79)	0.205 (5,21)	Cavity Up
B1	0.095 (2,41)	0.205 (5,21)	Cavity Down
C	0.040 (1,02)	0.060 (1,52)	Cavity Up
C1	0.025 (0,63)	0.060 (1,52)	Cavity Down
MAXIMUM PINS WITHIN MATRIX − 225			

4040114-8/C 04/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Index mark may appear on top or bottom depending on package vendor.
D. Pins are located within 0.010 (0,25) diameter of true position relative to each other at maximum material condition and within 0.030 (0,76) diameter relative to the edges of the ceramic.
E. This package can be hermetically sealed with metal lids or with ceramic lids using glass frit.
F. The pins can be gold plated or solder dipped.
G. Falls within MIL-STD-1835 CMGA7-PN and CMGA19-PN and JEDEC MO-067AG and MO-066AG, respectively

Thermal Resistance Characteristics

PARAMETER	°C/W
$R_{\theta JA}$	26.6
$R_{\theta JC}$	1.1

The above data applies to the SMJ320C30 181-pin PGA.

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
5962-9052604MUA	ACTIVE	CFP	HFG	196	1	TBD	Call TI	Level-NC-NC-NC
5962-9052604MXA	ACTIVE	CPGA	GB	181	1	TBD	Call TI	Level-NC-NC-NC
5962-9052604Q9A	OBSOLETE	XCEPT	KGD	0		TBD	Call TI	Call TI
5962-9052605MUA	ACTIVE	CFP	HFG	196	4	TBD	Call TI	Level-NC-NC-NC
5962-9052605MXA	ACTIVE	CPGA	GB	181	1	TBD	Call TI	Level-NC-NC-NC
5962-9052605QXC	ACTIVE	CPGA	GB	181	1	TBD	Call TI	Level-NC-NC-NC
SM320C30GBM40	ACTIVE	CPGA	GB	181	1	TBD	Call TI	Level-NC-NC-NC
SM320C30GBM50	ACTIVE	CPGA	GB	181	1	TBD	Call TI	Level-NC-NC-NC
SM320C30HFGM40	ACTIVE	CFP	HFG	196	1	TBD	Call TI	Level-NC-NC-NC
SM320C30HFGM50	ACTIVE	CFP	HFG	196	1	TBD	Call TI	Level-NC-NC-NC
SMJ320C30GBM40	ACTIVE	CPGA	GB	181	1	TBD	Call TI	Level-NC-NC-NC
SMJ320C30GBM50	ACTIVE	CPGA	GB	181	1	TBD	Call TI	Level-NC-NC-NC
SMJ320C30HFGM40	ACTIVE	CFP	HFG	196	1	TBD	Call TI	Level-NC-NC-NC
SMJ320C30HFGM50	ACTIVE	CFP	HFG	196	4	TBD	Call TI	Level-NC-NC-NC

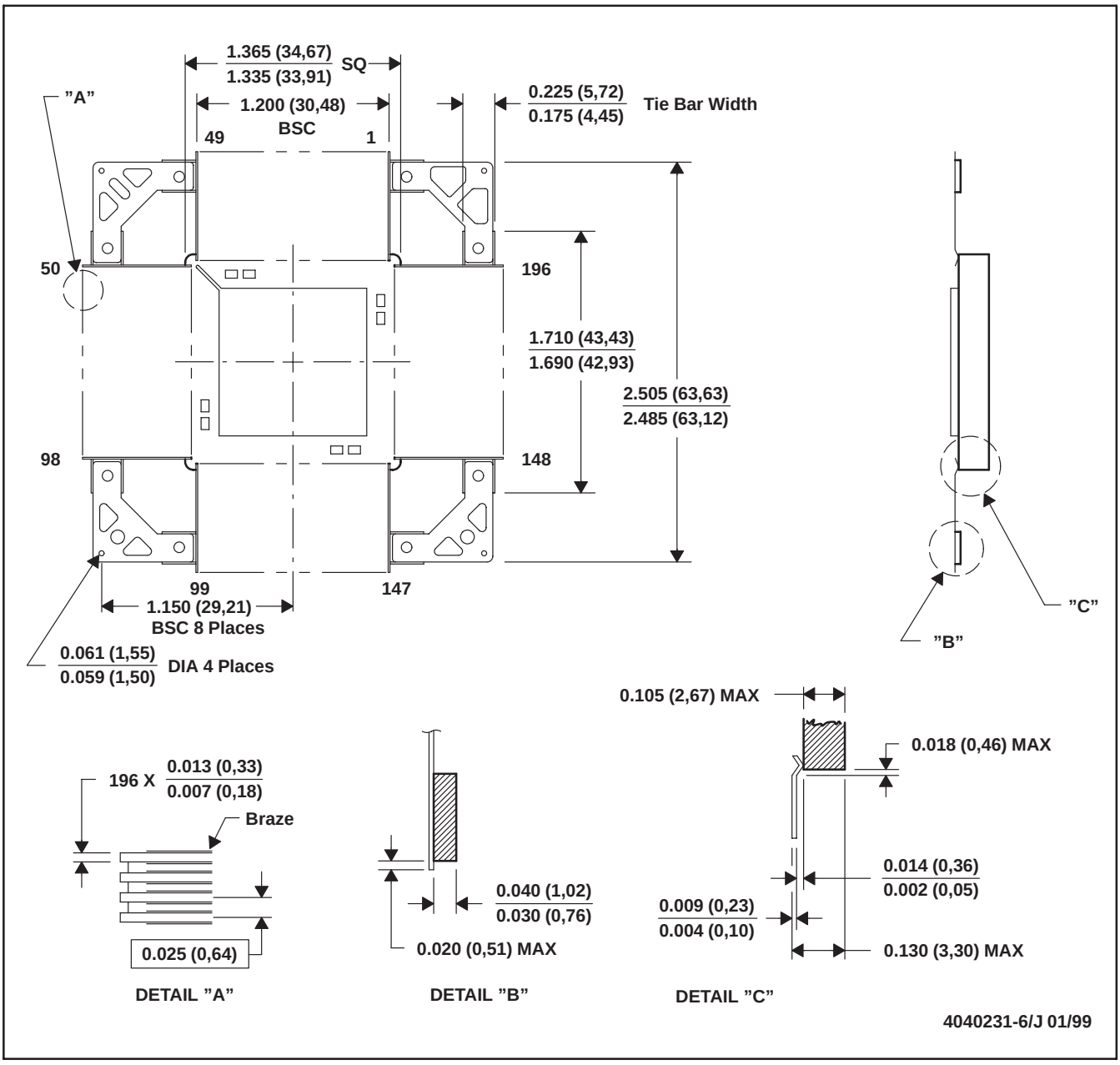
[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

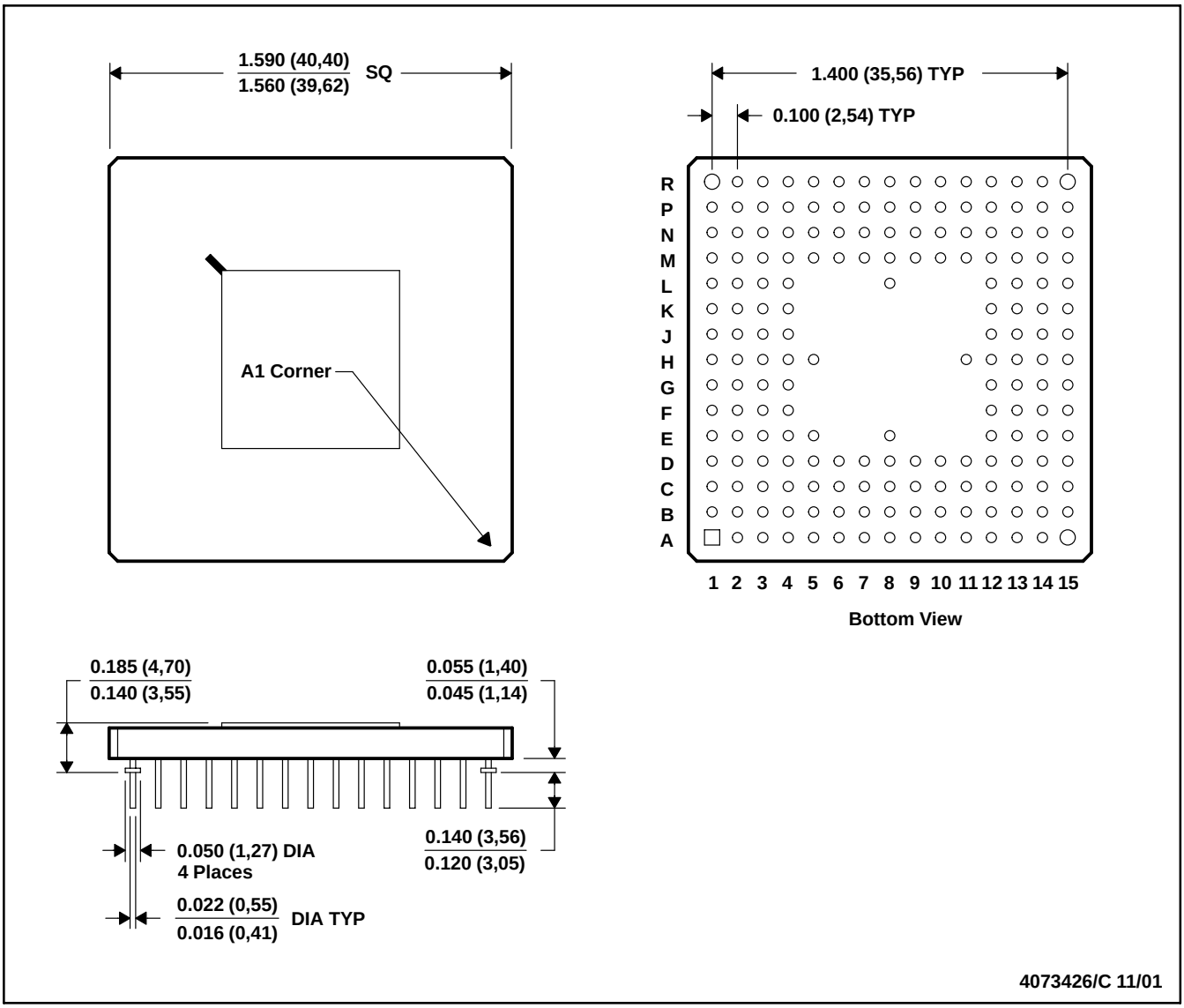
MCFP023C – JANUARY 1995 – REVISED JUNE 1999

HFG (S-CQFP-F196) **CERAMIC QUAD FLATPACK WITH NCTB**



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Ceramic quad flatpack with flat leads brazed to non-conductive tie bar carrier
D. This package is hermetically sealed with a metal lid.
E. The leads are gold-plated and can be solder-dipped.
F. Leads not shown for clarity purposes
G. Falls within JEDEC MO-113AB

GB (S-CPGA-P181) **CERAMIC PIN GRID ARRAY**



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Index mark can appear on top or bottom, depending on package vendor.
D. Pins are located within 0.010 (0,25) diameter of true position relative to each other at maximum material condition and within 0.030 (0,76) diameter relative to the edge of the ceramic.
E. This package can be hermetically sealed with metal lids or with ceramic lids using glass frit.
F. The pins can be gold-plated or solder-dipped.
G. Falls within MIL-STD-1835 CMGA7-PN

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