



## 3.0V/3.3V Microprocessor Supervisory Circuits

### General Description

These microprocessor ( $\mu$ P) supervisory circuits reduce the complexity and number of components required for power-supply monitoring and battery-control functions in  $\mu$ P systems. They significantly improve system reliability and accuracy compared to separate ICs or discrete components.

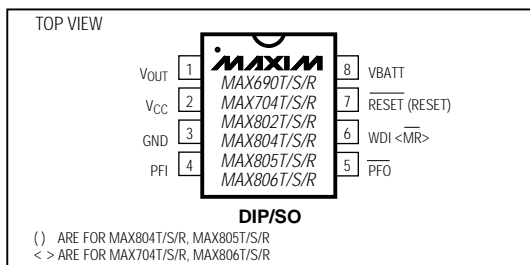
These devices are designed for use in systems powered by 3.0V or 3.3V supplies. See the selector guide in the back of this data sheet for similar devices designed for 5V systems. The suffixes denote different reset threshold voltages: 3.075V (T), 2.925V (S), and 2.625V (R) (see *Reset Threshold* section in the *Detailed Description*). All these parts are available in 8-pin DIP and SO packages. Functions offered in this series are as follows:

Part	Active-Low Reset	Active-High Reset	Watchdog Input	Manual Reset Input	Threshold Accuracy	Power-Fail Comparator	Reset Window
MAX690	✓			✓	±4%	✓	±75mV
MAX704	✓			✓	±4%	✓	±75mV
MAX802	✓		✓		±2%	✓	±2%
MAX804		✓	✓		±2%	✓	±2%
MAX805		✓	✓		±4%	✓	±75mV
MAX806	✓			✓	±2%	✓	±2%

### Applications

Battery-Powered Computers and Controllers  
Embedded Controllers  
Intelligent Instruments  
Automotive Systems  
Critical  $\mu$ P Power Monitoring  
Portable Equipment

### Pin Configuration



### Features

- ♦ **RESET and RESET Outputs**
- ♦ **Manual Reset Input**
- ♦ **Precision Supply-Voltage Monitor**
- ♦ **200ms Reset Time Delay**
- ♦ **Watchdog Timer (1.6sec timeout)**
- ♦ **Battery-Backup Power Switching—  
Battery Can Exceed  $V_{CC}$  in Normal Operation**
- ♦ **40 $\mu$ A  $V_{CC}$  Supply Current**
- ♦ **1 $\mu$ A Battery Supply Current**
- ♦ **Voltage Monitor for Power-Fail or Low-Battery Warning**
- ♦ **Guaranteed RESET Assertion to  $V_{CC} = 1V$**
- ♦ **8-Pin DIP and SO Packages**

### Ordering Information

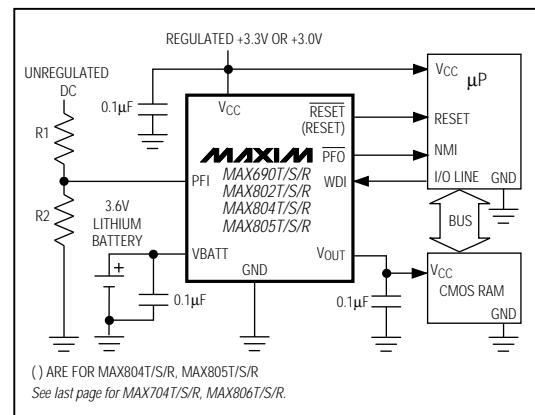
PART**	TEMP. RANGE	PIN-PACKAGE
MAX690_CPA	0°C to +70°C	8 Plastic DIP
MAX690_CSA	0°C to +70°C	8 SO
MAX690_C/D	0°C to +70°C	Dice*
MAX690_EPA	-40°C to +85°C	8 Plastic DIP
MAX690_ESA	-40°C to +85°C	8 SO
MAX690_MJA	-55°C to +125°C	8 CERDIP

Ordering Information continued on last page.

\* Contact factory for dice specifications.

\*\* These parts offer a choice of reset threshold voltage. Select the letter corresponding to the desired nominal reset threshold voltage (T = 3.075V, S = 2.925V, R = 2.625V) and insert it into the blank to complete the part number.

### Typical Operating Circuits



( ) ARE FOR MAX804T/S/R, MAX805T/S/R  
See last page for MAX704T/S/R, MAX806T/S/R.



Maxim Integrated Products 1

Call toll free 1-800-998-8800 for free samples or literature.

MAX690T/S/R, 704T/S/R, 802T/S/R, 804-806T/S/R

## 3.0V/3.3V Microprocessor Supervisory Circuits

### ABSOLUTE MAXIMUM RATINGS

Terminal Voltage (with respect to GND)

V<sub>CC</sub> ..... -0.3V to 6.0V

VBATT ..... -0.3V to 6.0V

All Other Inputs ..... -0.3V to the higher of V<sub>CC</sub> or VBATT

Continuous Input Current

V<sub>CC</sub> ..... 100mA

VBATT ..... 18mA

GND ..... 18mA

Output Current

RESET, PFO ..... 18mA

V<sub>OUT</sub> ..... 100mA

Continuous Power Dissipation (T<sub>A</sub> = +70°C)

Plastic DIP (derate 9.09mW/°C above +70°C) ..... 727mW

SO (derate 5.88mW/°C above +70°C) ..... 471mW

CERDIP (derate 8.00mW/°C above +70°C) ..... 640mW

Operating Temperature Ranges

MAX690\_C\_/MAX704\_C\_/MAX80\_C\_ ..... 0°C to +70°C

MAX690\_E\_/MAX704\_E\_/MAX80\_E\_ ..... -40°C to +85°C

MAX690\_M\_/MAX704\_M\_/MAX80\_M\_ ..... -55°C to +125°C

Storage Temperature Range ..... -65°C to +160°C

Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### ELECTRICAL CHARACTERISTICS

(V<sub>CC</sub> = 3.17V to 5.5V for the MAX690T/MAX704T/MAX80\_T, V<sub>CC</sub> = 3.02V to 5.5V for the MAX690S/MAX704S/MAX80\_S, V<sub>CC</sub> = 2.72V to 5.5V for the MAX690R/MAX704R/MAX80\_R; VBATT = 3.6V; T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>; unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range, V <sub>CC</sub> , VBATT (Note 1)		MAX690_C, MAX704_C, MAX80_C	1.0		5.5	V
		MAX690_E/M, MAX704_E/M, MAX80_E/M	1.1		5.5	
V <sub>CC</sub> Supply Current (excluding I <sub>OUT</sub> )	I <sub>SUPPLY</sub>	MR = V <sub>CC</sub> (MAX704_/MAX806_) MAX690_C/E, MAX704_C/E, MAX80_C/E, V <sub>CC</sub> < 3.6V		40	50	μA
		MAX690_C/E, MAX704_C/E, MAX80_C/E, V <sub>CC</sub> < 5.5V		50	65	
		MAX690_M, MAX704_M, MAX80_M, V <sub>CC</sub> < 3.6V		40	55	
		MAX690_M, MAX704_M, MAX80_M, V <sub>CC</sub> < 5.5V		50	70	
V <sub>CC</sub> Supply Current in Battery-Backup Mode (excluding I <sub>OUT</sub> )		MR = V <sub>CC</sub> (MAX704_/MAX806_) V <sub>CC</sub> = 2.0V, VBATT = 2.3V		25	50	μA
VBATT Supply Current, Any Mode (excluding I <sub>OUT</sub> ) (Note 2)		MAX690_C/E, MAX704_C/E, MAX80_C/E		0.4	1	μA
		MAX690_M, MAX704_M, MAX80_M		0.4	10	
Battery Leakage Current (Note 3)		MAX690_C/E, MAX704_C/E, MAX80_C/E		0.01	0.5	μA
		MAX690_M, MAX704_M, MAX80_M		0.01	5	
V <sub>OUT</sub> Output Voltage		MAX690_C/E, MAX704_C/E, MAX80_C/E, I <sub>OUT</sub> = 5mA (Note 4)	V <sub>CC</sub> - 0.03	V <sub>CC</sub> - 0.015		V
		MAX690_C/E, MAX704_C/E, MAX80_C/E, I <sub>OUT</sub> = 50mA	V <sub>CC</sub> - 0.3	V <sub>CC</sub> - 0.15		
		MAX690_M, MAX704_M, MAX80_M, I <sub>OUT</sub> = 5mA (Note 4)	V <sub>CC</sub> - 0.035	V <sub>CC</sub> - 0.015		
		MAX690_M, MAX704_M, MAX80_M, I <sub>OUT</sub> = 50mA	V <sub>CC</sub> - 0.35	V <sub>CC</sub> - 0.15		
		I <sub>OUT</sub> = 250μA, V <sub>CC</sub> > 2.5V (Note 4)	V <sub>CC</sub> - 0.0015	V <sub>CC</sub> - 0.0006		

## 3.0V/3.3V Microprocessor Supervisory Circuits

### ELECTRICAL CHARACTERISTICS (continued)

( $V_{CC}$  = 3.17V to 5.5V for the MAX690T/MAX704T/MAX80\_T,  $V_{CC}$  = 3.02V to 5.5V for the MAX690S/MAX704S/MAX80\_S,  $V_{CC}$  = 2.72V to 5.5V for the MAX690R/MAX704R/MAX80\_R;  $V_{BATT}$  = 3.6V;  $T_A$  =  $T_{MIN}$  to  $T_{MAX}$ ; unless otherwise noted. Typical values are at  $T_A$  = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
V <sub>OUT</sub> in Battery-Backup Mode		I <sub>OUT</sub> = 250μA, V <sub>BATT</sub> = 2.3V		VBATT - 0.1	VBATT - 0.034		V
		I <sub>OUT</sub> = 1mA, V <sub>BATT</sub> = 2.3V			VBATT - 0.14		
Battery Switch Threshold, V <sub>CC</sub> Falling		VBATT - V <sub>CC</sub> , V <sub>SW</sub> > V <sub>CC</sub> > 1.75V (Note 5)		65	25		mV
	V <sub>SW</sub>	VBATT > V <sub>CC</sub> (Note 6)		2.30	2.40	2.50	V
Battery Switch Threshold, V <sub>CC</sub> Rising (Note 7)		This value is identical to the reset threshold, V <sub>CC</sub> rising					V
Reset Threshold (Note 8)	V <sub>RST</sub>	MAX690T/704T/805T	V <sub>CC</sub> falling	3.00	3.075	3.15	V
			V <sub>CC</sub> rising	3.00	3.085	3.17	
		MAX802T/804T/806T	V <sub>CC</sub> falling	3.00	3.075	3.12	
			V <sub>CC</sub> rising	3.00	3.085	3.14	
		MAX690S/704S/805S	V <sub>CC</sub> falling	2.85	2.925	3.00	
			V <sub>CC</sub> rising	2.85	2.935	3.02	
		MAX802S/804S/806S	V <sub>CC</sub> falling	2.88	2.925	3.00	
			V <sub>CC</sub> rising	2.88	2.935	3.02	
		MAX690R/704R/805R	V <sub>CC</sub> falling	2.55	2.625	2.70	
			V <sub>CC</sub> rising	2.55	2.635	2.72	
		MAX802R/804R/806S	V <sub>CC</sub> falling	2.59	2.625	2.70	
			V <sub>CC</sub> rising	2.59	2.635	2.72	
Reset Timeout Period	t <sub>WP</sub>	V <sub>CC</sub> < 3.6V		140	200	280	ms
P <sub>F0</sub> , R <sub>ESET</sub> Output Voltage	V <sub>OH</sub>	I <sub>SOURCE</sub> = 50μA		V <sub>CC</sub> - 0.3	V <sub>CC</sub> - 0.05		V
P <sub>F0</sub> , R <sub>ESET</sub> Output Short to GND Current (Note 4)	I <sub>OS</sub>	V <sub>CC</sub> = 3.3V, V <sub>OH</sub> = 0V			180	500	μV
P <sub>F0</sub> , R <sub>ESET</sub> , R <sub>ESET</sub> Output Voltage	V <sub>OL</sub>	I <sub>SINK</sub> = 1.2mA; MAX690_/704_/802_/806_, V <sub>CC</sub> = V <sub>RST</sub> min; MAX804_/805_, V <sub>CC</sub> = V <sub>RST</sub> max			0.06	0.3	V
P <sub>F0</sub> , R <sub>ESET</sub> Output Voltage	V <sub>OL</sub>	VBATT = 0V, V <sub>CC</sub> = 1.0V, I <sub>SINK</sub> = 40μA, MAX690_C, MAX704_C, MAX80__C			0.13	0.3	V
		VBATT = 0V, V <sub>CC</sub> = 1.2V, I <sub>SINK</sub> = 200μA, MAX690_E/M, MAX704_E/M, MAX80__E/M			0.17	0.3	
RESET Output Leakage Current (Note 9)		VBATT = 0V, V <sub>CC</sub> = V <sub>RST</sub> min; V <sub>RESET</sub> = 0V, V <sub>CC</sub>	MAX804_C, MAX805_C	-1		1	μA
			MAX804_E/M, MAX805_E/M	-10		10	

MAX690T/S/R, 704T/S/R, 802T/S/R, 804-806T/S/R

## 3.0V/3.3V Microprocessor Supervisory Circuits

### ELECTRICAL CHARACTERISTICS (continued)

( $V_{CC}$  = 3.17V to 5.5V for the MAX690T/MAX704T/MAX80\_T,  $V_{CC}$  = 3.02V to 5.5V for the MAX690S/MAX704S/MAX80\_S,  $V_{CC}$  = 2.72V to 5.5V for the MAX690R/MAX704R/MAX80\_R;  $V_{BATT}$  = 3.6V;  $T_A$  =  $T_{MIN}$  to  $T_{MAX}$ ; unless otherwise noted. Typical values are at  $T_A$  = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PFI Input Threshold	VPFT	VCC < 3.6V VPFI falling	MAX802_C/E, MAX804_C/E, MAX806_C/E	1.212	1.237	1.262	V
			MAX690_/MAX704_/MAX805_	1.187	1.237	1.287	
PFI Input Current		MAX690_C/E, MAX704_C/E, MAX80_ _C/E		-25	2	25	nA
		MAX690_M, MAX704_M, MAX80_ _M		-500	2	500	
PFI Hysteresis, PFI Rising	VPFH	VCC < 3.6V	MAX690_C/E, MAX704_C/E, MAX80_ _C/E		10	20	mV
			MAX690_M, MAX704_M, MAX80_ _M		10	25	
PFI Input Current		MAX690_C/E, MAX704_C/E, MAX80_ _C/E		-25	2	25	nA
		MAX690_M, MAX704_M, MAX80_ _M		-500	2	500	
MR Input Threshold	VIH	MAX704_/MAX806_ only			0.7 x VCC		V
	VIL				0.3 x VCC		
MR Pulse Width	tMR	MAX704_/MAX806_ only		100	20		ns
MR to Reset Delay	tMD	MAX704_/MAX806_ only			60	500	ns
MR Pull-Up Current		MAX704_/MAX806_ only, MR = 0V, VCC = 3V		20	60	350	μA
WDI Input Threshold	VIH	MAX690_/MAX802_/MAX804_/MAX805_ only			0.7 x VCC		V
	VIL				0.3 x VCC		
WDI Input Current		0V< VCC < 5.5V	MAX690_C/E, MAX802_C/E, MAX804_C/E, MAX805_C/E	-1	0.01	1	μA
			MAX690_M, MAX802_M, MAX804_M, MAX805_M	-10	0.01	10	
Watchdog Timeout Period	tWD	VCC < 3.6V	MAX690/MAX802/MAX804/ MAX805 only	1.12	1.60	2.24	sec
WDI Pulse Width		MAX690_/MAX802_/MAX804_/MAX805_ only			100	20	ns

**Note 1:**  $V_{CC}$  supply current, logic input leakage, watchdog functionality (MAX690\_/802\_/805\_/804\_),  $\overline{MR}$  functionality (MAX704\_/806\_), PFI functionality, state of  $\overline{RESET}$  (MAX690\_/704\_/802\_/806\_), and RESET (MAX804\_/805\_) tested at  $V_{BATT}$  = 3.6V, and  $V_{CC}$  = 5.5V. The state of  $\overline{RESET}$  or RESET and  $PFI$  is tested at  $V_{CC}$  =  $V_{CC}$  min.

**Note 2:** Tested at  $V_{BATT}$  = 3.6V,  $V_{CC}$  = 3.5V and 0V. The battery current will rise to 10 $\mu A$  over a narrow transition window around  $V_{CC}$  = 1.9V.

**Note 3:** Leakage current into the battery is tested under the worst-case conditions at  $V_{CC}$  = 5.5V,  $V_{BATT}$  = 1.8V and at  $V_{CC}$  = 1.5V,  $V_{BATT}$  = 1.0V.

**Note 4:** Guaranteed by design.

**Note 5:** When  $V_{SW} > V_{CC} > V_{BATT}$ ,  $V_{OUT}$  remains connected to  $V_{CC}$  until  $V_{CC}$  drops below  $V_{BATT}$ . The  $V_{CC}$ -to- $V_{BATT}$  comparator has a small 25mV typical hysteresis to prevent oscillation. For  $V_{CC} < 1.75V$  (typ),  $V_{OUT}$  switches to  $V_{BATT}$  regardless of the voltage on  $V_{BATT}$ .

**Note 6:** When  $V_{BATT} > V_{CC} > V_{SW}$ ,  $V_{OUT}$  remains connected to  $V_{CC}$  until  $V_{CC}$  drops below the battery switch threshold ( $V_{SW}$ ).

**Note 7:**  $V_{OUT}$  switches from  $V_{BATT}$  to  $V_{CC}$  when  $V_{CC}$  rises above the reset threshold, independent of  $V_{BATT}$ . Switchover back to  $V_{CC}$  occurs at the exact voltage that causes  $\overline{RESET}$  to go high (on the MAX804\_/805\_,  $\overline{RESET}$  goes low); however switchover occurs 200ms prior to reset.

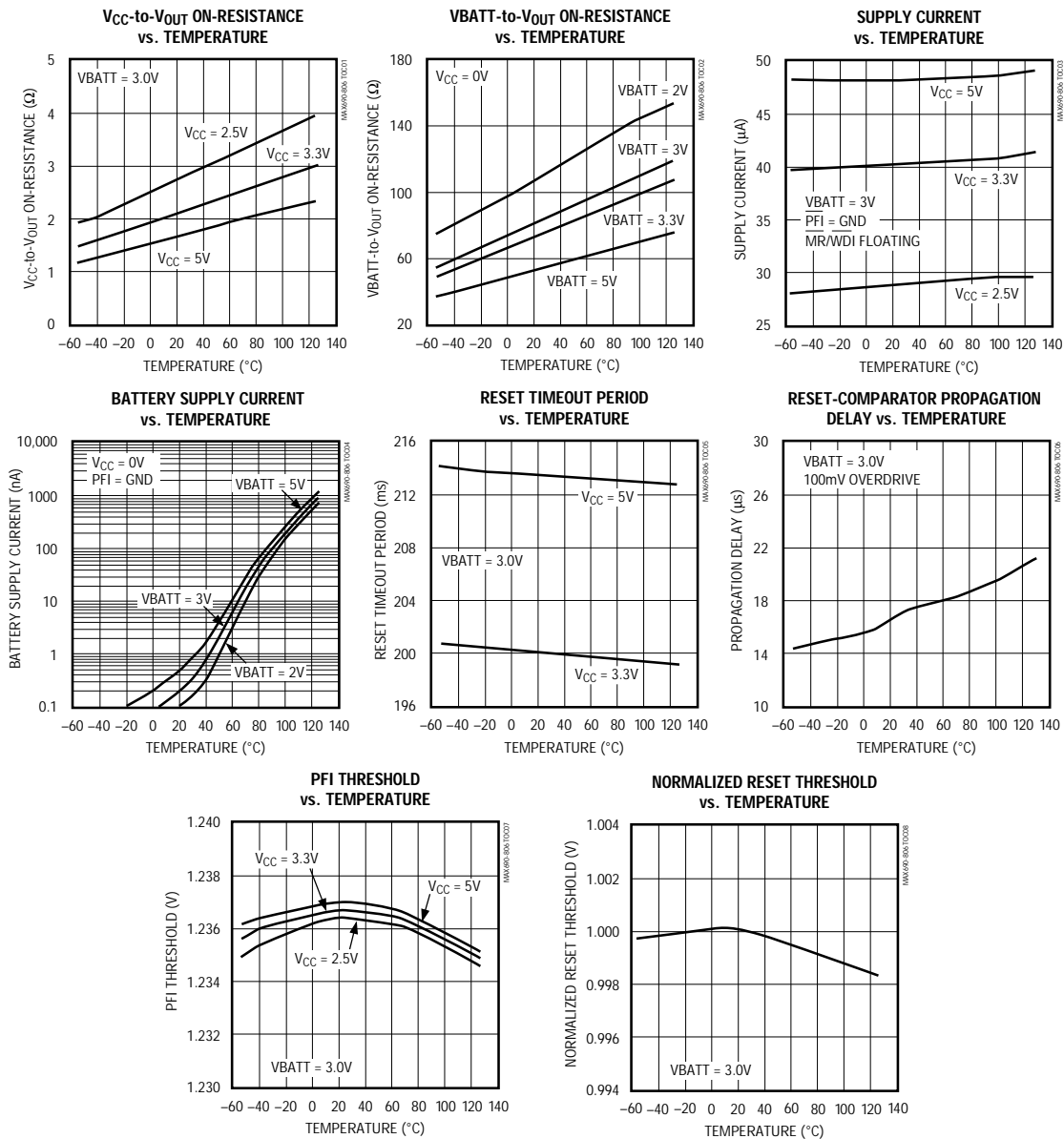
**Note 8:** The reset threshold tolerance is wider for  $V_{CC}$  rising than for  $V_{CC}$  falling to accommodate the 10mV typical hysteresis, which prevents internal oscillation.

**Note 9:** The leakage current into or out of the RESET pin is tested with RESET asserted (RESET output high impedance).

## 3.0V/3.3V Microprocessor Supervisory Circuits

### Typical Operating Characteristics

( $T_A = +25^\circ\text{C}$ , unless otherwise noted.)



MAX690T/S/R, 704T/S/R, 802T/S/R, 804-806T/S/R

## 3.0V/3.3V Microprocessor Supervisory Circuits

### Pin Description

PIN			NAME	FUNCTION
MAX690 MAX802	MAX704 MAX806	MAX804 MAX805		
1	1	1	V <sub>OUT</sub>	Supply Output for CMOS RAM. When V <sub>CC</sub> is above the reset threshold, V <sub>OUT</sub> is connected to V <sub>CC</sub> through a P-channel MOSFET switch. When V <sub>CC</sub> falls below V <sub>SW</sub> and VBATT, VBATT connects to V <sub>OUT</sub> . Connect to V <sub>CC</sub> if no battery is used.
2	2	2	V <sub>CC</sub>	Main Supply Input
3	3	3	GND	Ground
4	4	4	PFI	Power-Fail Input. When PFI is less than V <sub>PFT</sub> or when V <sub>CC</sub> falls below V <sub>SW</sub> , PFO goes low; otherwise, PFO remains high. Connect to ground if unused.
5	5	5	PFO	Power-Fail Output. When PFI is less than V <sub>PFT</sub> , or V <sub>CC</sub> falls below V <sub>SW</sub> , PFO goes low; otherwise, PFO remains high. Leave open if unused.
6	—	6	WDI	Watchdog Input. If WDI remains high or low for 1.6sec, the internal watchdog timer runs out and reset is triggered. The internal watchdog timer clears while reset is asserted or when WDI sees a rising or falling edge. The watchdog function cannot be disabled.
—	6	—	MR	Manual Reset Input. A logic low on MR asserts reset. Reset remains asserted as long as MR is low and for 200ms after MR returns high. This active-low input has an internal 70µA pull-up current. It can be driven from a TTL or CMOS logic line, or shorted to ground with a switch. Leave open if unused.
7	7	—	RESET	Active-Low Reset Output. Pulses low for 200ms when triggered, and stays low whenever V <sub>CC</sub> is below the reset threshold or when MR is a logic low. It remains low for 200ms after either V <sub>CC</sub> rises above the reset threshold, the watchdog triggers a reset, or MR goes from low to high.
—	—	7	RESET	Active-High, Open-Drain Reset Output is the inverse of RESET.
8	8	8	VBATT	Backup-Battery Input. When V <sub>CC</sub> falls below V <sub>SW</sub> and VBATT, V <sub>OUT</sub> switches from V <sub>CC</sub> to VBATT. When V <sub>CC</sub> rises above the reset threshold, V <sub>OUT</sub> reconnects to V <sub>CC</sub> . VBATT may exceed V <sub>CC</sub> . Connect to V <sub>CC</sub> if no battery is used.

### Detailed Description

#### Reset Output

A microprocessor's (µP's) reset input starts the µP in a known state. These µP supervisory circuits assert reset to prevent code execution errors during power-up, power-down, brownout conditions, or a watchdog timeout.

RESET is guaranteed to be a logic low for  $0V < V_{CC} < V_{RST}$ , provided that VBATT is greater than 1V. Without a backup battery, RESET is guaranteed valid for  $V_{CC} > 1V$ . Once V<sub>CC</sub> exceeds the reset threshold, an internal timer keeps RESET low for the reset timeout period; after this interval, RESET goes high (Figure 2).

If a brownout condition occurs (V<sub>CC</sub> dips below the reset threshold), RESET goes low. Each time RESET is asserted, it stays low for the reset timeout period. Any time V<sub>CC</sub> goes below the reset threshold, the internal timer restarts.

The watchdog timer can also initiate a reset. See the *Watchdog Input* section.

The MAX804/MAX805 active-high RESET output is open drain, and the inverse of the MAX690/MAX704/MAX802/MAX806 RESET output.

#### Reset Threshold

The MAX690T/MAX704T/MAX805T are intended for 3.3V systems with a ±5% power-supply tolerance and a 10% system tolerance. Except for watchdog faults, reset will not assert as long as the power supply remains above 3.15V (3.3V - 5%). Reset is guaranteed to assert before the power supply falls below 3.0V.

The MAX690S/MAX704S/MAX805S are designed for 3.3V ±10% power supplies. Except for watchdog faults, they are guaranteed not to assert reset as long as the supply remains above 3.0V (3.3V - 10%). Reset is guaranteed to assert before the power supply falls below 2.85V (V<sub>CC</sub> - 14%).

The MAX690R/MAX704R/MAX805R are optimized for monitoring 3.0V ±10% power supplies. Reset will not occur until V<sub>CC</sub> falls below 2.7V (3.0V - 10%), but is guaranteed to occur before the supply falls below 2.59V (3.0V - 14%).

The MAX802R/S/T, MAX804R/S/T, and MAX806R/S/T are respectively similar to the MAX690R/S/T, MAX805R/S/T, and MAX704R/S/T, but with tightened reset and power-fail threshold tolerances.

## 3.0V/3.3V Microprocessor Supervisory Circuits

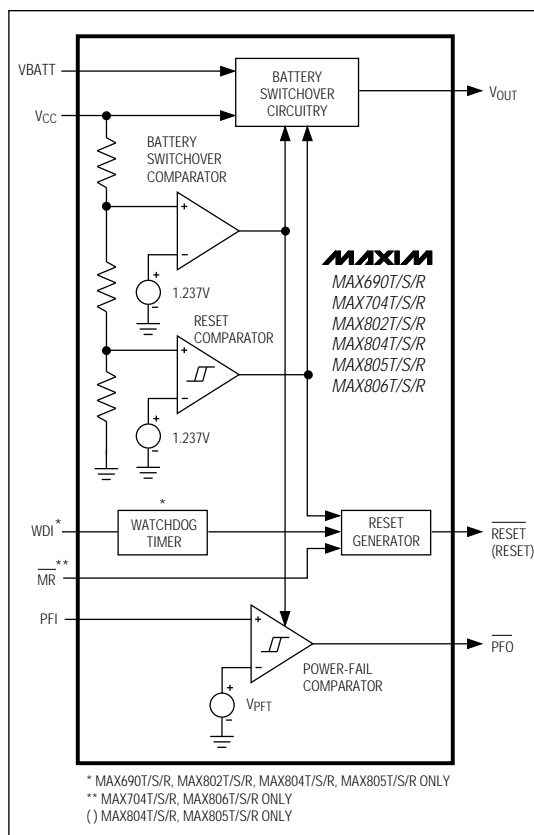


Figure 1. Block Diagram

### Watchdog Input (MAX690\_/802\_/804\_/805\_)

The watchdog circuit monitors the  $\mu P$ 's activity. If the  $\mu P$  does not toggle the watchdog input (WDI) within 1.6sec, a reset pulse is triggered. The internal 1.6sec timer is cleared by either a reset pulse or by a transition (low-to-high or high-to-low) at WDI. If WDI is tied high or low, a  $\overline{\text{RESET}}$  pulse is triggered every 1.8sec ( $t_{WD}$  plus  $t_{RS}$ ).

As long as reset is asserted, the timer remains cleared and does not count. As soon as reset is deasserted, the timer starts counting. Unlike the 5V MAX690 family, the watchdog function **cannot** be disabled.

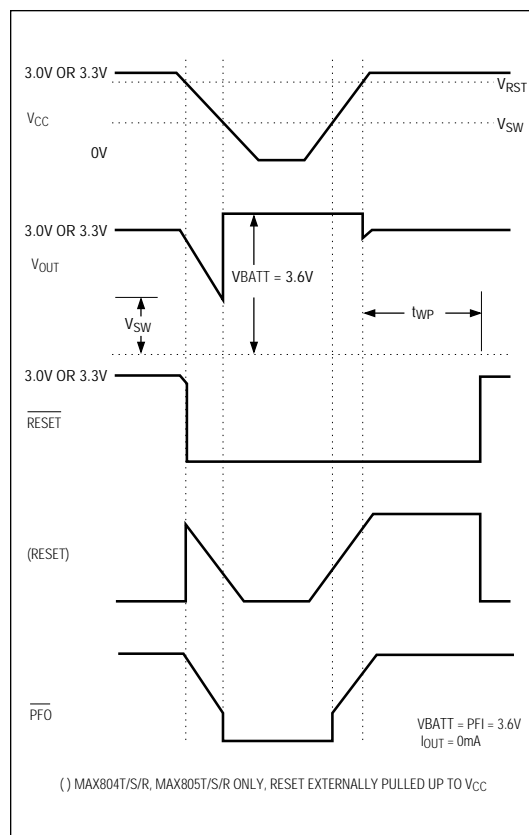


Figure 2. Timing Diagram

### Power-Fail Comparator

The PFI input is compared to an internal reference. If PFI is less than  $V_{PFT}$ ,  $\overline{\text{PFO}}$  goes low. The power-fail comparator is intended for use as an undervoltage detector to signal a failing power supply. However, the comparator does not need to be dedicated to this function because it is completely separate from the rest of the circuitry.

The power-fail comparator turns off and  $\overline{\text{PFO}}$  goes low when  $V_{CC}$  falls below  $V_{SW}$  on power-down. The power-fail comparator turns on as  $V_{CC}$  crosses  $V_{SW}$  on power-up. If the comparator is not used, connect PFI to ground and leave  $\overline{\text{PFO}}$  unconnected.  $\overline{\text{PFO}}$  may be connected to MR on the MAX704\_/MAX806\_ so that a low voltage on PFI will generate a reset (Figure 5b).

MAX690T/S/R, 704T/S/R, 802T/S/R, 804-806T/S/R

## 3.0V/3.3V Microprocessor Supervisory Circuits

### Backup-Battery Switchover

In the event of a brownout or power failure, it may be necessary to preserve the contents of RAM. With a backup battery installed at VBATT, the devices automatically switch RAM to backup power when  $V_{CC}$  falls.

This family of  $\mu P$  supervisors (designed for 3.3V and 3V systems) doesn't always connect VBATT to  $V_{OUT}$  when VBATT is greater than  $V_{CC}$ . VBATT connects to  $V_{OUT}$  (through a  $140\Omega$  switch) when  $V_{CC}$  is below  $V_{SW}$  and VBATT is greater than  $V_{CC}$ , or when  $V_{CC}$  falls below 1.75V (typ) regardless of the VBATT voltage. This is done to allow the backup battery (e.g., a 3.6V lithium cell) to have a higher voltage than  $V_{CC}$ .

Switchover at  $V_{SW}$  (2.40V) ensures that battery-backup mode is entered before  $V_{OUT}$  gets too close to the 2.0V minimum required to reliably retain data in CMOS RAM. Switchover at higher  $V_{CC}$  voltages would decrease backup-battery life. When  $V_{CC}$  recovers, switchover is deferred until  $V_{CC}$  rises above the reset threshold ( $V_{RST}$ ) to ensure a stable supply.  $V_{OUT}$  is connected to  $V_{CC}$  through a  $3\Omega$  PMOS power switch.

### Manual Reset

A logic low on  $\overline{MR}$  asserts reset. Reset remains asserted while  $\overline{MR}$  is low, and for  $t_{WP}$  (200ms) after  $\overline{MR}$  returns high. This input has an internal  $70\mu A$  pull-up current, so it can be left open if it is not used.  $\overline{MR}$  can be driven with TTL or CMOS logic levels, or with open-drain/collector outputs. Connect a normally open momentary switch from  $\overline{MR}$  to GND to create a manual-reset function; external debounce circuitry is not required.

**Table 1. Input and Output Status in Battery-Backup Mode**

PIN NAME	STATUS
$V_{OUT}$	Connected to VBATT through an internal $140\Omega$ switch
$V_{CC}$	Disconnected from $V_{OUT}$
PFI	The power-fail comparator is disabled when $V_{CC} < V_{SW}$
$\overline{PFO}$	Logic low when $V_{CC} < V_{SW}$ or $PFI < V_{PFT}$
WDI	The watchdog timer is disabled
$\overline{MR}$	Disabled
$\overline{RESET}$	Low logic
RESET	High impedance
VBATT	Connected to $V_{OUT}$

### Applications Information

These  $\mu P$  supervisory circuits are not short-circuit protected. Shorting  $V_{OUT}$  to ground—excluding power-up transients such as charging a decoupling capacitor—destroys the device. Decouple both  $V_{CC}$  and VBATT pins to ground by placing  $0.1\mu F$  capacitors as close to the device as possible.

#### Using a SuperCap as a Backup Power Source

SuperCaps™ are capacitors with extremely high capacitance values (e.g., order of 0.47F) for their size. Figure 3 shows two ways to use a SuperCap as a backup power source. The SuperCap may be connected through a diode to the 3V input (Figure 3a) or, if a 5V supply is also available, the SuperCap may be charged up to the 5V supply (Figure 3b) allowing a longer backup period. Since VBATT can exceed  $V_{CC}$  while  $V_{CC}$  is above the reset threshold, there are no special precautions when using these  $\mu P$  supervisors with a SuperCap.

#### Operation without a Backup Power Source

These  $\mu P$  supervisors were designed for battery-backed applications. If a backup battery is not used, connect both VBATT and  $V_{OUT}$  to  $V_{CC}$ , or use a different  $\mu P$  supervisor such as the MAX706T/S/R or MAX708T/S/R.

#### Replacing the Backup Battery

The backup power source can be removed while  $V_{CC}$  remains valid, if VBATT is decoupled with a  $0.1\mu F$  capacitor to ground, without danger of triggering RESET/ $\overline{RESET}$ . As long as  $V_{CC}$  stays above  $V_{SW}$ , battery-backup mode cannot be entered.

#### Adding Hysteresis to the Power-Fail Comparator

The power-fail comparator has a typical input hysteresis of 10mV. This is sufficient for most applications where a power-supply line is being monitored through an external voltage divider (see the section *Monitoring an Additional Power Supply*).

If additional noise margin is desired, connect a resistor between  $\overline{PFO}$  and PFI as shown in Figure 4a. Select the ratio of R1 and R2 such that PFI sees  $1.237V$  ( $V_{PFT}$ ) when  $V_{IN}$  falls to its trip point ( $V_{TRIP}$ ). R3 adds the hysteresis and will typically be more than 10 times the value of R1 or R2. The hysteresis window extends both above ( $V_H$ ) and below ( $V_L$ ) the original trip point ( $V_{TRIP}$ ).

™ SuperCap is a trademark of Baknor Industries.

## 3.0V/3.3V Microprocessor Supervisory Circuits

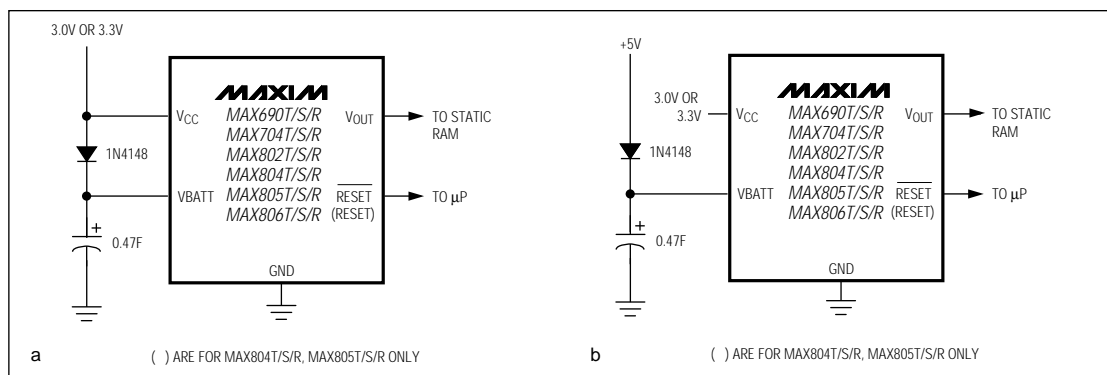


Figure 3. Using a SuperCap as a Backup Power Source

Connecting an ordinary signal diode in series with R3, as shown in Figure 4b, causes the lower trip point ( $V_L$ ) to coincide with the trip point without hysteresis ( $V_{TRIP}$ ), so the entire hysteresis window occurs above  $V_{TRIP}$ . This method provides additional noise margin without compromising the accuracy of the power-fail threshold when the monitored voltage is falling. It is useful for accurately detecting when a voltage falls past a threshold.

The current through R1 and R2 should be at least 1 $\mu$ A to ensure that the 25nA (max over extended temperature range) PFI input current does not shift the trip point. R3 should be larger than 10k $\Omega$  so it does not load down the  $\overline{PFO}$  pin. Capacitor C1 adds additional noise rejection.

### Monitoring an Additional Power Supply

These  $\mu$ P supervisors can monitor either positive or negative supplies using a resistor voltage divider to PFI.  $\overline{PFO}$  can be used to generate an interrupt to the  $\mu$ P (Figure 5). Connecting  $\overline{PFO}$  to MR on the MAX704 and MAX806 causes reset to assert when the monitored supply goes out of tolerance. Reset remains asserted as long as  $\overline{PFO}$  holds MR low, and for 200ms after  $\overline{PFO}$  goes high.

### Interfacing to $\mu$ Ps with Bidirectional Reset Pins

$\mu$ Ps with bidirectional reset pins, such as the Motorola 68HC11 series, can contend with the MAX690/\_/MAX704/\_/MAX802/\_/MAX806\_  $\overline{RESET}$  output. If, for

example, the  $\overline{RESET}$  output is driven high and the  $\mu$ P wants to pull it low, indeterminate logic levels may result. To correct this, connect a 4.7k $\Omega$  resistor between the  $\overline{RESET}$  output and the  $\mu$ P reset I/O, as in Figure 6. Buffer the  $\overline{RESET}$  output to other system components.

### Negative-Going $V_{CC}$ Transients

While issuing resets to the  $\mu$ P during power-up, power-down, and brownout conditions, these supervisors are relatively immune to short-duration negative-going  $V_{CC}$  transients (glitches). It is usually undesirable to reset the  $\mu$ P when  $V_{CC}$  experiences only small glitches.

Figure 7 shows maximum transient duration vs. reset-comparator overdrive, for which reset pulses are **not** generated. The graph was produced using negative-going  $V_{CC}$  pulses, starting at 3.3V and ending below the reset threshold by the magnitude indicated (reset comparator overdrive). The graph shows the maximum pulse width a negative-going  $V_{CC}$  transient may typically have without causing a reset pulse to be issued. As the amplitude of the transient increases (i.e., goes farther below the reset threshold), the maximum allowable pulse width decreases. Typically, a  $V_{CC}$  transient that goes 100mV below the reset threshold and lasts for 40 $\mu$ s or less will not cause a reset pulse to be issued.

A 100nF bypass capacitor mounted close to the  $V_{CC}$  pin provides additional transient immunity.

MAX690T/S/R, 704T/S/R, 802T/S/R, 804-806T/S/R

## 3.0V/3.3V Microprocessor Supervisory Circuits

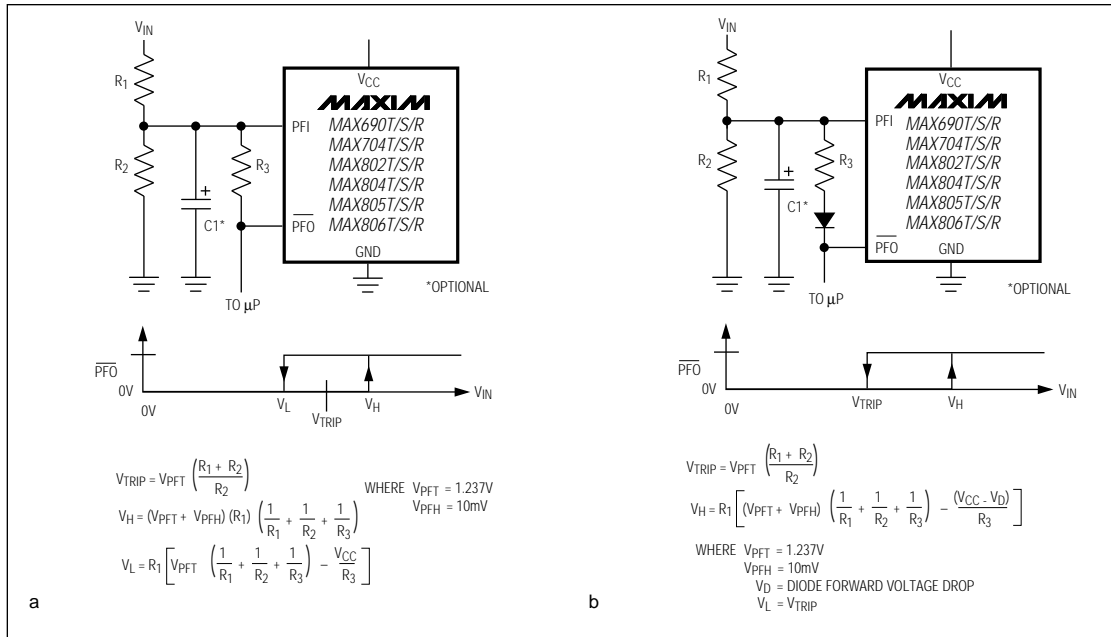


Figure 4. a) Adding Additional Hysteresis to the Power-Fail Comparator b) Shifting the Additional Hysteresis above  $V_{PFT}$

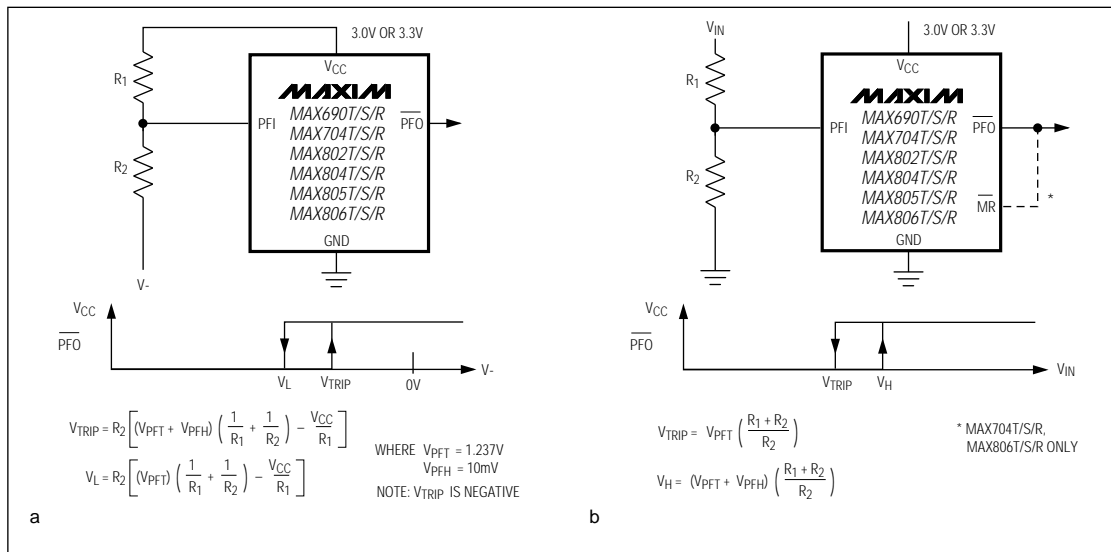


Figure 5. Using the Power-Fail Comparator to Monitor an Additional Power Supply

## 3.0V/3.3V Microprocessor Supervisory Circuits

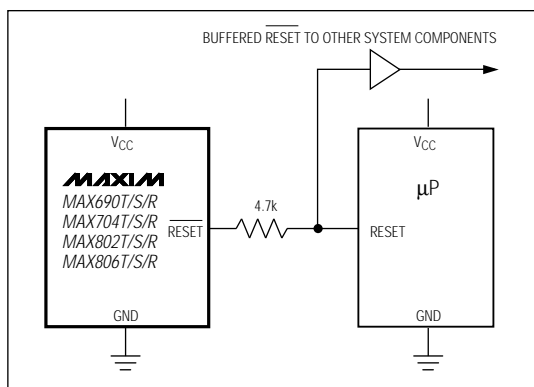


Figure 6. Interfacing to  $\mu$ Ps with Bidirectional Reset I/O

### \_Typical Operating Circuits (cont.)

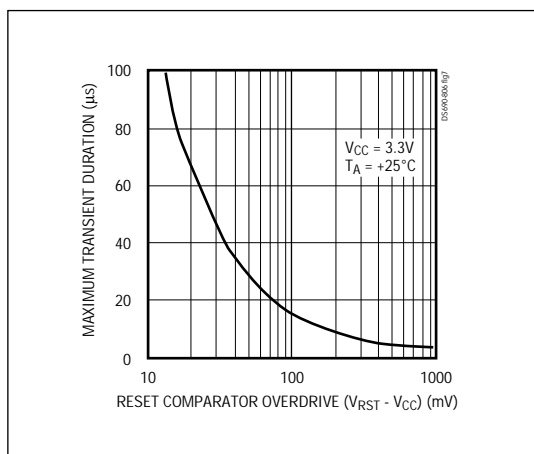
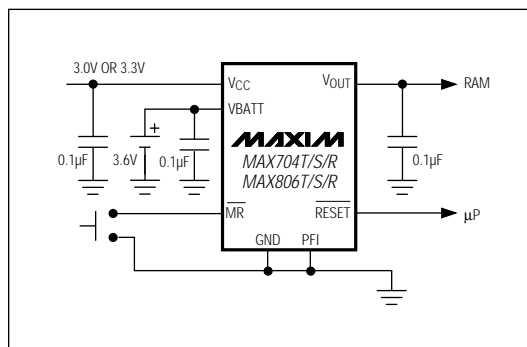


Figure 7. Maximum Transient Duration without Causing a Reset Pulse vs. Reset Comparator Overdrive

MAX690T/S/R, 704T/S/R, 802T/S/R, 804-806T/S/R

## 3.0V/3.3V Microprocessor Supervisory Circuits

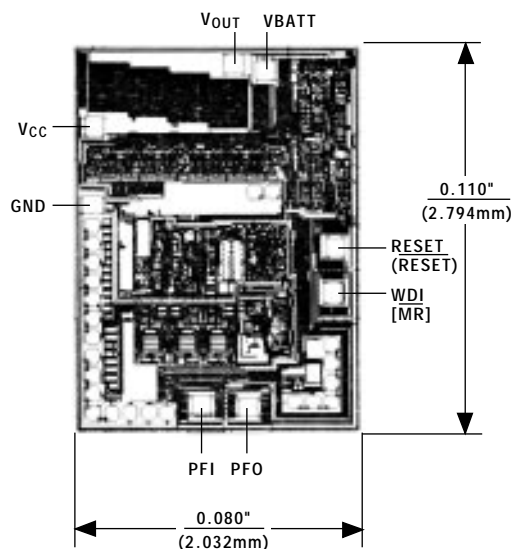
### Ordering Information (continued)

PART**	TEMP. RANGE	PIN-PACKAGE
<b>MAX704_CPA</b>	0°C to +70°C	8 Plastic DIP
MAX704_CSA	0°C to +70°C	8 SO
MAX704_C/D	0°C to +70°C	Dice*
MAX704_EPA	-40°C to +85°C	8 Plastic DIP
MAX704_ESA	-40°C to +85°C	8 SO
MAX704_MJA	-55°C to +125°C	8 Cerdip
<b>MAX802_CPA</b>	0°C to +70°C	8 Plastic DIP
MAX802_CSA	0°C to +70°C	8 SO
MAX802_C/D	0°C to +70°C	Dice*
MAX802_EPA	-40°C to +85°C	8 Plastic DIP
MAX802_ESA	-40°C to +85°C	8 SO
MAX802_MJA	-55°C to +125°C	8 Cerdip
<b>MAX804_CPA</b>	0°C to +70°C	8 Plastic DIP
MAX804_CSA	0°C to +70°C	8 SO
MAX804_C/D	0°C to +70°C	Dice*
MAX804_EPA	-40°C to +85°C	8 Plastic DIP
MAX804_ESA	-40°C to +85°C	8 SO
MAX804_MJA	-55°C to +125°C	8 Cerdip
<b>MAX805_CPA</b>	0°C to +70°C	8 Plastic DIP
MAX805_CSA	0°C to +70°C	8 SO
MAX805_C/D	0°C to +70°C	Dice*
MAX805_EPA	-40°C to +85°C	8 Plastic DIP
MAX805_ESA	-40°C to +85°C	8 SO
MAX805_MJA	-55°C to +125°C	8 Cerdip
<b>MAX806_CPA</b>	0°C to +70°C	8 Plastic DIP
MAX806_CSA	0°C to +70°C	8 SO
MAX806_C/D	0°C to +70°C	Dice*
MAX806_EPA	-40°C to +85°C	8 Plastic DIP
MAX806_ESA	-40°C to +85°C	8 SO
MAX806_MJA	-55°C to +125°C	8 Cerdip

\* Contact factory for dice specifications.

\*\* These parts offer a choice of reset threshold voltage. Select the letter corresponding to the desired nominal reset threshold voltage (T = 3.075V, S = 2.925V, R = 2.625V) and insert it into the blank to complete the part number.

### Chip Topography



( ) ARE FOR MAX804T/S/R, MAX805T/S/R.

[ ] ARE FOR MAX704T/S/R, MAX806T/S/R.

TRANSISTOR COUNT: 802;

SUBSTRATE IS CONNECTED TO THE HIGHER OF  $V_{CC}$  OR  $V_{BATT}$ , AND MUST BE FLOATED IN ANY HYBRID DESIGN.

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