

SN54LS114A, SN54S114, SN74LS114A, SN74S114A DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET, COMMON CLEAR, AND COMMON CLOCK

SDLS010 – MARCH 1973 – REVISED MARCH 1988

- Fully Buffered to Offer Maximum Isolation from External Disturbance
- Package Options Include Ceramic Carriers and Flat Packages in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the preset and clear inputs sets or resets the outputs regardless of the levels of the other inputs. When preset and clear are inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

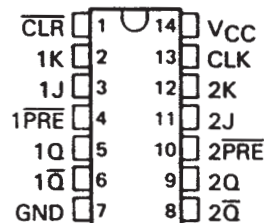
The SN54LS114A and SN54S114 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LS114A and SN74S114A are characterized for operation from 0°C to 70°C .

FUNCTION TABLE

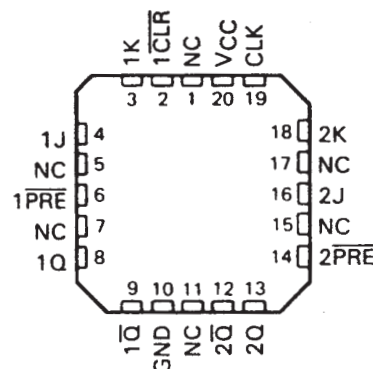
| INPUTS | | | | | OUTPUTS | |
|--------|-----|--------------|---|---|---------------|---------------|
| PRE | CLR | CLK | J | K | Q | \bar{Q} |
| L | H | X | X | X | H | L |
| H | L | X | X | X | L | H |
| L | L | X | X | X | H^{\dagger} | H^{\dagger} |
| H | H | \downarrow | L | L | Q_0 | \bar{Q}_0 |
| H | H | \downarrow | H | L | H | L |
| H | H | \downarrow | L | H | L | H |
| H | H | \downarrow | H | H | TOGGLE | TOGGLE |
| H | H | H | X | X | Q_0 | \bar{Q}_0 |

\dagger The output levels in this configuration are not guaranteed to meet the minimum levels for V_{OH} if the lows at preset and clear are near V_{IL} minimum. Furthermore, this configuration is nonstable; that is, it will not persist when either preset or clear returns to its inactive (high) level.

SN54LS114A, SN54S114 . . . J OR W PACKAGE
SN74LS114A, SN74S114A . . . D OR N PACKAGE
(TOP VIEW)

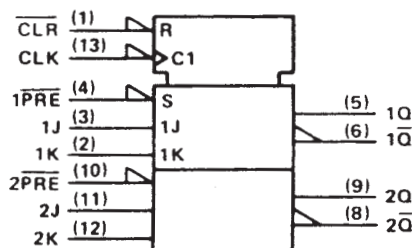


SN54LS114A, SN54S114 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic symbol \dagger



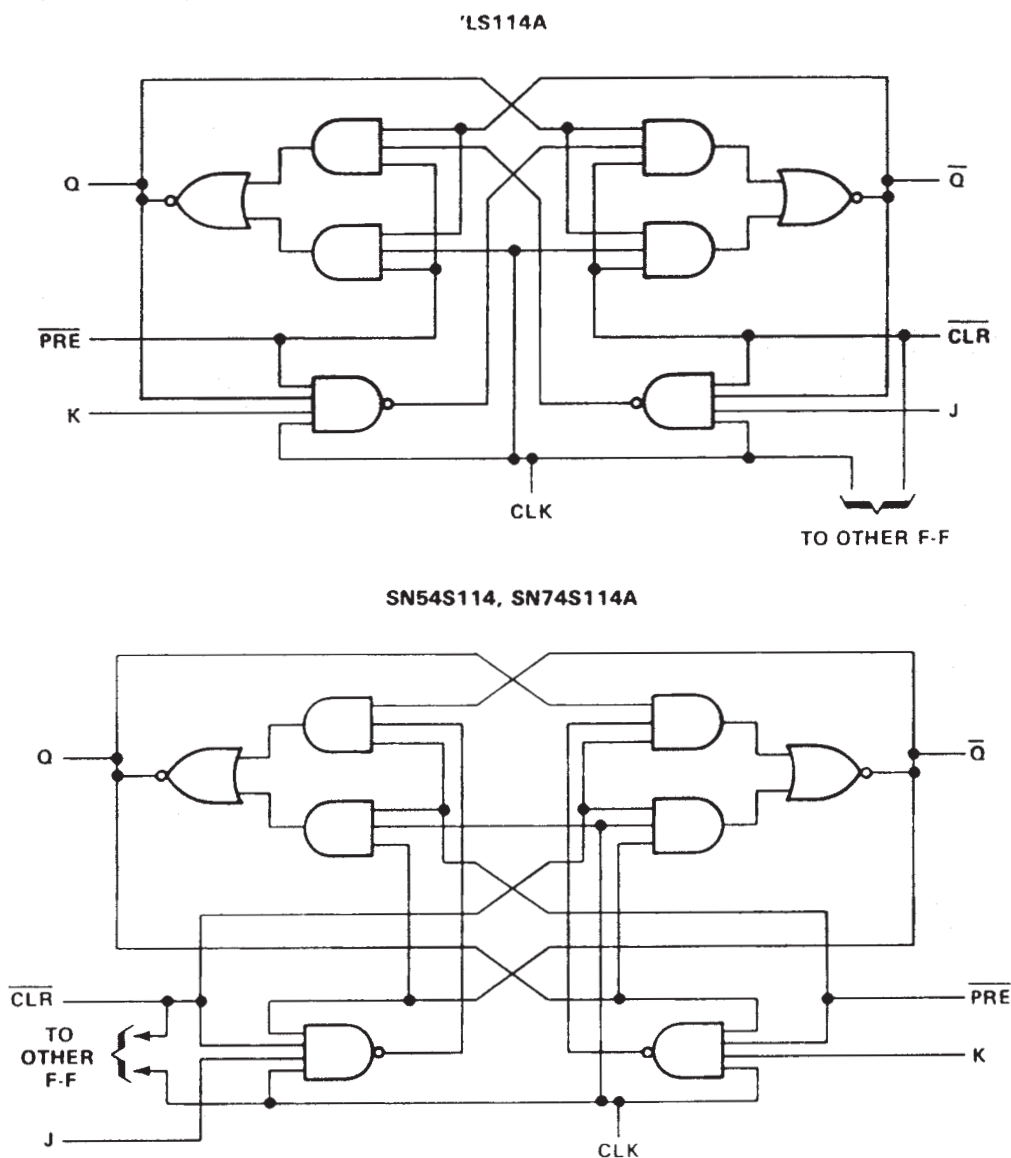
\dagger This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, N, and W packages.

SN54LS114A, SN54S114, SN74LS114A, SN74S114A
DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS
WITH PRESET, COMMON CLEAR, AND COMMON CLOCK

SDLS010 – MARCH 1973 – REVISED MARCH 1988

logic diagram (positive logic)

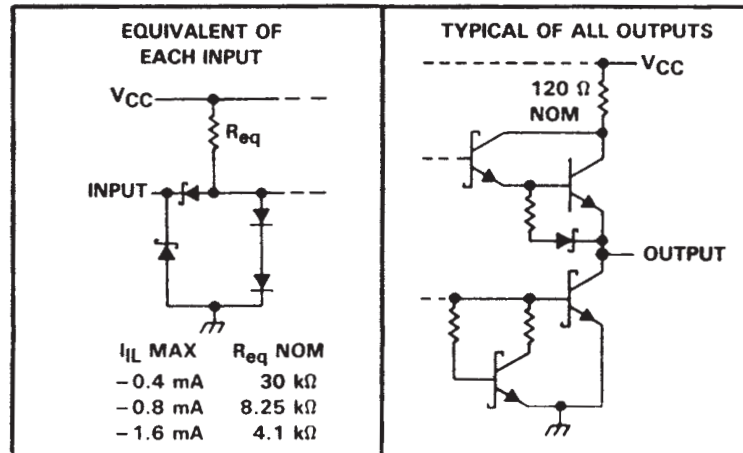


SN54LS114A, SN54S114, SN74LS114A, SN74S114A DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET, COMMON CLEAR, AND COMMON CLOCK

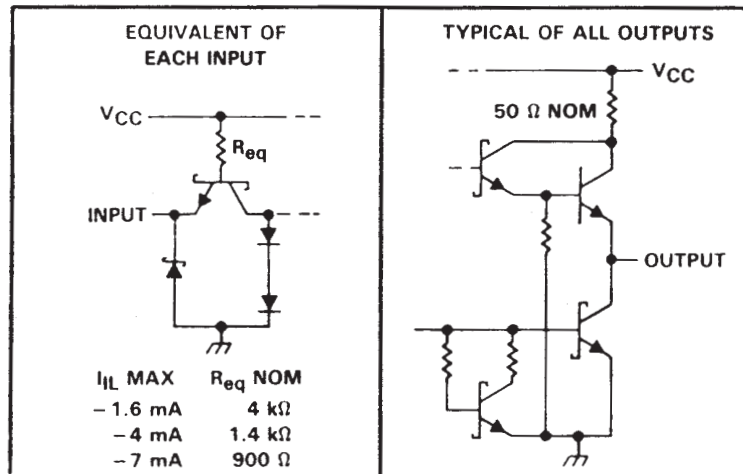
SDLS010 – MARCH 1973 – REVISED MARCH 1988

schematics of inputs and outputs

'LS114A



SN54S114, SN74S114A



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| | |
|---|----------------|
| Supply voltage, V_{CC} (see Note 1) | 7 V |
| Input voltage: 'LS114A | 7 V |
| SN54S114, SN74S114A | 5.5 V |
| Operating free-air temperature range: SN54' | -55°C to 125°C |
| SN74' | 0°C to 70°C |
| Storage temperature range | -65°C to 150°C |

NOTE 1: Voltage values are with respect to network ground terminal.

SN54LS114A, SN54S114, SN74LS114A, SN74S114A

DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS

WITH PRESET, COMMON CLEAR, AND COMMON CLOCK

SDLS010 – MARCH 1973 – REVISED MARCH 1988

recommended operating conditions

| | | | SN54LS114A | | | SN74LS114A | | | UNIT |
|--------------------|--------------------------------|--|------------|-----|-----|------------|-----|------|------|
| | | | MIN | NOM | MAX | MIN | NOM | MAX | |
| V _{CC} | Supply voltage | | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| V _{IH} | High-level input voltage | | 2 | | | 2 | | | V |
| V _{IL} | Low-level input voltage | | 0.7 | | | 0.8 | | | V |
| I _{OH} | High-level output current | | −0.4 | | | −0.4 | | | mA |
| I _{OL} | Low-level output current | | 4 | | | 8 | | | mA |
| f _{clock} | Clock frequency | | 0 | | | 0 | | | MHz |
| t _w | Pulse duration | CLK | 20 | | | 20 | | | ns |
| | | $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ low | 25 | | | 25 | | | |
| t _{su} | Set up time-before CLK↓ | Data high or low | 20 | | | 20 | | | ns |
| | | $\overline{\text{CLR}}$ inactive | 25 | | | 25 | | | |
| | | $\overline{\text{PRE}}$ inactive | 20 | | | 20 | | | |
| t _h | Hold time-data after CLK↓ | | 0 | | | 0 | | | ns |
| T _A | Operating free-air temperature | | −55 | | | 125 | | | °C |

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS† | | SN54LS114A | | | SN74LS114A | | | UNIT |
|-------------------------|--------|--|--|------------|------|------|------------|------|------|------|
| | | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| V _{IK} | | V _{CC} = MIN, I _I = -18 mA | | | | -1.5 | | | -1.5 | V |
| V _{OH} | | V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX, I _{OH} = -0.4 mA | | 2.5 | 3.4 | | 2.7 | 3.4 | | V |
| V _{OL} | | V _{CC} = MIN, V _{IL} = MAX, V _{IH} = 2 V, I _{OL} = 4 mA | | | 0.25 | 0.4 | | 0.25 | 0.4 | V |
| | | V _{CC} = MIN, V _{IL} = MAX, V _{IH} = 2 V, I _{OL} = 8 mA | | | | | | 0.35 | 0.5 | |
| I _I | J or K | V _{CC} = MAX, V _I = 7 V | | | | 0.1 | | | 0.1 | mA |
| | CLR | | | | | 0.6 | | | 0.6 | |
| | PRE | | | | | 0.3 | | | 0.3 | |
| | CLK | | | | | 0.8 | | | 0.8 | |
| I _{IH} | J or K | V _{CC} = MAX, V _I = 2.7 V | | | | 20 | | | 20 | μA |
| | CLR | | | | | 120 | | | 120 | |
| | PRE | | | | | 60 | | | 60 | |
| | CLK | | | | | 160 | | | 160 | |
| I _{IL} | J or K | V _{CC} = MAX, V _I = 0.4 V | | | | -0.4 | | | -0.4 | mA |
| | CLR | | | | | -1.6 | | | -1.6 | |
| | PRE | | | | | -0.8 | | | -0.8 | |
| | CLK | | | | | -1.6 | | | -1.6 | |
| I _{OS} § | | V _{CC} = MAX, See Note 2 | | -20 | | -100 | -20 | | -100 | mA |
| I _{CC} (Total) | | V _{CC} = MAX, See Note 3 | | | 4 | 6 | | 4 | 6 | mA |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

NOTES: 2. For certain devices where state commutation can be caused by shorting an output to ground, an equivalent test may be performed with V_O = 2.25 V and 2.125 V for the '54 family and the '74 family, respectively, with the minimum and maximum limits reduced to one half of their stated values.

3. With all outputs open, I_{CC} is measured with the Q and Q̄ outputs high in turn. At the time of measurement, the clock input is grounded.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN54LS114A, SN54S114, SN74LS114A, SN74S114A
DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS
WITH PRESET, COMMON CLEAR, AND COMMON CLOCK

SDLS010 – MARCH 1973 – REVISED MARCH 1988

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ (see Note 4)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------|-----------------|----------------|--|-----|-----|-----|------|
| f _{max} | | | R _L = 2 kΩ, C _L = 15 pF | 30 | 45 | | MHz |
| t _{PLH} | CLR, PRE or CLK | Q or Q̄ | | | 15 | 20 | ns |
| t _{PHL} | | | | | 15 | 20 | ns |

NOTE 4: Load circuit and voltage waveforms are shown in Section 1.



SN54LS114A, SN54S114, SN74LS114A, SN74S114A

DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS

WITH PRESET, COMMON CLEAR, AND COMMON CLOCK

SDLS010 – MARCH 1973 – REVISED MARCH 1988

recommended operating conditions

| | | SN54S114 | | | SN74S114A | | | UNIT |
|----------|--------------------------------|------------------|-----|-----|-----------|-----|------|------|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| V_{CC} | Supply voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| V_{IH} | High-level input voltage | 2 | | | 2 | | | V |
| V_{IL} | Low-level input voltage | | | 0.8 | | | 0.8 | V |
| I_{OH} | High-level output current | | | -1 | | | -1 | mA |
| I_{OL} | Low-level output current | | | 20 | | | 20 | mA |
| t_w | Pulse duration | CLK | 6 | | 6 | | | ns |
| | | CLK low | 6.5 | | 6.5 | | | |
| | | PRE or CLR low | 8 | | 8 | | | |
| t_{su} | Setup time | Data high or low | 7 | | 7 | | | ns |
| t_h | Hold time-data after CLK↓ | | 0 | | 0 | | | ns |
| T_A | Operating free-air temperature | -55 | | 125 | 0 | | 70 | °C |

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS† | | SN54S114 | | | SN74S114A | | | UNIT |
|---------------|--------|---|--|----------|------|------|-----------|------|------|---------------|
| | | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| V_{IK} | | $V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$ | | | | -1.2 | | | -1.2 | V |
| V_{OH} | | $V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -1 \text{ mA}$ | | 2.5 | 3.4 | | 2.7 | 3.4 | | V |
| V_{OL} | | $V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 20 \text{ mA}$ | | | | 0.5 | | | 0.5 | V |
| I_I | | $V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$ | | | | 1 | | | 1 | mA |
| I_{IH} | J or K | $V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$ | | | | 50 | | | 50 | μA |
| | CLR | | | | | 200 | | | 200 | |
| | PRE | | | | | 100 | | | 100 | |
| | CLK | | | | | 200 | | | 200 | |
| I_{IL} | J or K | $V_{CC} = \text{MAX}, V_I = 0.5 \text{ V}$ | | | | -1.6 | | | -1.6 | mA |
| | CLR | | | | | -14 | | | -14 | |
| | PRE | | | | | -7 | | | -7 | |
| | CLK | | | | | -8 | | | -8 | |
| I_{OS}^{\S} | | $V_{CC} = \text{MAX}$ | | -40 | | -100 | -40 | | -100 | mA |
| $I_{CC}^{\#}$ | | $V_{CC} = \text{MAX},$ See Note 3 | | | 15 | 25 | | 15 | 25 | mA |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

Values are average per flip-flop.

NOTE 3: With all outputs open, I_{CC} is measured with the Q and \bar{Q} outputs high in turn. At the time of measurement, the clock input is grounded.

SN54LS114A, SN54S114, SN74LS114A, SN74S114A
DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS
WITH PRESET, COMMON CLEAR, AND COMMON CLOCK

SDLS010 – MARCH 1973 – REVISED MARCH 1988

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ (see Note 4)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------|-----------------------|----------------|---|-----|-----|-----|------|
| f _{max} | | | R _L = 280 Ω, C _L = 15 pF | 80 | 125 | | MHz |
| t _{PLH} | PRE or CLR | Q or Q̄ | | | 4 | 7 | ns |
| t _{PHL} | PRE or CLR (CLK high) | Q̄ or Q | | | 5 | 7 | ns |
| | PRE or CLR (CLK low) | | | | 5 | 7 | |
| t _{PLH} | CLK | Q or Q̄ | | | 4 | 7 | ns |
| t _{PHL} | | | | | 5 | 7 | ns |

NOTE 4: Load circuit and voltage waveforms are shown in Section 1.



IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.

Copyright © Each Manufacturing Company.

All Datasheets cannot be modified without permission.

This datasheet has been download from :

www.AllDataSheet.com

100% Free DataSheet Search Site.

Free Download.

No Register.

Fast Search System.

www.AllDataSheet.com