#### CY54FCT240T, CY74FCT240T 8-BIT BUFFERS/LINE DRIVERS WITH 3-STATE OUTPUTS

SCCS017A - MAY 1994 - REVISED OCTOBER 2001

- Function, Pinout, and Drive Compatible With FCT and F Logic
- Reduced V<sub>OH</sub> (Typically = 3.3 V) Versions of Equivalent FCT Functions
- Edge-Rate Control Circuitry for Significantly Improved Noise Characteristics
- I<sub>off</sub> Supports Partial-Power-Down Mode Operation
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)
- Matched Rise and Fall Times
- Fully Compatible With TTL Input and Output Logic Levels
- CY54FCT240T
  - 48-mA Output Sink Current
     12-mA Output Source Current
- CY74FCT240T
  - 64-mA Output Sink Current
     32-mA Output Source Current
- 3-State Outputs

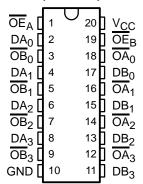
#### description

The 'FCT240T devices are octal buffers and line drivers designed to be employed as memory address drivers, clock drivers, and

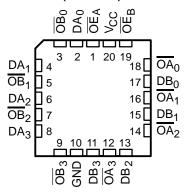
bus-oriented transmitters/receivers. These devices provide speed and drive capabilities equivalent to their fastest bipolar logic counterparts, while reducing power consumption. The input and output voltage levels allow direct interface with TTL, NMOS, and CMOS devices without external components.

These devices are fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.





CY54FCT240T . . . L PACKAGE (TOP VIEW)





Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



#### **ORDERING INFORMATION**

TA	PACKAGE†		SPEED (ns)	ORDERABLE PART NUMBER	TOP-SIDE MARKING	
	SOIC - SO	Tube	4.3	CY74FCT240CTSOC	FCT240C	
	3010 - 30	Tape and reel	4.3	CY74FCT240CTSOCT	FC1240C	
	QSOP - Q	Tape and reel	4.3	CY74FCT240CTQCT	FCT240C	
	SOIC - SO	Tube	4.8	CY74FCT240ATSOC	FCT240A	
–40°C to 85°C	3010 - 30	Tape and reel	4.8	CY74FCT240ATSOCT	FC1240A	
	QSOP - Q	Tape and reel	4.8	CY74FCT240ATQCT	FCT240A	
	SOIC - SO	Tube	8	CY74FCT240TSOC	ECT040	
	3010 - 30	Tape and reel	8	CY74FCT240TSOCT	FCT240	
	QSOP - Q	Tape and reel	8	CY74FCT240TQCT	FCT240	
	CDIP – D	Tube	4.7	CY54FCT240CTDMB		
–55°C to 125°C	CDIP – D	Tube	5.1	CY54FCT240ATDMB		
-55 C to 125 C	LCC – L	Tube	5.1	CY54FCT240ATLMB		
	CDIP – D	Tube	9	CY54FCT240TDMB		

 $<sup>\ ^{\</sup>dagger} \ Package \ drawings, standard \ packing \ quantities, thermal \ data, symbolization, and \ PCB \ design \ guidelines \ are \ available$ at www.ti.com/sc/package.

#### **FUNCTION TABLE**

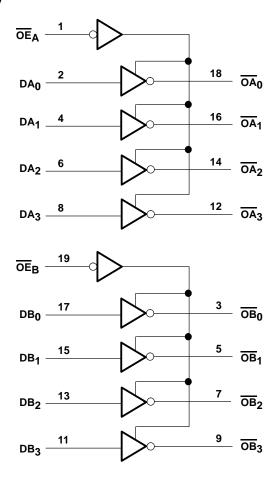
	INPUTS	ОИТРИТ	
ΘE <sub>A</sub>	OE <sub>B</sub>	D	ō
L	L	L	Н
L	L	Н	L
Н	Н	Χ	z

H = High logic level, L = Low logic level, X = Don't care, Z = High-impedance state



SCCS017A - MAY 1994 - REVISED OCTOBER 2001

#### logic diagram (positive logic)



## absolute maximum rating over operating free-air temperature range (unless otherwise noted)†

Supply voltage range to ground potential	0.5 V to 7 V
DC input voltage range	–0.5 V to 7 V
DC output voltage range	–0.5 V to 7 V
DC output current (maximum sink current/pin)	
Package thermal impedance, θ <sub>JA</sub> (see Note 1): Q package	68°C/W
SO package	58°C/W
Ambient temperature range with power applied, TA	
Storage temperature range, T <sub>stq</sub>	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.



# CY54FCT240T, CY74FCT240T 8-BIT BUFFERS/LINE DRIVERS WITH 3-STATE OUTPUTS SCCS017A - MAY 1994 - REVISED OCTOBER 2001

#### recommended operating conditions (see Note 2)

		CY54FCT240T			CY74FCT240T			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
VIH	High-level input voltage	2			2			V
$V_{IL}$	Low-level input voltage		-	8.0			0.8	V
loh	High-level output current			-12			-32	mA
lOL	Low-level output current			48			64	mA
TA	Operating free-air temperature	-55		125	-40		85	°C

NOTE 2: All unused inputs of the device must be held at  $V_{\hbox{CC}}$  or GND to ensure proper device operation.



SCCS017A - MAY 1994 - REVISED OCTOBER 2001

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

242445752		TEST CONDITIONS				ЮT	CY	74FCT24	-OT	LINUT		
PARAMETER		TEST CONDITION	NS	MIN	TYP <sup>†</sup>	MAX	MIN	TYP <sup>†</sup>	MAX	UNIT		
V	$V_{CC} = 4.5 \text{ V},$	$I_{IN} = -18 \text{ mA}$			-0.7	-1.2				V		
VIK	$V_{CC} = 4.75 \text{ V},$	$I_{IN} = -18 \text{ mA}$						-0.7	-1.2	V		
	$V_{CC} = 4.5 \text{ V},$	$I_{OH} = -12 \text{ mA}$		2.4	3.3							
Voн	V <sub>CC</sub> = 4.75 V	$I_{OH} = -32 \text{ mA}$					2			V		
	VCC = 4.75 V	$I_{OH} = -15 \text{ mA}$					2.4	3.3				
VOL	$V_{CC} = 4.5 \text{ V},$	$I_{OL} = 48 \text{ mA}$			0.3	0.55				V		
VOL	$V_{CC} = 4.75 \text{ V},$	$I_{OL} = 64 \text{ mA}$						0.3	0.55	V		
$V_{hys}$	All inputs				0.2			0.2		>		
1.	$V_{CC} = 5.5 \text{ V},$	VIN = VCC				5				μΑ		
-	$V_{CC} = 5.25 \text{ V},$	VIN = VCC							5	μΑ		
1	$V_{CC} = 5.5 \text{ V},$	$V_{1N} = 2.7 \text{ V}$				±1				μΑ		
ЧH	$V_{CC} = 5.25 \text{ V},$	$V_{1N} = 2.7 \text{ V}$							±1	μΑ		
1	$V_{CC} = 5.5 \text{ V},$	$V_{IN} = 0.5 V$				±1				μА		
ļ.	$V_{CC} = 5.25 \text{ V}, \qquad V_{IN} = 0.5 \text{ V}$								±1	μΑ		
10711	$V_{CC} = 5.5 \text{ V},$	V <sub>OUT</sub> = 2.7 V				10				μА		
IOZH	$V_{CC} = 5.25 \text{ V},$	V <sub>OUT</sub> = 2.7 V							10	μΑ		
lo-	$V_{CC} = 5.5 \text{ V},$	V <sub>OUT</sub> = 0.5 V				-10				μА		
lozL	$V_{CC} = 5.25 \text{ V},$	V <sub>OUT</sub> = 0.5 V							-10	μΑ		
los‡	$V_{CC} = 5.5 \text{ V},$	$V_{OUT} = 0 V$		-60	-120	-225				mA		
105+	$V_{CC} = 5.25 \text{ V},$	$V_{OUT} = 0 V$					-60	-120	-225	ША		
l <sub>off</sub>	$V_{CC} = 0 V$	V <sub>OUT</sub> = 4.5 V				±1			±1	μΑ		
loo	$V_{CC} = 5.5 \text{ V},$	$V_{IN} \le 0.2 V$ ,	$V_{IN} \ge V_{CC} - 0.2 \text{ V}$		0.1	0.2				mA		
Icc	$V_{CC} = 5.25 \text{ V},$	$V_{IN} \le 0.2 V$ ,	$V_{IN} \ge V_{CC} - 0.2 V$					0.1	0.2	IIIA		
Alaa	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> =	= 3.4 V§, f <sub>1</sub> = 0, Out	puts open		0.5	2				mA		
∆lCC	$V_{CC} = 5.25 \text{ V}, V_{IN}$					0.5	2	ША				
	$V_{CC} = 5.5 \text{ V}, O_{ne} \text{ i}$	input switching at 50	0% duty cycle,		0.00	0.40						
_	Outputs open, OE <sub>A</sub> V <sub>IN</sub> ≤ 0.2 V or V <sub>IN</sub>	\ = OEB = GND, ≥ VCC - 0.2 V		0.06	0.12				mA/			
1CCD¶		input switching at 5	50% duty cycle.							MHz		
	Outputs open, OE	$\chi = \overline{OE}_B = GND$ ,	, o, o.o.,					0.06	0.12	.12		
	$V_{IN} \le 0.2 \text{ V or } V_{IN}$	≥ V <sub>CC</sub> – 0.2 V										

<sup>&</sup>lt;sup>†</sup> Typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .



Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample-and-hold techniques are preferable to minimize internal chip heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output can raise the chip temperature well above normal and cause invalid readings in other parametric tests. In any sequence of parameter tests, Ios tests should be performed last.

<sup>§</sup> Per TTL-driven input (V<sub>IN</sub> = 3.4 V); all other inputs at V<sub>CC</sub> or GND

This parameter is derived for use in total power-supply calculations.

### CY54FCT240T, CY74FCT240T 8-BIT BUFFERS/LINE DRIVERS WITH 3-STATE OUTPUTS

SCCS017A - MAY 1994 - REVISED OCTOBER 2001

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

DADAMETER		TEST CONDITIONS					CY	74FCT24	0T	UNIT
PARAMETER		LEST CONDITIONS		MIN	TYP <sup>†</sup>	MAX	MIN	TYP <sup>†</sup>	MAX	UNIT
		One bit switching at f <sub>1</sub> = 10 MHz	$V_{IN} \le 0.2 \text{ V or}$ $V_{IN} \ge V_{CC} - 0.2 \text{ V}$		0.7	1.4				
	$V_{CC} = 5.5 V$ ,	at 50% duty cycle	$V_{IN} = 3.4 \text{ V or GND}$		1	2.4				
	$\frac{\text{Outputs open,}}{\text{OE}_A} = \frac{\text{OE}_B}{\text{OE}_B} = \text{GND}$	Eight bits switching at f <sub>1</sub> = 2.5 MHz	$V_{IN} = 0.2 \text{ V or}$ $V_{IN} \ge V_{CC} - 0.2 \text{ V}$		1.3	2.6				
IC#		at 50% duty cycle	$V_{IN} = 3.4 \text{ V or GND}$		3.3	10.6				mA
IC"		at f <sub>1</sub> = 10 MHz	$V_{IN} \le 0.2 \text{ V or}$ $V_{IN} \ge V_{CC} - 0.2 \text{ V}$					0.7	1.4	IIIA
	$V_{CC} = 5.25 \text{ V},$		$V_{IN} = 3.4 \text{ V or GND}$					1	2.4	
	$\overline{OE}_A = \overline{OE}_B = GND$	Eight bits switching	$V_{IN} = 0.2 \text{ V or}$ $V_{IN} \ge V_{CC} - 0.2 \text{ V}$					1.3	2.6	
		at f <sub>1</sub> = 2.5 MHz at 50% duty cycle	$V_{IN} = 3.4 \text{ V or GND}$					3.3	10.6	
Ci					5	10		5	10	pF
Co					9	12		9	12	pF

 $<sup>\</sup>overline{\dagger}$  Typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

 $^{\#}$ IC = ICC +  $\Delta$ ICC  $\times$  DH  $\times$  NT + ICCD (f<sub>0</sub>/2 + f<sub>1</sub>  $\times$  N<sub>1</sub>)

Where:

IC = Total supply current

ICC = Power-supply current with CMOS input levels

 $\Delta I_{CC}$  = Power-supply current for a TTL high input (V<sub>IN</sub> = 3.4 V)

 $D_H$  = Duty cycle for TTL inputs high  $N_T$  = Number of TTL inputs at  $D_H$ 

I<sub>CCD</sub> = Dynamic current caused by an input transition pair (HLH or LHL)

f<sub>0</sub> = Clock frequency for registered devices, otherwise zero

f<sub>1</sub> = Input signal frequency

N<sub>1</sub> = Number of inputs changing at f<sub>1</sub>

All currents are in milliamperes and all frequencies are in megahertz.

|| Values for these conditions are examples of the I<sub>CC</sub> formula.



## **CY54FCT240T, CY74FCT240T** 8-BIT BUFFERS/LINE DRIVERS WITH 3-STATE OUTPUTS SCCS017A - MAY 1994 - REVISED OCTOBER 2001

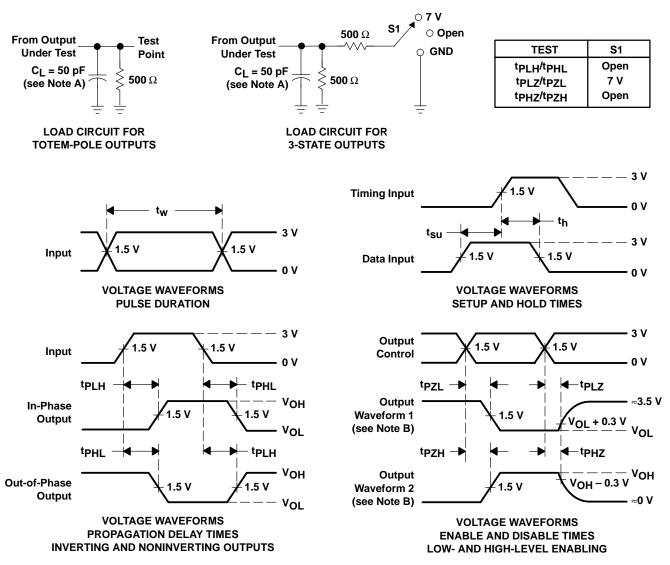
### switching characteristics over operating free-air temperature range (see Figure 1)

DADAMETED	PARAMETER FROM		CY54FC	CY54FCT240T		CY54FCT240AT		CY54FCT240CT	
(INPUT)		(OUTPUT)	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
<sup>t</sup> PLH	D	ō	1.5	9	1.5	5.1	1.5	4.7	20
t <sub>PHL</sub>	D		1.5	9	1.5	5.1	1.5	4.7	ns
<sup>t</sup> PZH	ŌĒ	ō	1.5	10.5	1.5	6.5	1.5	5.7	20
t <sub>PZL</sub>	OE	U	1.5	10.5	1.5	6.5	1.5	5.7	ns
<sup>t</sup> PHZ	ŌĒ	ō	1.5	10	1.5	5.9	1.5	4.6	20
<sup>t</sup> PLZ	OE .	0	1.5	10	1.5	5.9	1.5	4.6	ns

### switching characteristics over operating free-air temperature range (see Figure 1)

DADAMETED	FROM	то	CY74FC	CY74FCT240T		CY74FCT240AT		CY74FCT240CT	
PARAMETER	(INPUT)	(OUTPUT)	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
<sup>t</sup> PLH	D	ō		8	1.5	4.8	1.5	4.3	20
<sup>t</sup> PHL	D	O	1.5	8	1.5	4.8	1.5	4.3	ns
<sup>t</sup> PZH	ŌĒ	ō	1.5	10	1.5	6.2	1.5	5	no
t <sub>PZL</sub>	OE	U	1.5	10	1.5	6.2	1.5	5	ns
<sup>t</sup> PHZ	ŌĒ	ō	1.5	9.5	1.5	5.6	1.5	4.5	no
<sup>t</sup> PLZ	) OE		1.5	9.5	1.5	5.6	1.5	4.5	ns

#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms









#### **PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp (3)
5962-9220301M2A	ACTIVE	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
5962-9220301MRA	ACTIVE	CDIP	J	20	1	None	Call TI	Level-NC-NC-NC
5962-9220301MSA	ACTIVE	CFP	W	20	1	None	Call TI	Level-NC-NC-NC
5962-9220302M2A	ACTIVE	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
5962-9220302MRA	ACTIVE	CDIP	J	20	1	None	Call TI	Level-NC-NC-NC
5962-9220302MSA	ACTIVE	CFP	W	20	1	None	Call TI	Level-NC-NC-NC
5962-9220303M2A	ACTIVE	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
5962-9220303MRA	ACTIVE	CDIP	J	20	1	None	Call TI	Level-NC-NC-NC
5962-9220303MSA	ACTIVE	CFP	W	20	1	None	Call TI	Level-NC-NC-NC
5962-9221301MRA	ACTIVE	CDIP	J	20	1	None	Call TI	Level-NC-NC-NC
5962-9221303M2A	ACTIVE	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
5962-9221303MRA	ACTIVE	CDIP	J	20	1	None	Call TI	Level-NC-NC-NC
5962-9221305MRA	ACTIVE	CDIP	J	20	1	None	Call TI	Level-NC-NC-NC
CY54FCT240ATDMB	ACTIVE	CDIP	J	20	1	None	Call TI	Level-NC-NC-NC
CY54FCT240ATLMB	ACTIVE	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
CY54FCT244ATDMB	ACTIVE	CDIP	J	20	1	None	Call TI	Level-NC-NC-NC
CY54FCT244ATLMB	ACTIVE	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
CY54FCT244ATW	ACTIVE	CFP	W	20	1	None	Call TI	Level-NC-NC-NC
CY54FCT244CTDMB	ACTIVE	CDIP	J	20	1	None	Call TI	Level-NC-NC-NC
CY54FCT244CTW	ACTIVE	CFP	W	20	1	None	Call TI	Level-NC-NC-NC
CY54FCT244TDMB	ACTIVE	CDIP	J	20	1	None	Call TI	Level-NC-NC-NC
CY54FCT244TLMB	ACTIVE	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
CY54FCT244TW	ACTIVE	CFP	W	20	1	None	Call TI	Level-NC-NC-NC
CY74FCT240ATQCT	ACTIVE	SSOP/ QSOP	DBQ	20	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
CY74FCT240ATSOC	ACTIVE	SOIC	DW	20	25	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
CY74FCT240ATSOCT	ACTIVE	SOIC	DW	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
CY74FCT240CTQCT	ACTIVE	SSOP/ QSOP	DBQ	20	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
CY74FCT240CTSOC	ACTIVE	SOIC	DW	20	25	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
CY74FCT240CTSOCT	ACTIVE	SOIC	DW	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
CY74FCT240TQCT	ACTIVE	SSOP/ QSOP	DBQ	20	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
CY74FCT240TSOC	ACTIVE	SOIC	DW	20	25	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
CY74FCT240TSOCT	ACTIVE	SOIC	DW	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
CY74FCT244ATPC	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
CY74FCT244ATQCT	ACTIVE	SSOP/ QSOP	DBQ	20	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM





com 28-Feb-2005

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finisl	h MSL Peak Temp <sup>(3)</sup>
CY74FCT244ATSOC	ACTIVE	SOIC	DW	20	25	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
CY74FCT244ATSOCT	ACTIVE	SOIC	DW	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
CY74FCT244CTQCT	ACTIVE	SSOP/ QSOP	DBQ	20	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
CY74FCT244CTSOC	ACTIVE	SOIC	DW	20	25	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
CY74FCT244CTSOCT	ACTIVE	SOIC	DW	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
CY74FCT244DTQCT	ACTIVE	SSOP/ QSOP	DBQ	20	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
CY74FCT244DTSOC	ACTIVE	SOIC	DW	20	25	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
CY74FCT244DTSOCT	ACTIVE	SOIC	DW	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
CY74FCT244TQCT	ACTIVE	SSOP/ QSOP	DBQ	20	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
CY74FCT244TSOC	ACTIVE	SOIC	DW	20	25	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
CY74FCT244TSOCT	ACTIVE	SOIC	DW	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM

<sup>&</sup>lt;sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - May not be currently available - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

None: Not yet available Lead (Pb-Free).

**Pb-Free** (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDECindustry standard classifications, and peak solder temperature.

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