51256SL
256K (32K x 8) CMOS SLOW STATIC RAM

■ **Performance Range**

Symbol	Parameter	51256SL-10	Unit
t_{AA}	Address Access Time	100	ns
t_{ACS}	Chip Select Access Time	100	ns
t_{OE}	Output Enable Access Time	50	ns

■ **Static Operation**
  — No Clock/Refresh Required

■ **Equal Access and Cycle Times**
  — Simplifies System Design

■ **Single +5V Supply**

■ **Power Down Mode**

■ **TTL Compatible**

■ **Common Data Input and Output**

■ **High Reliability 28-Pin 600 Mil PDIP (P) and 28-Pin SOP (PG) Package Types**

Intel's 51256SL is a 32768-word by 8-bit CMOS static RAM fabricated using CMOS Silicon Gate process.

When the Chip Select is brought high, the device assumes a standby mode in which the standby current is reduced to 2 μA (typ) @ 25°C. The device has a data retention mode that guarantees that data will remain valid at minimum V_{CC} of 2.0V.


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Figure 1. Block Diagram

Pin Connections

A_{14}	1	28	V_{CC}
A_{12}	2	27	$\overline{WE}$
A_7	3	26	A_{13}
A_6	4	25	A_8
A_5	5	24	A_9
A_4	6	23	A_{11}
A_3	7	22	$\overline{OE}$
A_2	8	21	A_{10}
A_1	9	20	$\overline{CS}$
A_0	10	19	D_7
D_0	11	18	D_6
D_1	12	17	D_5
D_2	13	16	D_4
GND	14	15	D_3

Pin Names

$A_0 - A_{14}$	Address
$D_0 - D_7$	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
V_{CC}	Power
GND	Ground
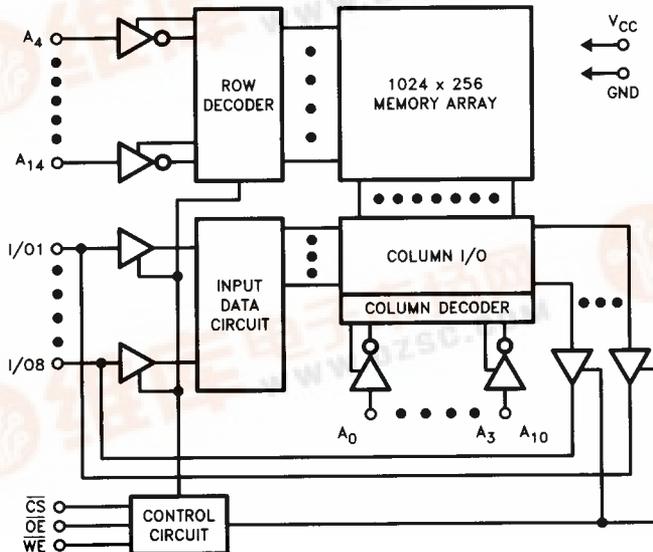
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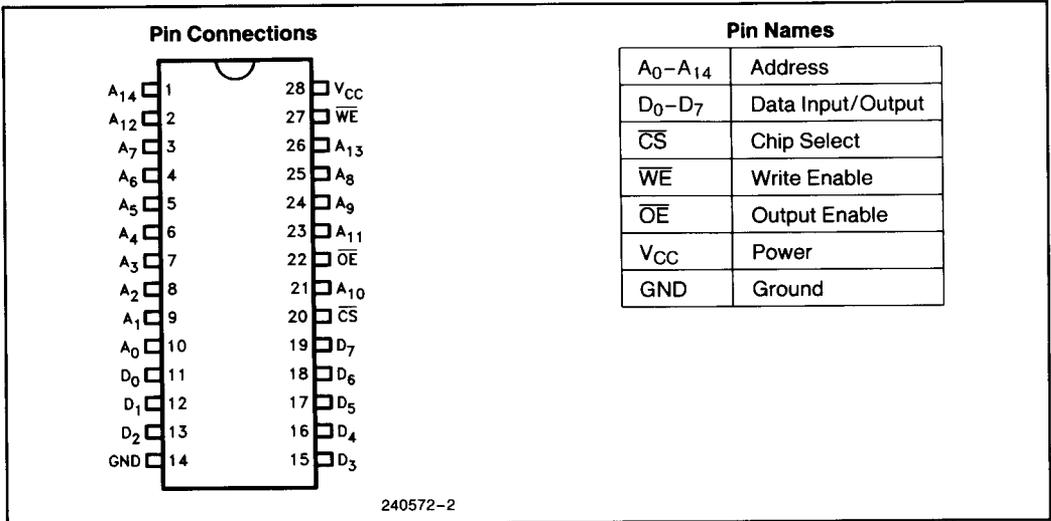
Device Operation

The 51256SL has two control inputs: Chip Select ($\overline{CS}$) and Write Enable ($\overline{WE}$). $\overline{CS}$ is the power control pin used for device operation. $\overline{WE}$ is the data control pin used to gate data at the I/O pins. Out Enable (OE) is used for precise control of the outputs.

Table 1. Mode Selection Truth Table

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O	Power
H	X	X	Standby	High Z	Standby
L	X	H	Read	High Z	Active
L	H	L	Read	D_{OUT}	Active
L	L	X	Write	D_{IN}	Active

ABSOLUTE MAXIMUM RATINGS

Voltage on Any Pin
  Relative to Ground (V_{IN}, V_{OUT}) ..... −0.3V to 7V
Storage Temperature (T_{STG}) .... −55°C to +150°C
Power Dissipation (P_D) 1.0W
DC Continuous Output Current (I_{OS}) .... 50 mA

RECOMMENDED OPERATING CONDITIONS

Voltage referenced to V_{SS}, T_A = 0°C to 70°C

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2		V_{CC} + 0.5	V
Input Low Voltage	V_{IL}	−0.3		0.8	V

NOTE:
V_{IL} (Min) = −3.0V for 20 ns pulse.

CAPACITANCE T_A = 25°C, f = 1.0 MHz

Symbol	Parameter	Min	Max	Unit
C_{IN1}	Input Capacitance (V_{IN} = 0V)		8	pF
C_{OUT}	Output Capacitance (V_{OUT} = 0V)		10	pF

NOTE:
This parameter is sampled and not 100% tested.

DC AND OPERATING CHARACTERISTICS

Recommended Operating Conditions unless otherwise noted

Symbol	Parameter		Min	Typ*	Max	Units	Test Conditions
I_{CC1}	Operating Current			30	50	mA	V_{CC} = Max, $\overline{CS}$ = V_{IL} I/O Open
I_{CC2}	Dynamic Operating Current			35	70	mA	Min Cycle, $\overline{CS}$ = V_{IL} V_{CC} = Max, I/O Open
I_{SB}				—	3	mA	$\overline{CS}$ = V_{IH}
I_{SB1}	Standby Current	Std.	—	—	1	mA	$\overline{CS}$ = V_{CC} ≥ 0.2V
		L	—	2	100	μA	
I_{LI}	Input Load Current		−2		2	μA	V_{CC} = Max V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage		−2		2	μA	$\overline{CS}$ = V_{IH} V_{OUT} = Ground to V_{CC}
V_{OH}	Output High Voltage		2.4			V	I_{OH} = −1.0 mA
V_{OL}	Output Low Voltage				0.4	V	I_{OL} = −2.1 mA

*V_{CC} = 5V, T_A = 25°C

DATA RETENTION ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Min	Typ*	Max	Units	Test Conditions
V_{CDR}	Voltage for Data Retention	2			V	
I_{CCDR}	Data Retention Current		2	50	μA	$\overline{CS} \geq V_{CC} - 0.2V$ $V_{CC} = 3.0V$
t_{CDR}	Chip Deselect to Data Retention Time	0			ns	
t_R	Operation Recovery Time	t_{RC}**			ns	

*Typ: 3V @ 25°C
**t_{RC} = Read Cycle Time

LOW V_{CC} DATA RETENTION WAVEFORM

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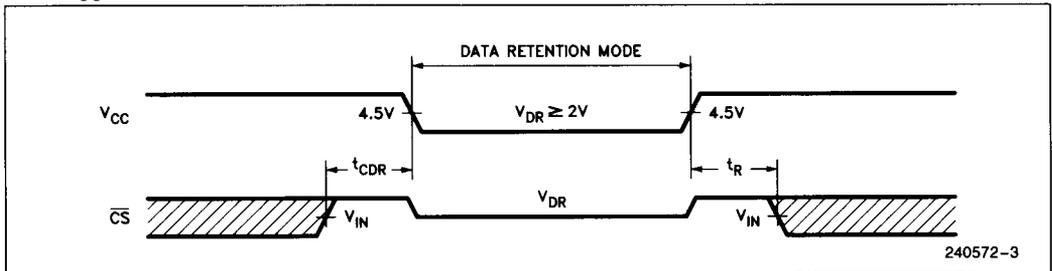
AC TEST CONDITIONS

Input Pulse Levels .0.8V to 2.4V

Input Rise and Fall Times .5 ns

Timing Reference Level 1.5V

Output Load. . . . . .1 TTL Load + 100 pF

AC CHARACTERISTICS (READ CYCLE)

T_A = 0°C to 70°C, V_{CC} = 5V ±10%

READ CYCLE

Symbol	Parameter	51256SL-10		Unit
		Min	Max	
t_{RC}	READ Cycle Time	100		ns
t_{AA}	Address Access Time		100	ns
t_{ACS}	Chip Select Access Time		100	ns
t_{OH}	Output Hold from Address Change	10		ns
t_{CLZ}	Chip Selection to Output in Low Z	10		ns
t_{CHZ}	Chip Deselection to Output in High Z	0	35	ns
t_{OE}	Output Enable Access Time		50	ns
t_{OLZ}	Output Enable to Output in Low Z	5		ns
t_{OHZ}	Output Disable to Output in High Z	0	35	ns

TIMING DIAGRAMS (READ CYCLE)

READ CYCLE[1]

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READ CYCLE 2[1, 2, 4]

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READ CYCLE 3[1, 3, 4]

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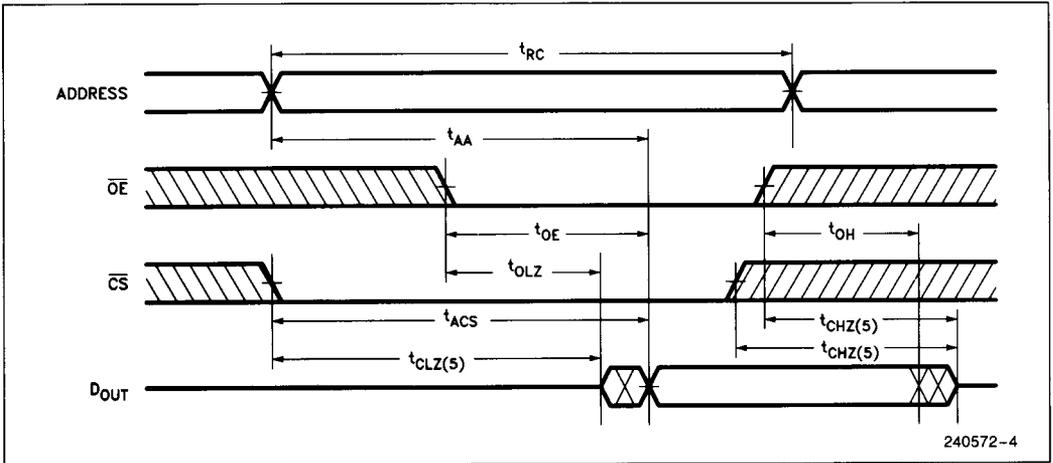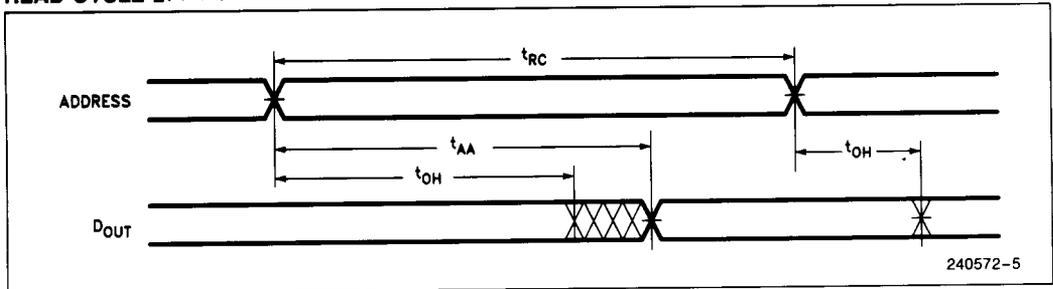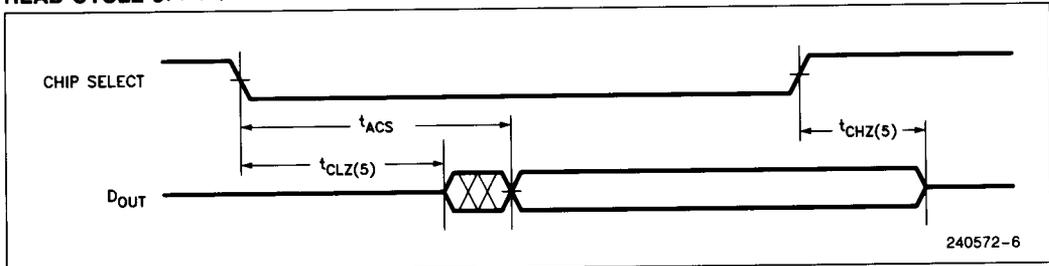
NOTES:
1. $\overline{WE}$ is high for Read Cycle.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE} = V_{IL}$.
5. Transition is measured +500 mV from steady. This parameter is sampled and not 100% tested.

AC CHARACTERISTICS (WRITE CYCLE)

WRITE CYCLE

Symbol	Parameter	51256SL-10		Unit
		Min	Max	
t_{WC}	WRITE Cycle Time	100		ns
t_{CW}	Chip Selection to End of Write	80		ns
t_{AW}	Address Valid to End of Write	80		ns
t_{AS}	Address Set-Up Time	0		ns
t_{WP}	Write Pulse Width	70		ns
t_{WR}	Write Recovery Time	5		ns
t_{DW}	Data Valid to End of Write	40		ns
t_{DH}	Data Hold Time	0		ns
t_{WHZ}	Write Enable to Output in High Z	0	35	ns
t_{OW}	Output Active from End of Write	10		ns
t_{OHZ}	Output Disable to Output in High Z	0	35	ns

TIMING DIAGRAMS (WRITE CYCLE)

WRITE CYCLE 1[1]
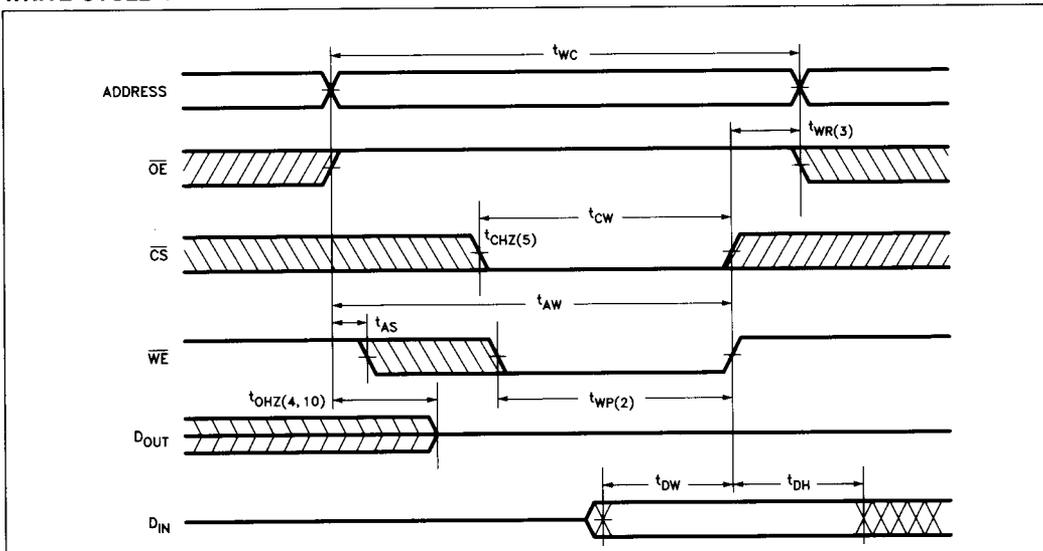
TIMING DIAGRAMS (WRITE CYCLE) (CONTINUED)

WRITE CYCLE 2[1, 6]
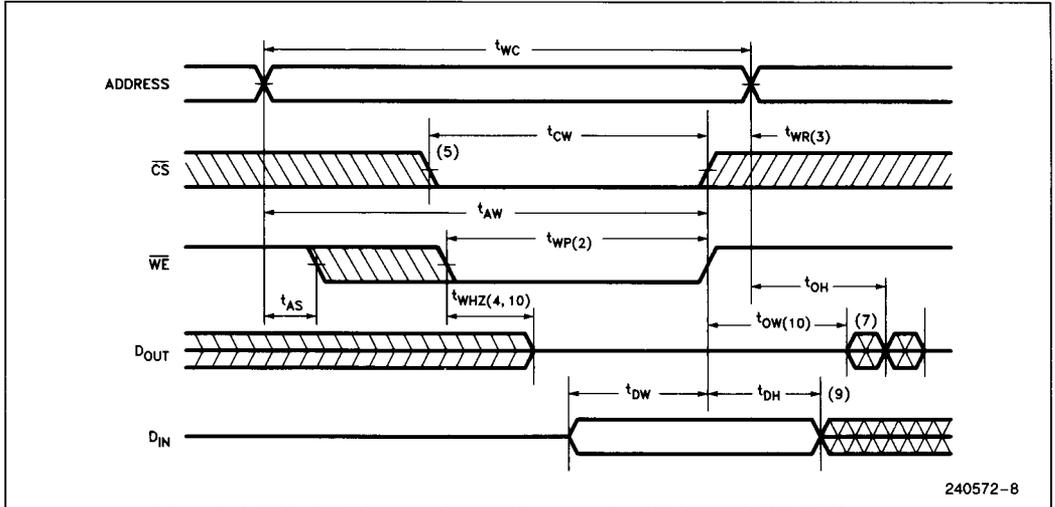
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NOTES:

1. $\overline{WE}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
6. $\overline{OE}$ is continuously low ($\overline{OE} = V_{IL}$).
7. D_{OUT} is the same phase of write data of this write cycle.
8. D_{OUT} is the read data of next address.
9. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the output must not be applied to them.
10. Transition is measured ±500 mV from steady state. This parameter is sampled and not 100% tested.

PACKAGE OUTLINE

0° ~ 15°

0.55 (14.0) MAX

0.60 (15.24) TYP

0.008 (0.20) / 0.012 (0.30)

1.465 (37.2) MAX

0.145 (3.68) / 0.155 (3.93)

0.120 (3.05) MIN

0.020 (0.51) MIN

0.1 (2.54) TYP

0.060 (1.52) TYP

0.014 (0.36) / 0.022 (0.56)

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Units = inches
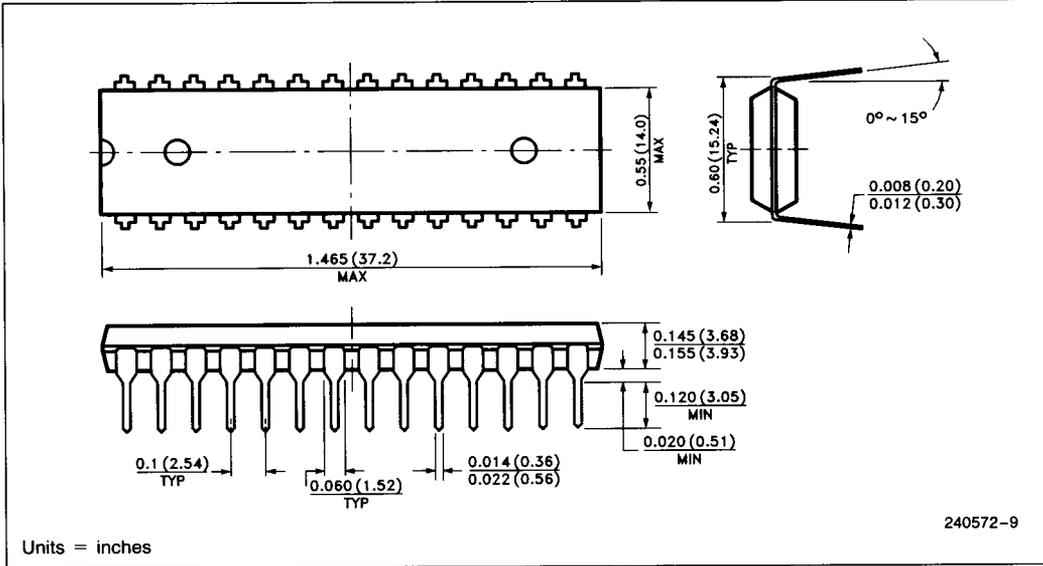
Figure 2. 28-Lead Plastic Dual In-Line Package (P)

28 - 0.4 ± 0.1   P - 1.27 TYP.   ⊕ Ø 0.12 Ⓜ

28   15

(1.7)

8.6 ± 0.2   12.0 ± 0.4   (10.6)

(1.7)

1   14

18.0 ± 0.2   0.15 ± 0.05

1.025   1.025   2.2 ± 0.2

0.15

0.1 ± 0.1

□ 0.15

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Units = millimeter (mm)