

Structure	Silicon Monolithic Integrated Circuit
Product name	Power management IC for cellular phone
Type	BH6951GU
Features	Including switching regulator (DC/DC MODE changes LDO at low load)

○ Absolute maximum ratings (Ta=25°C)

Parameter	Symbol	Limit	Unit	Condition
Maximum applied voltage	VCC	7.0	V	
Power dissipation	Pd	870 (*1)	mW	At single unit
Operating temperature range	Topr	-30 ~ +75	°C	
Storage temperature range	Tstr	-55 ~ +125	°C	

(*1) 50mm×58mm×1.75mm At glass epoxy board mounting.

When it's used by more than Ta=25 °C, it's reduced by 8.7mW/°C.

○ Recommended operating range (Ta=-30 °C~+75 °C)

Parameter	Symbol	Limit			Unit	Condition
		Min.	Typ.	Max.		
Power supply voltage	VCC	3.0	3.6	4.5	V	BATP voltage

This chip is not designed to protect itself against radioactive rays.

Status of this document

The Japanese version of this document is the formal specification. A customer may use this translation version only for a reference to help reading the formal version. If there are any differences in translation version of this document, formal version takes priority.

Application example

The product described in this specification is designed to be used with ordinary electronic equipment or devices (such as audio-visual equipment, office-automation equipment, communications devices, electrical appliances, and electronic toys).

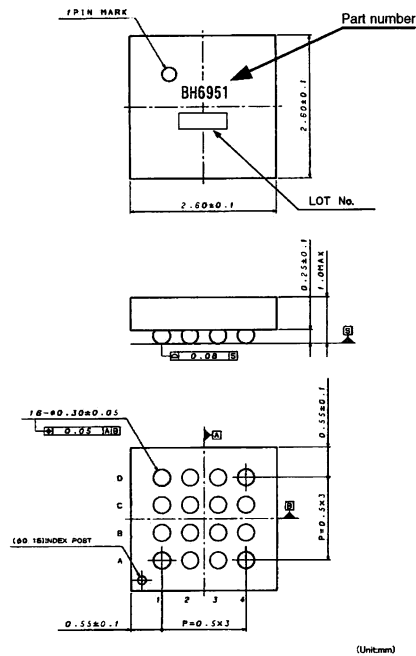
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○Electrical characteristic

Unless otherwise specified Ta=25°C, VCC=BATP=3.6V

Parameter		Symbol	Spec			Unit	Condition
			Min.	Typ.	Max.		
Circuit current (No load)							
Circuit current 1		ICC1	-	8.1	14.0	μA	SWEN=0V,MODE=0V (Operated only reference voltage source)
Circuit current 2		ICC2	-	4.2	5.8	mA	SWEN,MODE=2.8V
Circuit current 3		ICC3	-	24	42.4	μA	SWEN =2.8V, MODE=0V
SWREG							
Input voltage range		Vi	3.0	3.6	4.5	V	
1.5V Output voltage range	SW mode	Vosw1	1.450	1.500	1.550	V	Io=400mA,MODE=3.6V SWVSEL=0V
	LDO mode	Voldo1	1.450	1.500	1.550	V	Io=50mA,MODE=0V SWVSEL=0V
1.2V Output voltage range	SW mode	Vosw2	1.150	1.200	1.250	V	Io=400mA,MODE=3.6V SWVSEL=3.6V
	LDO mode	Voldo2	1.150	1.200	1.250	V	Io=50mA,MODE=0V SWVSEL=3.6V
Output current	SW mode	Iosw	-	-	400	mA	
	LDO mode	Ioldo		-	100	mA	
Efficiency		Eff	-	85	-	%	Io=100mA, Vo=1.5V
			-	85	-	%	Io=200mA, Vo=1.5V
Oscillator frequency		Fosc	0.78	1.05	1.35	MHz	SW mode
Control I/F 1 (SWEN,MODE)							
Input current H level		IIH1	-10	1.95	10	μA	VIH=3.6V
Input current L level		IIL1	-10	0	10	μA	VIL=0V
Control I/F 2 (SWVSEL)							
Input current H level		IIH2	-10	0	10	μA	VIH=3.6V
Input current L level		IIL2	-10	0	10	μA	VIL=0V
Control I/F 3 (SWEN,MODE)							
Input voltage H level		VIH	1.4	-	-	V	
Input voltage L level		VIL	-	0	0.25	V	
Control I/F 4 (SWVSEL)							
Input voltage H level		VIH	VCC×0.8	-	VCC	V	
Input voltage L level		VIL	-	-	VCC×0.2	V	
UVLO (Under Voltage Lock Out)							
Detect voltage 1		VDETHL	2.4	2.5	2.6	V	VCC=3.6→0V SWEEP
Hystelisis		VHYS	25	50	100	mV	

○ Dimensions diagram, Marking diagram

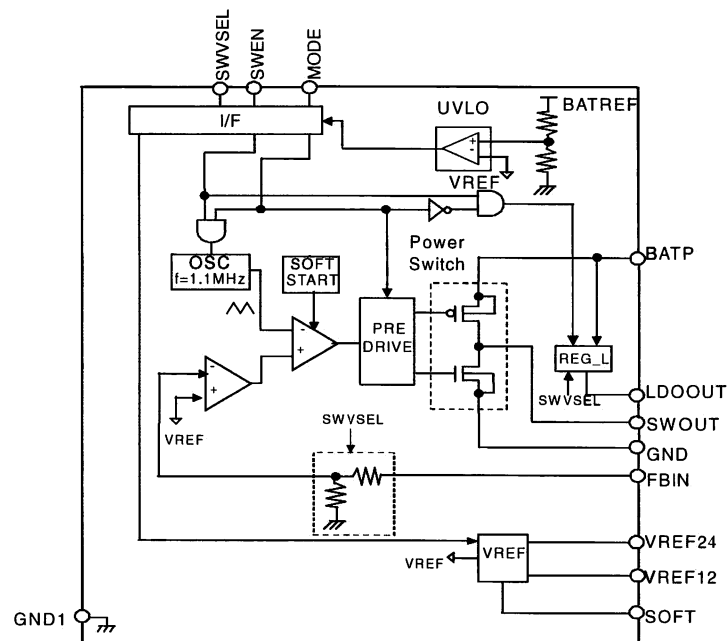


VCSP85H2(16pin) (unit:mm)

○ Pin assignment table

PIN	Pin name	PIN	Pin name
C3	VREF24	B3	SOFT
C4	VREF12	A3	MODE
D3	GND1	B4	SWEN
B2	GNDP	D2	SWVSEL
B1	SWOUT	A1	T1
C1	LDOOUT	A4	T2
C2	BATP	D4	T3
A2	FBIN	D1	T4

○ Block diagram



○ Cautions on use

(1) Absolute Maximum Ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

(2) Power supply and GND line

Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines. Pay attention to the interference by common impedance of layout pattern when there are plural power supplies and GND lines. Especially, when there are GND pattern for small signal and GND pattern for large current included the external circuits, please separate each GND pattern. Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use a capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

(3) GND voltage

Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

(4) Short circuit between terminals and erroneous mounting

In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

(5) Operation in strong electromagnetic field

Be noted that using ICs in the strong electromagnetic field can malfunction them.

(6) Input terminals

In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

(7) External capacitor

In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

(8) Thermal shutdown circuit (TSD)

When junction temperatures become 150°C (typ) or higher, the thermal shutdown circuit operates and turns a switch OFF. The thermal shutdown circuit, which is aimed at isolating the LSI from thermal runaway as much as possible, is not aimed at the protection or guarantee of the LSI. Therefore, do not continuously use the LSI with this circuit operating or use the LSI assuming its operation.

(9) Thermal design

Perform thermal design in which there are adequate margins by taking into account the permissible dissipation (Pd) in actual states of use.

(10) LDO

Use each output of LDO by the independence. Don't use under the condition that each output is short-circuited because it has the possibility that the operation becomes unstable.

(11) DC/DC converter

Select the low DCR inductors to decrease power loss for DC/DC converter.

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Taiwan / Taipei	TEL : +866(2)2500-6956	FAX : +866(2)2503-2869
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Japan /
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Tokyo	2-1-1, Yaesu, Chuo-ku, Tokyo 104-0082	
	TEL : +81(3)5203-0321	FAX : +81(3)5203-0300
Yokohama	2-4-8, Shin Yokohama, Kohoku-ku, Yokohama, Kanagawa 222-8575	
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	TEL : +81(52)581-8521	FAX : +81(52)561-2173
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	TEL : +81(75)311-2121	FAX : +81(75)314-6559
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