



CS52843

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Current Mode PWM Control Circuit

Description

The CS52843 provides all the necessary features to implement off-line fixed frequency current-mode control with a minimum number of external components.

The CS52843 incorporates a new precision temperature-controlled oscillator to minimize variations in frequency. An undervoltage lock-out ensures that V_{REF} is stabilized

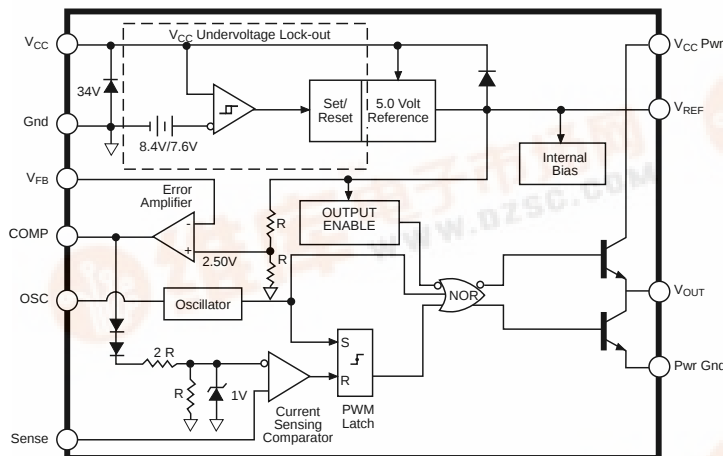
before the output stage is enabled. In the CS52843 turn on is at 8.4V and turn off at 7.6V.

Other features include low start-up current, pulse-by-pulse current limiting, and a high-current totem pole output for driving capacitive loads, such as gate of a power MOSFET. The output is low in the off state, consistent with N-channel devices.

Absolute Maximum Ratings

Supply Voltage ($I_{CC} < 30\text{mA}$)	Self Limiting
Supply Voltage (Low Impedance Source)	30V
Output Current	$\pm 1\text{A}$
Output Energy (Capacitive Load)	$5\mu\text{J}$
Analog Inputs (V_{FB} , V_{SENSE})	-0.3V to 5.5V
Error Amp Output Sink Current	10mA
Lead Temperature Soldering	
Reflow (SMD styles only)	60 sec. max above 183°C, 230°C peak

Block Diagram

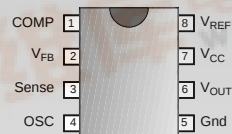


Features

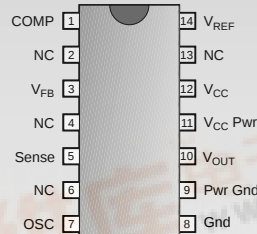
- Optimized for Off-line Control
- Internally Temperature Compensated Oscillator
- V_{REF} Stabilized before Output Stage is Enabled
- Very Low Start-up Current 300 μA (typ)
- Pulse-by-pulse Current Limiting
- Improved Undervoltage Lockout
- Double Pulse Suppression
- 2% 5 Volt Reference
- High Current Totem Pole Output

Package Options

8L SO Narrow



14L SO Narrow



Cherry Semiconductor

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Electrical Characteristics: $-40 \leq T_A \leq 85^\circ\text{C}$; $V_{CC} = 15\text{V}$ (Note 1); $R_T = 680\Omega$; $C_T = .022\mu\text{F}$ for triangle mode, $R_T = 10\text{k}\Omega$; $C_T = 3.3\text{nF}$ sawtooth mode unless otherwise stated.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
■ Reference Section					
Output Voltage	$T_J = 25^\circ\text{C}$, $I_{REF} = 1\text{mA}$	4.90	5.00	5.10	V
Line Regulation	$12 \leq V_{CC} \leq 25\text{V}$		6	20	mV
Load Regulation	$1 \leq I_{REF} \leq 20\text{mA}$		6	25	mV
Temperature Stability	(Note 1)		0.2	0.4	mV/ $^\circ\text{C}$
Total Output Variation	Line, Load, Temp. (Note 1)	4.82		5.18	V
Output Noise Voltage	$10\text{Hz} \leq f \leq 10\text{kHz}$, $T_J = 25^\circ\text{C}$ (Note 1)		50		μV
Long Term Stability	$T_A = 125^\circ\text{C}$, 1000 Hrs. (Note 1)		5	25	mV
Output Short Circuit	$T_A = 25^\circ\text{C}$	-30	-100	-180	mA
■ Oscillator Section					
Initial Accuracy	Sawtooth Mode, $T_J = 25^\circ\text{C}$ (Note 1)	47	52	57	kHz
	Triangle Mode, $T_J = 25^\circ\text{C}$	44	52	60	kHz
Voltage Stability	$12 \leq V_{CC} \leq 25\text{V}$		0.2	1.0	%
Temperature Stability	Sawtooth Mode $T_{MIN} \leq T_A \leq T_{MAX}$		5		%
	Triangle Mode $T_{MIN} \leq T_A \leq T_{MAX}$ (Note 1)		8		%
Amplitude	V_{OSC} (peak to peak)		1.7		V
Discharge Current	$T_J = 25^\circ\text{C}$	7.3	8.3	9.3	mA
	$T_{MIN} \leq T_A \leq T_{MAX}$	6.8		9.8	mA
■ Error Amp Section					
Input Voltage	$V_{COMP} = 2.5\text{V}$	2.42	2.50	2.58	V
Input Bias Current	$V_{FB} = 0\text{V}$		-0.3	-2.0	μA
A_{VOL}	$2 \leq V_{OUT} \leq 4\text{V}$	65	90		dB
Unity Gain Bandwidth	(Note 1)	0.7	1.0		MHz
PSRR	$12 \leq V_{CC} \leq 25\text{V}$	60	70		dB
Output Sink Current	$V_{FB} = 2.7\text{V}$, $V_{COMP} = 1.1\text{V}$	2	6		mA
Output Source Current	$V_{FB} = 2.3\text{V}$, $V_{COMP} = 5\text{V}$	-0.5	-0.8		mA
V_{OUT_HIGH}	$V_{FB} = 2.3\text{V}$, $R_L = 15\text{k}\Omega$ to Gnd	5	6		V
V_{OUT_LOW}	$V_{FB} = 2.7\text{V}$, $R_L = 15\text{k}\Omega$ to V_{REF}		0.7	1.1	V
■ Current Sense Section					
Gain	(Notes 2 & 3)	2.85	3.00	3.15	V/V
Maximum Input Signal	$V_{COMP} = 5\text{V}$ (Note 2)	0.9	1.0	1.1	V
PSRR	$12 \leq V_{CC} \leq 25\text{V}$ (Note 2)		70		dB
Input Bias Current	$V_{Sense} = 0\text{V}$		-2	-10	μA
Delay to Output	$T_J = 25^\circ\text{C}$ (Note 1)		150	300	ns
■ Output Section					
Output Low Level	$I_{SINK} = 20\text{mA}$		0.1	0.4	V
	$I_{SINK} = 200\text{mA}$		1.5	2.2	V
Output High Level	$I_{SOURCE} = 20\text{mA}$	13.0	13.5		V
	$I_{SOURCE} = 200\text{mA}$	12.0	13.5		V

Electrical Characteristics: $-40 \leq T_A \leq 85^\circ\text{C}$; $V_{CC} = 15\text{V}$ (Note 1); $R_T = 680\Omega$; $C_T = .022\mu\text{F}$ for triangle mode, $R_T = 10\text{k}\Omega$; $C_T = 3.3\text{nF}$ sawtooth mode unless otherwise stated.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Rise Time	$T_J = 25^\circ\text{C}$, $C_L = 1\text{nF}$ (Note 1)		50	150	ns
Fall Time	$T_J = 25^\circ\text{C}$, $C_L = 1\text{nF}$ (Note 1)		50	150	ns
Output Leakage	UVLO Active $V_{OUT} = 0$		-.01	-10.0	μA

■ Total Standby Current

Start-Up Current			300	500	μA
Operating Supply Current	$V_{FB} = V_{\text{Sense}} = 0\text{V}$ $R_T = 10\text{k}\Omega$, $C_T = 3.3\text{nF}$		11	17	mA
V_{CC} Zener Voltage	$I_{CC} = 25\text{mA}$		34		V

■ Undervoltage Lockout Section

Start Threshold		7.8	8.4	9.0	V
Min. Operating Voltage	After Turn On	7.0	7.6	8.2	V

Notes: 1. These parameters, although guaranteed, are not 100% tested in production.

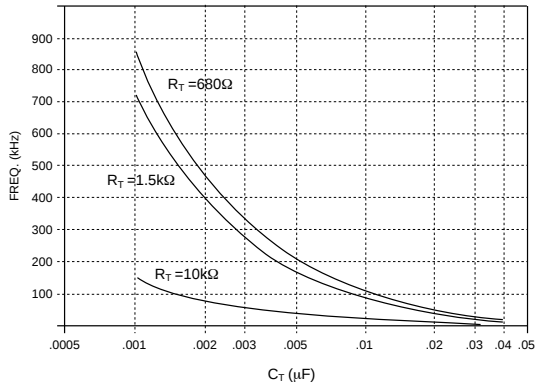
2. Parameter measured at trip point of latch with $V_{FB} = 0$.

3. Gain defined as: $A = \frac{\Delta V_{\text{COMP}}}{\Delta V_{\text{Sense}}}$; $0 \leq V_{\text{Sense}} \leq 0.8\text{V}$.

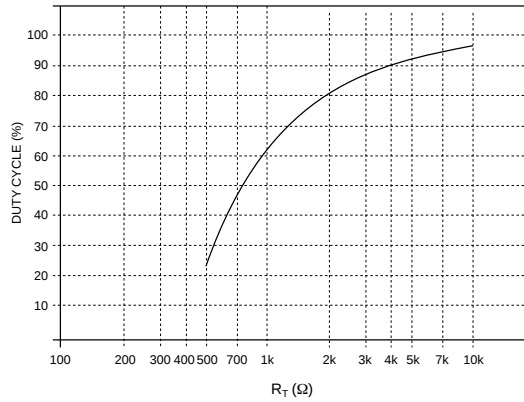
Package Pin Description

PACKAGE PIN #		PIN SYMBOL	FUNCTION
8L SO Narrow	14L SO Narrow		
1	1	COMP	Error amp output, used to compensate error amplifier.
2	3	V_{FB}	Error amp inverting input.
3	5	Sense	Noninverting input to Current Sense Comparator.
4	7	OSC	Oscillator timing network with Capacitor to Ground, resistor to V_{REF} .
5	8	Gnd	Ground.
5	9	Pwr Gnd	Output driver Ground.
6	10	V_{OUT}	Output drive pin.
7	11	V_{CCPwr}	Output driver positive supply.
7	12	V_{CC}	Positive power supply.
8	14	V_{REF}	Output of 5V internal reference.
2,4,6,13		NC	No Connection.

Typical Performance Characteristics

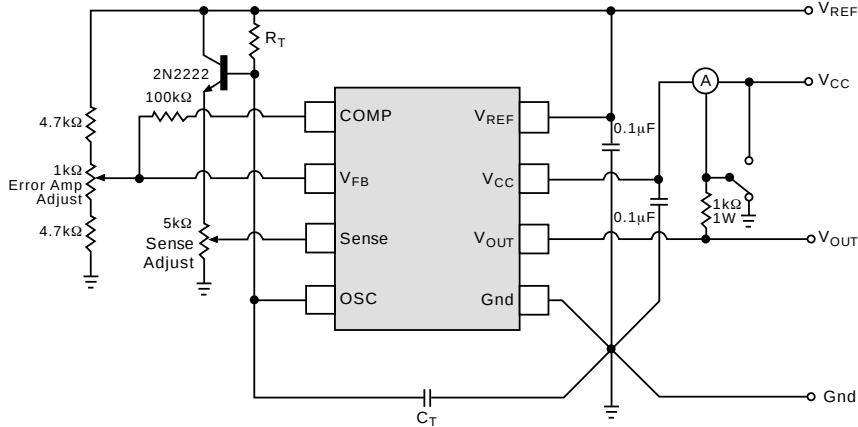


Oscillator Frequency vs C_T



Oscillator Duty Cycle vs R_T

Test Circuit Open Loop Laboratory Test Fixture



Circuit Description

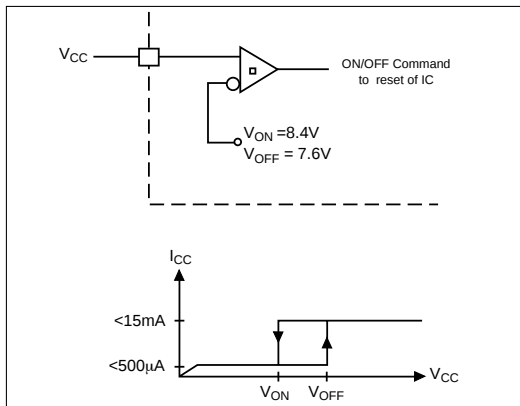


Figure 1: Startup voltage for the CS52843.

Undervoltage Lockout

During Undervoltage Lockout (Figure 1), the output driver is biased to sink minor amounts of current. The output should be shunted to ground with a resistor to prevent activating the power switch with extraneous leakage currents.

PWM Waveform

To generate the PWM waveform, the control voltage from the error amplifier is compared to a current sense signal which represents the peak output inductor current (Figure 2). An increase in V_{CC} causes the inductor current slope to increase, thus reducing the duty cycle. This is an inherent feed-forward characteristic of current mode control, since the control voltage does not have to change during changes of input supply voltage.

When the power supply sees a sudden large output current increase, the control voltage will increase allowing the duty cycle to momentarily increase. Since the duty cycle tends to exceed the maximum allowed to prevent transformer saturation in some power supplies, the internal oscillator waveform provides the maximum duty cycle clamp as programmed by the selection of oscillator timing components.

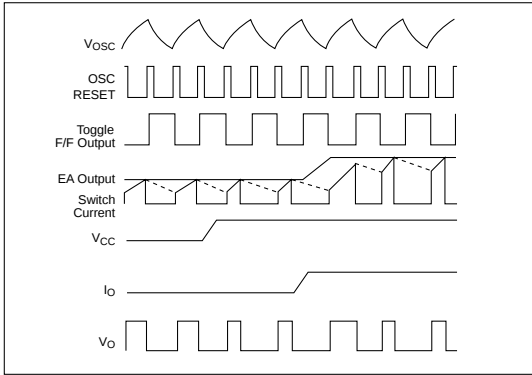


Figure 2: Timing Diagram

Setting the Oscillator

The times T_c and T_d can be determined as follows:

$$t_c = R_T C_T \ln \left(\frac{V_{REF} - V_{LOWER}}{V_{REF} - V_{UPPER}} \right)$$

$$t_d = R_T C_T \ln \left(\frac{V_{REF} - I_d R_T - V_{LOWER}}{V_{REF} - I_d R_T - V_{UPPER}} \right)$$

Substituting in typical values for the parameters in the above formulas:

$V_{REF} = 5.0V$, $V_{UPPER} = 2.7V$, $V_{LOWER} = 1.0V$, $I_d = 8.3mA$, then

$$t_c \approx 0.5534 R_T C_T$$

$$t_d = R_T C_T \ln \left(\frac{2.3 - 0.0083 R_T}{4.0 - 0.0083 R_T} \right)$$

For better accuracy R_T should be $\geq 10k\Omega$.

Grounding

High peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to Gnd in a single point ground.

The transistor and $5k\Omega$ potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to Sense.

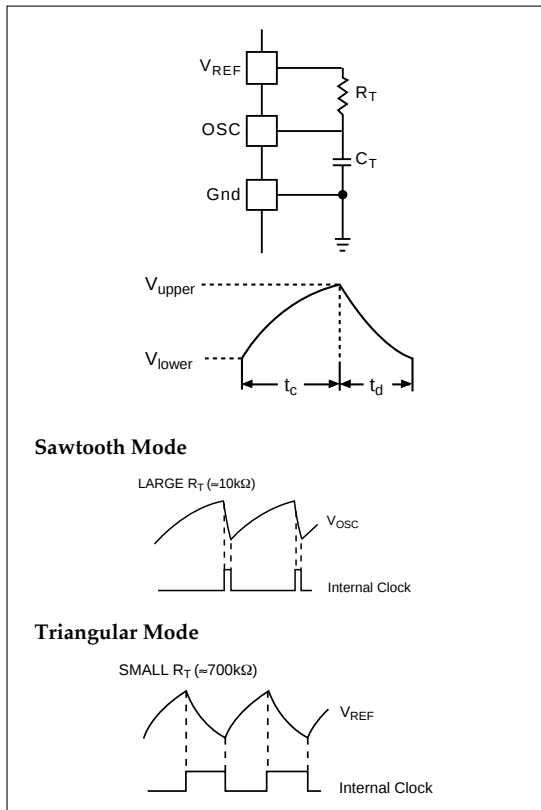


Figure 3: Oscillator Timing Network and Parameters

Package Specification

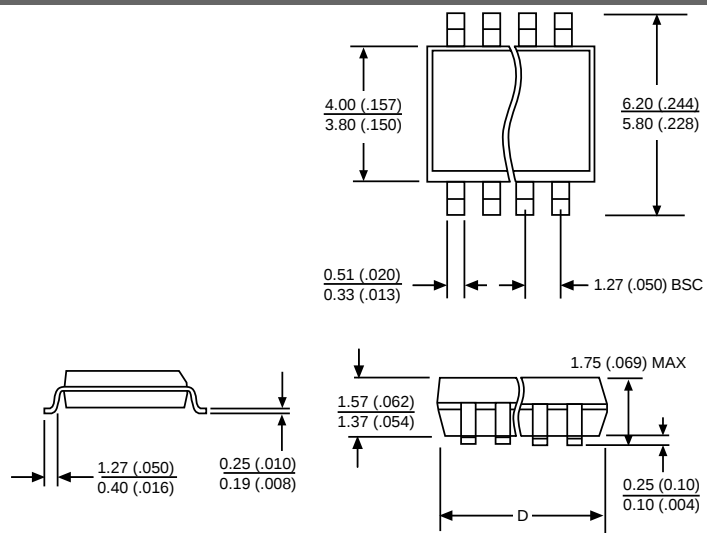
PACKAGE DIMENSIONS IN mm (INCHES)

Lead Count	D			
	Metric		English	
	Max	Min	Max	Min
8L SO Narrow	5.00	4.80	.197	.189
14L SO Narrow	8.75	8.55	.344	.337

PACKAGE THERMAL DATA

Thermal Data		8L SO Narrow	14L SO Narrow	
$R_{\theta JC}$	typ	45	30	$^{\circ}\text{C/W}$
$R_{\theta JA}$	typ	165	125	$^{\circ}\text{C/W}$

Surface Mount Narrow Body (D); 150 mil wide



REF: JEDEC MS-012

Ordering Information

Part Number	Description
CS52843ED8	8L SO Narrow
CS52843EDR8	8L SO Narrow (<i>tape & reel</i>)
CS52843ED14	14L SO Narrow
CS52843EDR14	14L SO Narrow (<i>tape & reel</i>)

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