

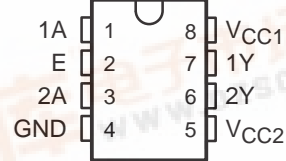
- Dual Circuits Capable of Driving High-Capacitance Loads at High Speeds
- Output Supply Voltage Range up to 24 V
- Low Standby Power Dissipation

description

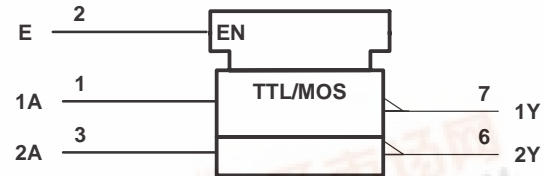
The SN75372 is a dual NAND gate interface circuit designed to drive power MOSFETs from TTL inputs. It provides high current and voltage levels necessary to drive large capacitive loads at high speeds. The device operates from a V_{CC1} of 5 V and a V_{CC2} of up to 24 V.

The SN75372 is characterized for operation from 0°C to 70°C.

D OR P PACKAGE (TOP VIEW)

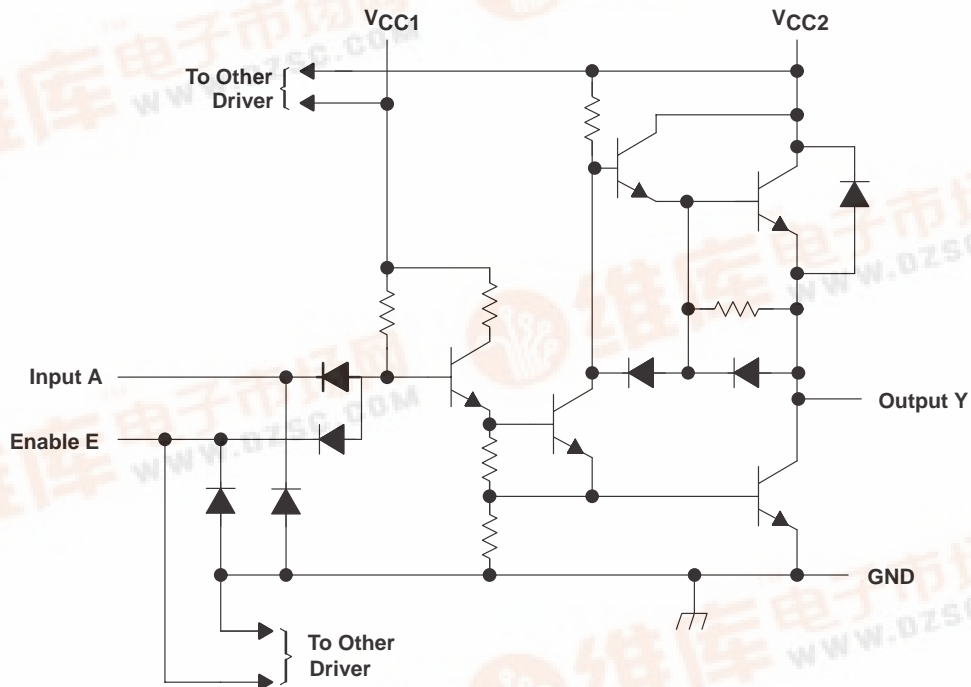


logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

schematic (each driver)



SN75372

DUAL MOSFET DRIVER

SLLS025A – JULY 1986

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC1} (see Note 1)	–0.5 V to 7 V
Supply voltage range, V_{CC2}	–0.5 V to 25 V
Input voltage, V_I	5.5 V
Peak output current, I_O ($t_w < 10$ ms, duty cycle $< 50\%$)	500 mA
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Voltage values are with respect to network GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A = 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW
P	1000 mW	8.0 mW/°C	640 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}	4.75	5	5.25	V
Supply voltage, V_{CC2}	4.75	20	24	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
High-level output current, I_{OH}			–10	mA
Low-level output current, I_{OL}			40	mA
Operating free-air temperature, T_A	0		70	°C

SN75372 DUAL MOSFET DRIVER

SLLS025A – JULY 1986

electrical characteristics over recommended ranges of V_{CC1} , V_{CC2} , and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	$I_I = -12$ mA				-1.5	V
V_{OH}	High-level output voltage	$V_{IL} = 0.8$ V,	$I_{OH} = -50$ μ A	$V_{CC2} - 1.3$	$V_{CC2} - 0.8$		V
		$V_{IL} = 0.8$ V,	$I_{OH} = -10$ mA	$V_{CC2} - 2.5$	$V_{CC2} - 1.8$		
V_{OL}	Low-level output voltage	$V_{IH} = 2$ V,	$I_{OL} = 10$ mA		0.15	0.3	V
		$V_{CC2} = 15$ V to 24 V, $I_{OL} = 40$ mA	$V_{IH} = 2$ V,		0.25	0.5	
V_F	Output clamp-diode forward voltage	$V_I = 0$,	$I_F = 20$ mA			1.5	V
I_I	Input current at maximum input voltage	$V_I = 5.5$ V				1	mA
I_{IH}	High-level input current	Any A	$V_I = 2.4$ V			40	μ A
		Any E				80	
I_{IL}	Low-level input current	Any A	$V_I = 0.4$ V		-1	-1.6	mA
		Any E			-2	-3.2	
$I_{CC1(H)}$	Supply current from V_{CC1} , both outputs high	$V_{CC1} = 5.25$ V, All inputs at 0 V,	$V_{CC2} = 24$ V, No load		2	4	mA
$I_{CC2(H)}$	Supply current from V_{CC2} , both outputs high					0.5	mA
$I_{CC1(L)}$	Supply current from V_{CC1} , both outputs low	$V_{CC1} = 5.25$ V, All inputs at 5 V,	$V_{CC2} = 24$ V, No load		16	24	mA
$I_{CC2(L)}$	Supply current from V_{CC2} , both outputs low				7	13	mA
$I_{CC2(S)}$	Supply current from V_{CC2} , standby condition	$V_{CC1} = 0$, All inputs at 5 V,	$V_{CC2} = 24$ V, No load			0.5	mA

† All typical values are at $V_{CC1} = 5$ V, $V_{CC2} = 20$ V, and $T_A = 25^\circ\text{C}$.

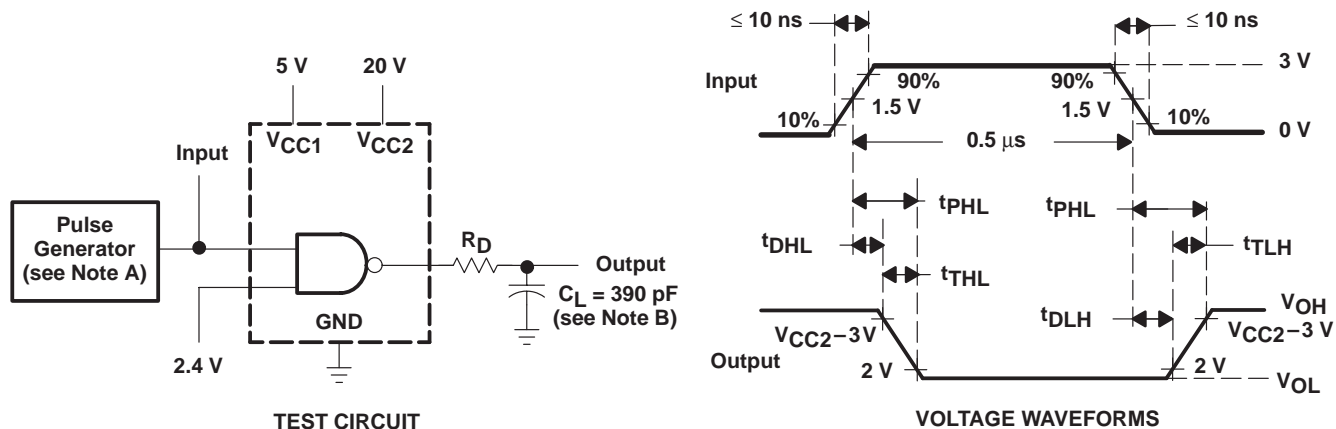
switching characteristics, $V_{CC1} = 5$ V, $V_{CC2} = 20$ V, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT	
t_{DLH}	Delay time, low-to-high-level output	$C_L = 390$ pF, $R_D = 10$ Ω , See Figure 1				20	35	ns	
t_{DHL}	Delay time, high-to-low-level output					10	20	ns	
t_{TLH}	Transition time, low-to-high-level output					20	30	ns	
t_{THL}	Transition time, high-to-low-level output					20	30	ns	
t_{PLH}	Propagation delay time, low-to-high-level output					10	40	65	ns
t_{PHL}	Propagation delay time, high-to-low-level output					10	30	50	ns

SN75372 DUAL MOSFET DRIVER

SLLS025A – JULY 1986

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_O \approx 50 \Omega$.
B. C_L includes probe and jig capacitance.

Figure 1. Test Circuit and Voltage Waveforms, Each Driver

TYPICAL CHARACTERISTICS

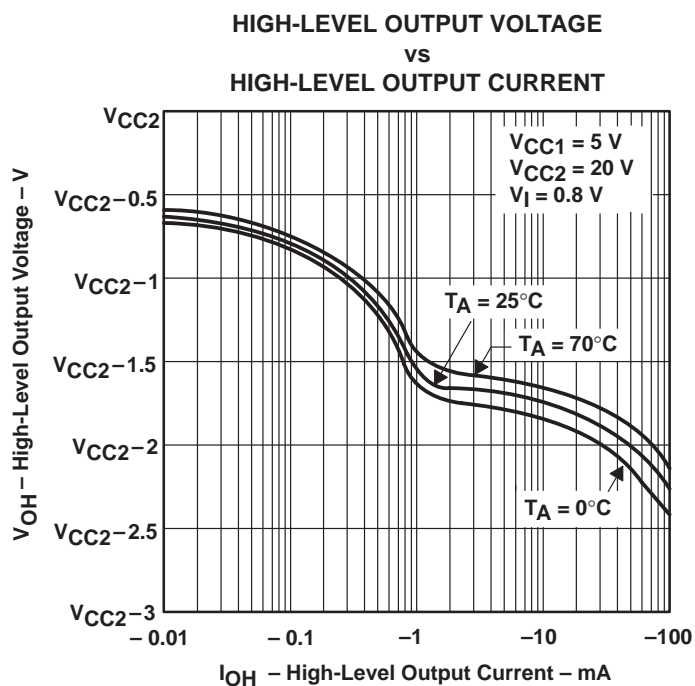


Figure 2

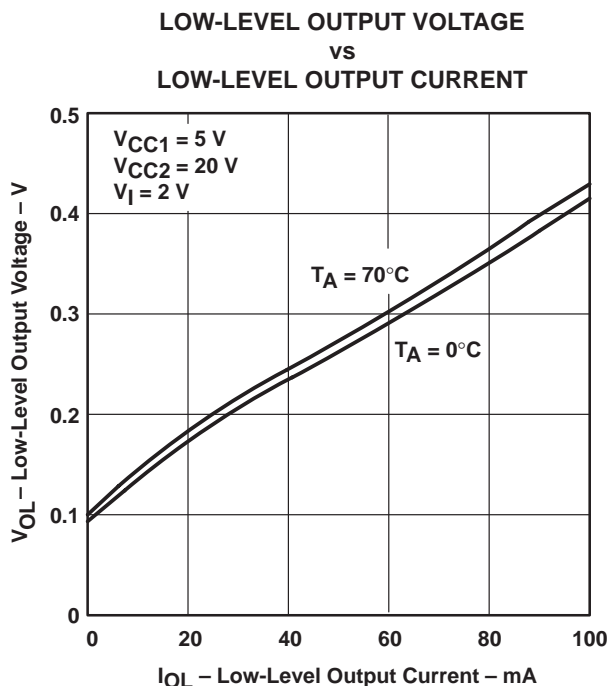


Figure 3

TYPICAL CHARACTERISTICS

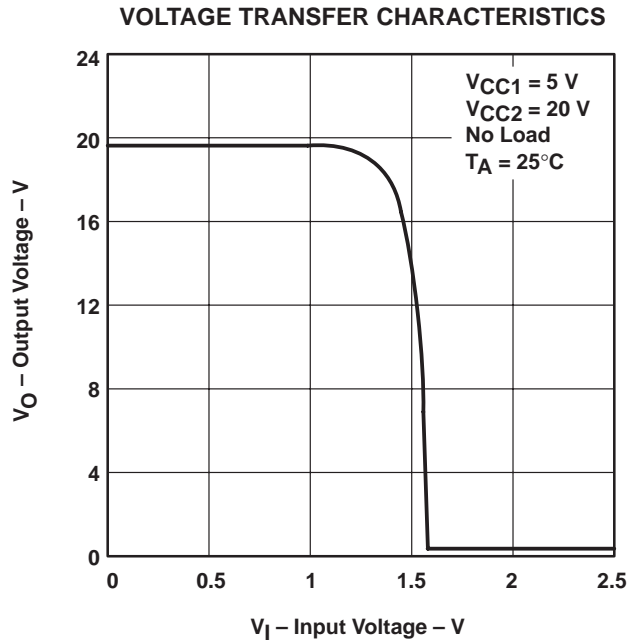


Figure 4

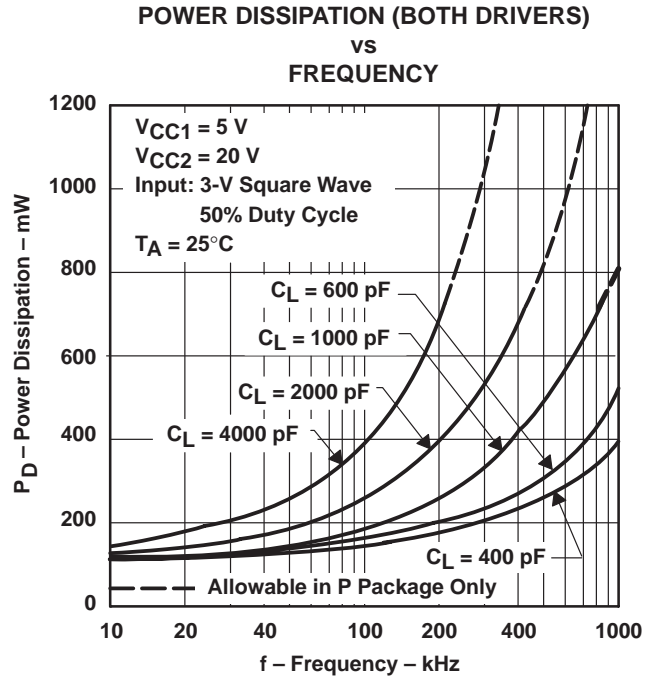


Figure 5

PROPAGATION DELAY TIME,
LOW-TO-HIGH-LEVEL OUTPUT
vs
FREE-AIR TEMPERATURE

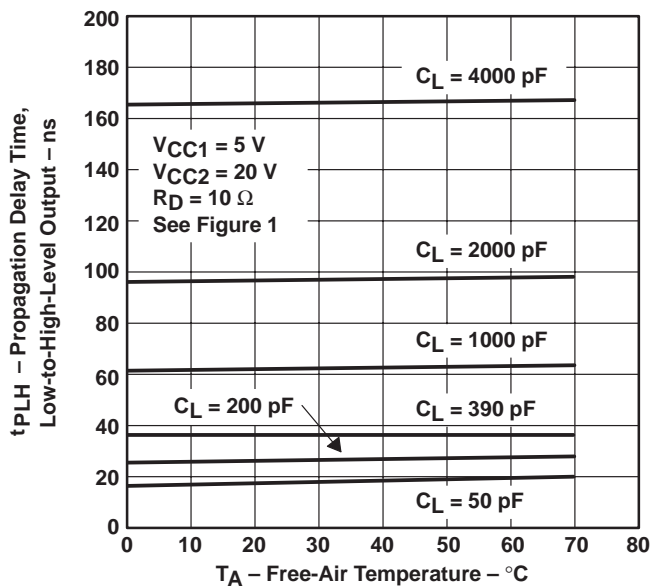


Figure 6

PROPAGATION DELAY TIME,
HIGH-TO-LOW-LEVEL OUTPUT
vs
FREE-AIR TEMPERATURE

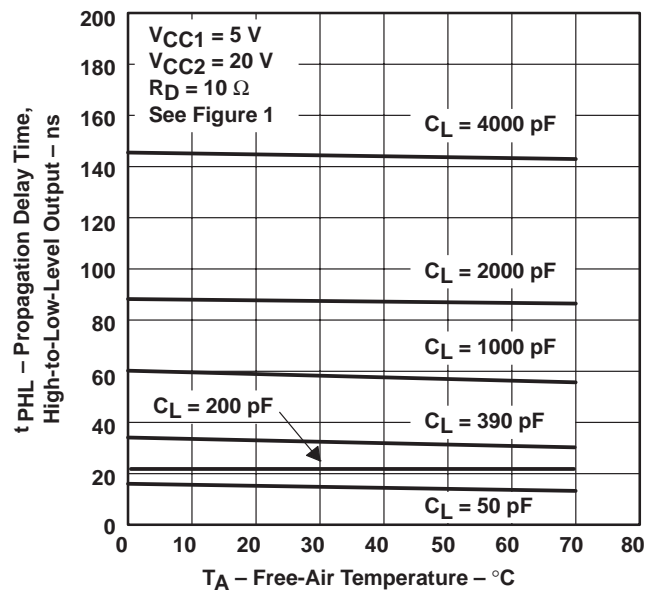
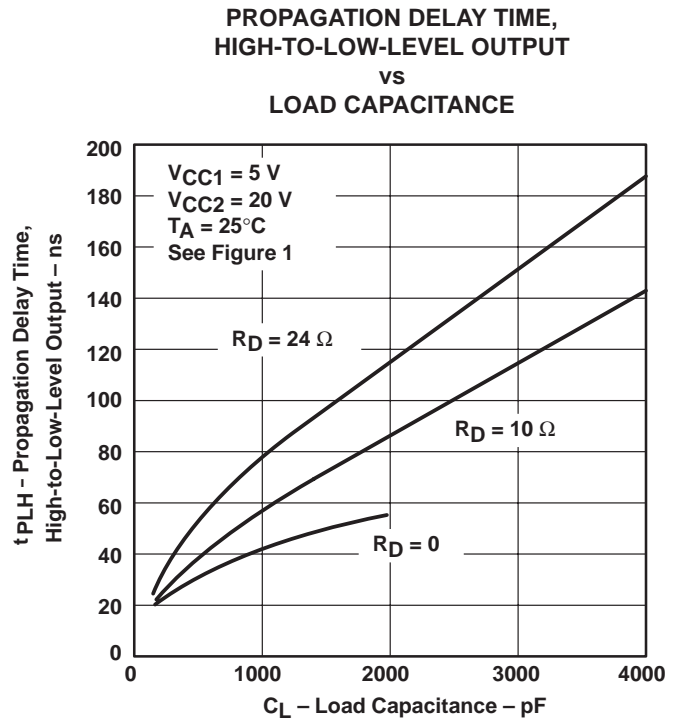
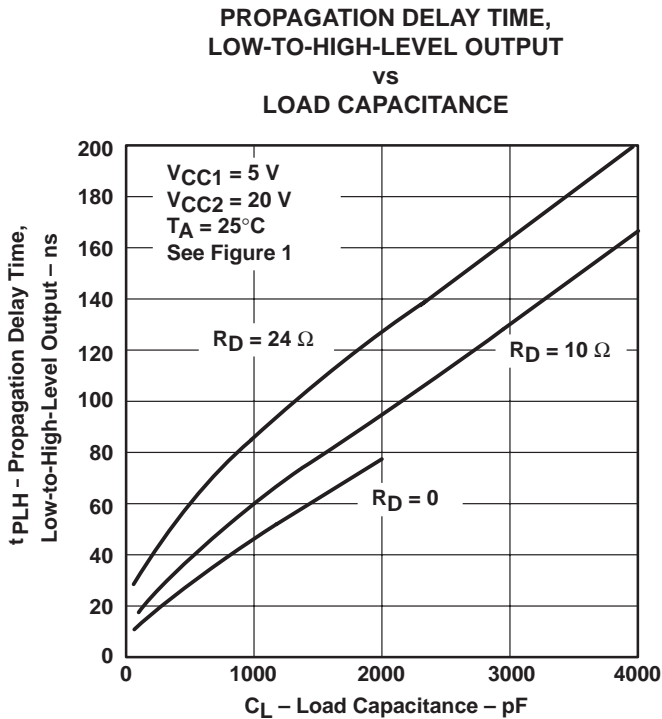
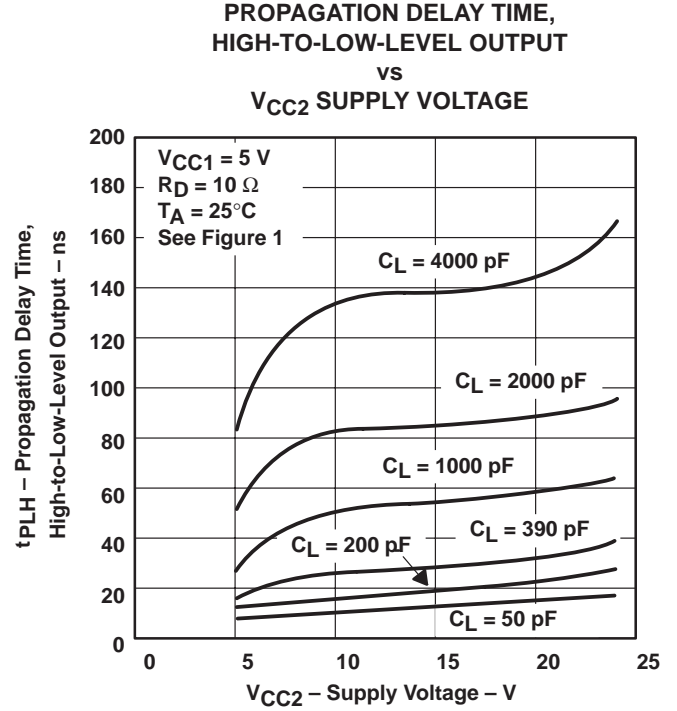
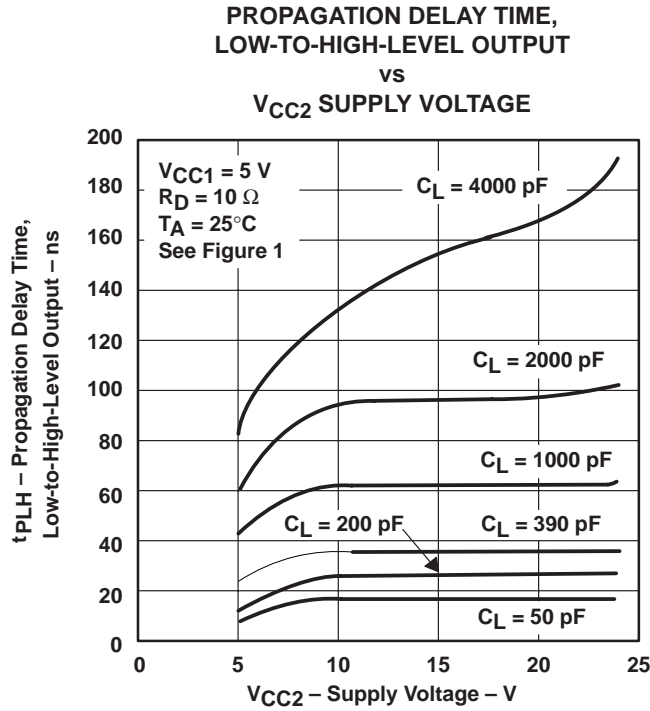


Figure 7

SN75372 DUAL MOSFET DRIVER

SLLS025A – JULY 1986

TYPICAL CHARACTERISTICS



NOTE: For $R_D = 0$, operation with $C_L > 2000$ pF violates absolute maximum current rating.

THERMAL INFORMATION

power dissipation precautions

Significant power may be dissipated in the SN75372 driver when charging and discharging high-capacitance loads over a wide voltage range at high frequencies. Figure 5 shows the power dissipated in a typical SN75372 as a function of load capacitance and frequency. Average power dissipated by this driver is derived from the equation

$$P_{T(AV)} = P_{DC(AV)} + P_{C(AV)} = P_{S(AV)}$$

where $P_{DC(AV)}$ is the steady-state power dissipation with the output high or low, $P_{C(AV)}$ is the power level during charging or discharging of the load capacitance, and $P_{S(AV)}$ is the power dissipation during switching between the low and high levels. None of these include energy transferred to the load, and all are averaged over a full cycle.

The power components per driver channel are

$$P_{DC(AV)} = \frac{P_H t_H + P_L t_L}{T}$$

$$P_{C(AV)} \approx C V_C^2 f$$

$$P_{S(AV)} = \frac{P_{LH} t_{LH} + P_{HL} t_{HL}}{T}$$

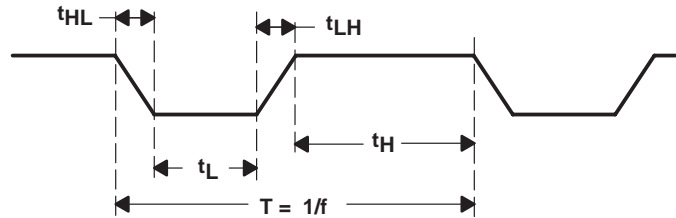


Figure 12. Output Voltage Waveform

where the times are as defined in Figure 14.

P_L , P_H , P_{LH} , and P_{HL} are the respective instantaneous levels of power dissipation, C is the load capacitance. V_C is the voltage across the load capacitance during the charge cycle shown by the equation

$$V_C = V_{OH} - V_{OL}$$

$P_{S(AV)}$ may be ignored for power calculations at low frequencies.

In the following power calculation, both channels are operating under identical conditions:

$V_{OH} = 19.2$ V and $V_{OL} = 0.15$ V with $V_{CC1} = 5$ V, $V_{CC2} = 20$ V, $V_C = 19.05$ V, $C = 1000$ pF, and the duty cycle = 60%. At 0.5 MHz, $P_{S(AV)}$ is negligible and can be ignored. When the output voltage is high, I_{CC2} is negligible and can be ignored.

On a per-channel basis using data sheet values,

$$P_{DC(AV)} = \left[(5 \text{ V}) \left(\frac{2 \text{ mA}}{2} \right) + (20 \text{ V}) \left(\frac{0 \text{ mA}}{2} \right) \right] (0.6) + \left[(5 \text{ V}) \left(\frac{16 \text{ mA}}{2} \right) + (20 \text{ V}) \left(\frac{7 \text{ mA}}{2} \right) \right] (0.4)$$

$$P_{DC(AV)} = 47 \text{ mW per channel}$$

Power during the charging time of the load capacitance is

$$P_{C(AV)} = (1000 \text{ pF}) (19.05 \text{ V})^2 (0.5 \text{ MHz}) = 182 \text{ mW per channel}$$

Total power for each driver is

$$P_{T(AV)} = 47 \text{ mW} + 182 \text{ mW} = 229 \text{ mW}$$

and total package power is

$$P_{T(AV)} = (229) (2) = 458 \text{ mW.}$$

SN75372 DUAL MOSFET DRIVER

SLLS025A – JULY 1986

APPLICATION INFORMATION

driving power MOSFETs

The drive requirements of power MOSFETs are much lower than comparable bipolar power transistors. The input impedance of a FET consists of a reverse biased PN junction that can be described as a large capacitance in parallel with a very high resistance. For this reason, the commonly used open-collector driver with a pullup resistor is not satisfactory for high-speed applications. In Figure 12(a), an IRF151 power MOSFET switching an inductive load is driven by an open-collector transistor driver with a 470- Ω pullup resistor. The input capacitance (C_{iSS}) specification for an IRF151 is 4000 pF maximum. The resulting long turn-on time due to the combination of C_{iSS} and the pullup resistor is shown in Figure 12(b).

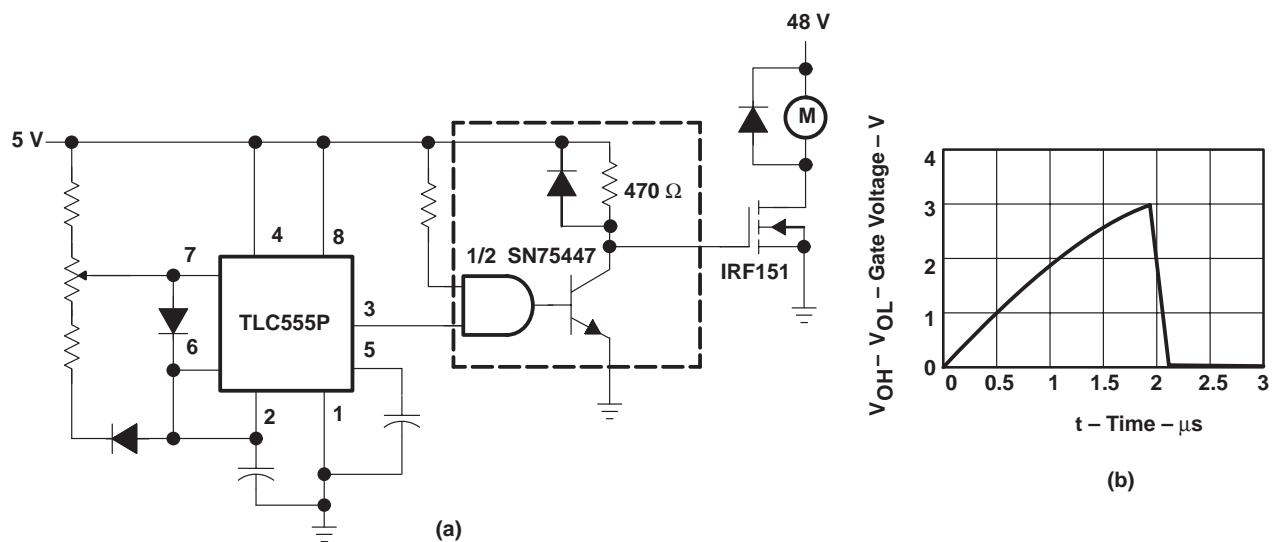


Figure 13. Power MOSFET Drive Using SN75447

APPLICATION INFORMATION

A faster, more efficient drive circuit uses an active pullup as well as an active pulldown output configuration, referred to as a totem-pole output. The SN75372 driver provides the high speed, totem-pole drive desired in an application of this type, see Figure 13(a). The resulting faster switching speeds are shown in Figure 13(b).

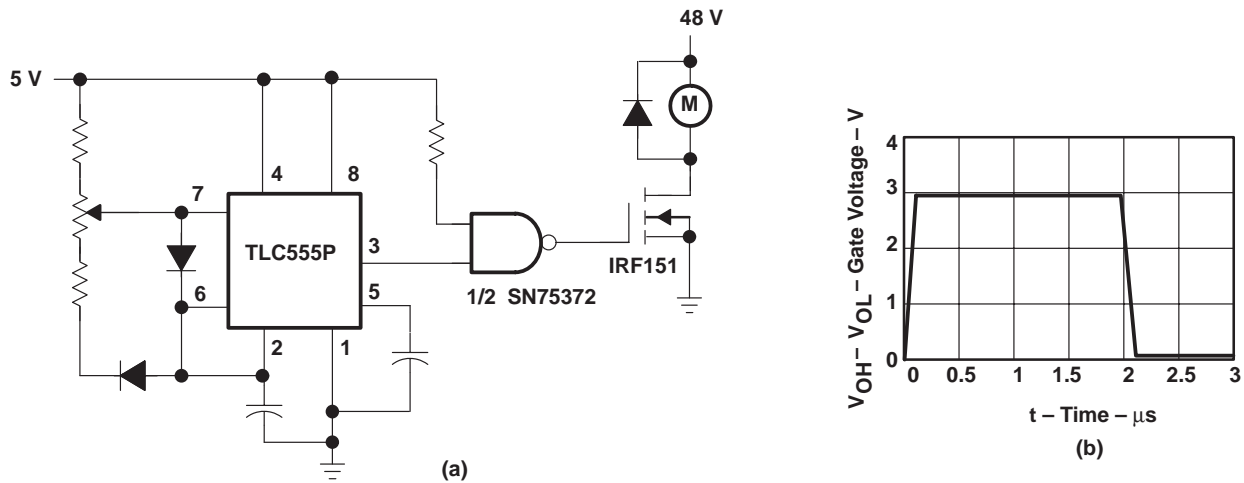


Figure 14. Power MOSFET Drive Using SN75372

Power MOSFET drivers must be capable of supplying high peak currents to achieve fast switching speeds as shown by the equation

$$I_{pk} = \frac{VC}{t_r}$$

where C is the capacitive load, and t_r is the desired drive time. V is the voltage that the capacitance is charged to. In the circuit shown in Figure 13(a), V is found by the equation

$$V = V_{OH} - V_{OL}$$

Peak current required to maintain a rise time of 100 ns in the circuit of Figure 13(a) is

$$I_{PK} = \frac{(3 - 0)4(10^{-9})}{100(10^{-9})} = 120 \text{ mA}$$

Circuit capacitance can be ignored because it is very small compared to the input capacitance of the IRF151. With a V_{CC} of 5 V, and assuming worst-case conditions, the gate drive voltage is 3 V.

For applications in which the full voltage of V_{CC2} must be supplied to the MOSFET gate, the SN75374 quad MOSFET driver should be used.

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current and complete.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.