



July 1998

54ABT244 Octal Buffer/Line Driver with TRI-STATE® Outputs

General Description

The 'ABT244 is an octal buffer and line driver with TRI-STATE outputs designed to be employed as a memory and address driver, clock driver, or bus-oriented transmitter/receiver.

Features

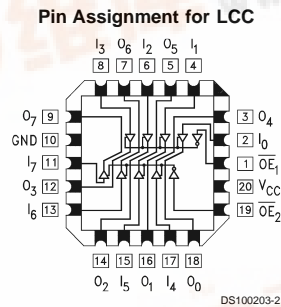
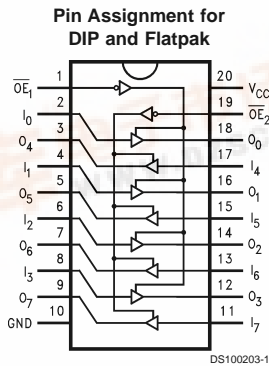
- Non-inverting buffers
- Output sink capability of 48 mA, source capability of 24 mA
- Output switching specified for both 50 pF and 250 pF loads

- Guaranteed simultaneous switching, noise level and dynamic threshold performance
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Nondestructive hot insertion capability
- Disable time less than enable time to avoid bus contention
- Standard Microcircuit Drawing (SMD) 5962-9214701

Ordering Code

Military	Package Number	Package Description
54ABT244J-QML	J20A	20-Lead Ceramic Dual-In-Line
54ABT244W-QML	W20A	20-Lead Cerpack
54ABT244E-QML	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C

Connection Diagrams



Pin Names	Description
OE ₁ , OE ₂	Output Enable Input (Active Low)
I ₀ -I ₇	Inputs
O ₀ -O ₇	Outputs

Truth Table

OE ₁	I ₀₋₃	O ₀₋₃	OE ₂	I ₄₋₇	O ₄₋₇
H	X	Z	H	X	Z
L	H	H	L	H	H
L	L	L	L	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

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54ABT244 Octal Buffer/Line Driver with TRI-STATE Outputs



Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	
Ceramic	-55°C to +175°C
V _{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Any Output	
in the Disabled or	
Power-Off State	-0.5V to 5.5V
in the HIGH State	-0.5V to V _{CC}

Current Applied to Output	
in LOW State (Max)	twice the rated I _{OL} (mA)
DC Latchup Source Current	-500 mA
Over Voltage Latchup (I/O)	10V

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	-55°C to +125°C
Supply Voltage	
Military	+4.5V to +5.5V
Minimum Input Edge Rate	(ΔV/Δt)
Data Input	50 mV/ns
Enable Input	20 mV/ns

DC Electrical Characteristics

Symbol	Parameter	ABT244			Units	V _{CC}	Conditions	
		Min	Typ	Max				
V _{IH}	Input HIGH Voltage	2.0			V		Recognized HIGH Signal	
V _{IL}	Input LOW Voltage						Recognized LOW Signal	
V _{CD}	Input Clamp Diode Voltage							
V _{OH}	Output HIGH Voltage	54ABT	2.5		V	Min	I _{IN} = -18 mA	
		54ABT	2.0		V	Min	I _{OH} = -24 mA	
V _{OL}	Output LOW Voltage	54ABT	0.55		V	Min	I _{OL} = 48 mA	
I _{IH}	Input HIGH Current				5	μA	Max	V _{IN} = 2.7V (Note 4)
					5	μA	Max	V _{IN} = V _{CC}
I _{BVI}	Input HIGH Current Breakdown Test				7	μA	Max	V _{IN} = 7.0V
I _{IL}	Input LOW Current				-5	μA	Max	V _{IN} = 0.5V (Note 4)
					-5	μA	Max	V _{IN} = 0.0V
V _{ID}	Input Leakage Test	4.75				V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded
I _{OZH}	Output Leakage Current				50	μA	0 - 5.5V	V _{OUT} = 2.7V; $\overline{OE}_n = 2.0V$
I _{OZL}	Output Leakage Current				-50	μA	0 - 5.5V	V _{OUT} = 0.5V; $\overline{OE}_n = 2.0V$
I _{OS}	Output Short-Circuit Current	-100	-275		mA	Max	V _{OUT} = 0.0V	
I _{CEX}	Output High Leakage Current				50	μA	Max	V _{OUT} = V _{CC}
I _{ZZ}	Bus Drainage Test				100	μA	0.0	V _{OUT} = 5.5V; All Others GND
I _{CCH}	Power Supply Current				50	μA	Max	All Outputs HIGH
I _{CCL}	Power Supply Current				30	mA	Max	All Outputs LOW
I _{CCZ}	Power Supply Current				50	μA	Max	$\overline{OE}_n = V_{CC}$; All Others at V _{CC} or Ground
I _{CC1}	Additional I _{CC} /Input	Outputs Enabled	2.5		mA	Max	V _I = V _{CC} - 2.1V	
		Outputs TRI-STATE	2.5		mA		Enable Input V _I = V _{CC} - 2.1V	
		Outputs TRI-STATE	50		μA		Data Input V _I = V _{CC} - 2.1V All Others at V _{CC} or Ground	
I _{CCD}	Dynamic I _{CC}	No Load			0.1	mA/ MHz	Max	Outputs Open $\overline{OE}_n = GND$, (Note 3) One Bit Toggling, 50% Duty Cycle

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Note 3: For 8 bits toggling, I_{CCD} < 0.8 mA/MHz.

Note 4: Guaranteed, but not tested.

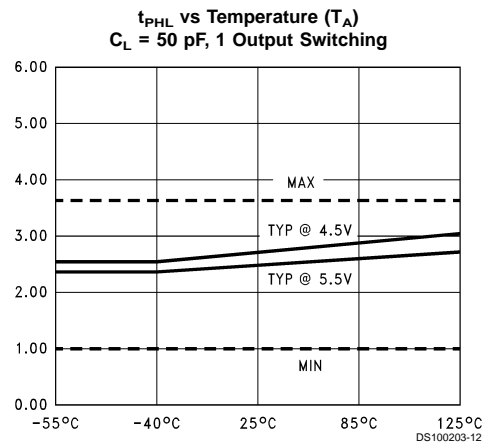
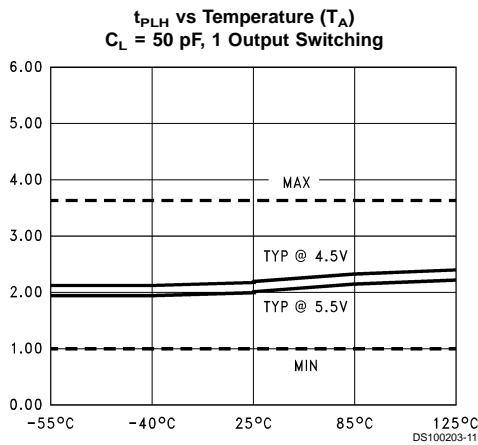
AC Electrical Characteristics

Symbol	Parameter	54ABT		Units	Fig. No.
		$T_A = -55^\circ\text{C to }+125^\circ\text{C}$ $V_{CC} = 4.5\text{V}-5.5\text{V}$ $C_L = 50\text{ pF}$			
		Min	Max		
t_{PLH}	Propagation Delay	1.0	5.3	ns	Figure 5
t_{PHL}	Data to Outputs	1.0	5.0		
t_{PZH}	Output Enable	0.8	6.5	ns	Figure 4
t_{PZL}	Time	1.2	7.9		
t_{PHZ}	Output Disable	1.2	7.6	ns	Figure 4
t_{PLZ}	Time	1.0	7.9		

Capacitance

Symbol	Parameter	Typ	Units	Conditions $T_A = 25^\circ\text{C}$
C_{IN}	Input Capacitance	5.0	pF	$V_{CC} = 0\text{V}$
C_{OUT} (Note 5)	Output Capacitance	9.0	pF	$V_{CC} = 5.0\text{V}$

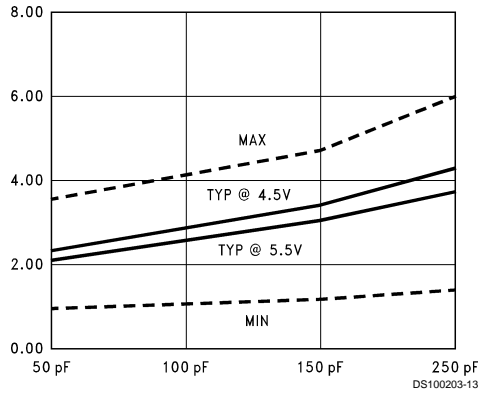
Note 5: C_{OUT} is measured at frequency $f = 1\text{ MHz}$, per MIL-STD-883B, Method 3012.



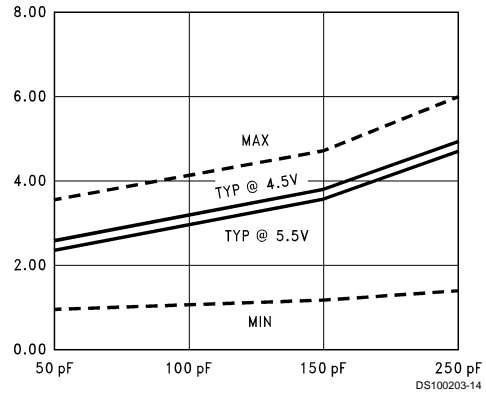
Dashed lines represent design characteristics; for specified guarantees refer to AC Characteristics Table.

Capacitance (Continued)

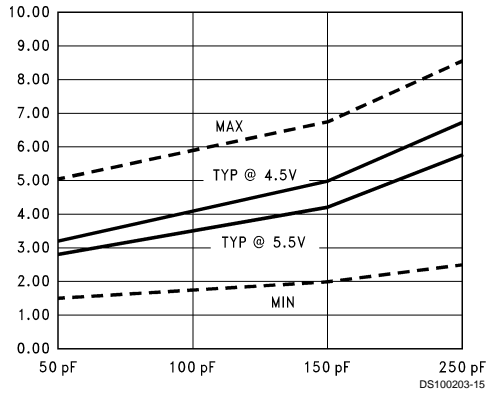
t_{PLH} vs Load Capacitance
1 Output Switching, $T_A = 25^\circ\text{C}$



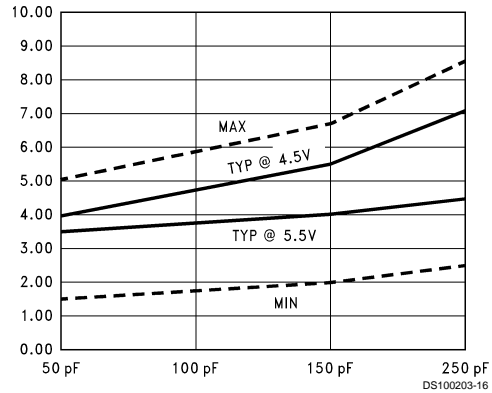
t_{PHL} vs Load Capacitance
1 Output Switching, $T_A = 25^\circ\text{C}$



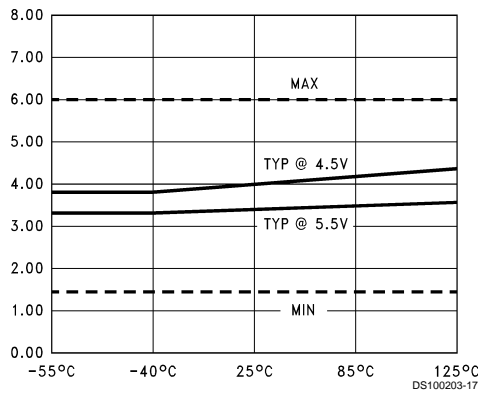
t_{PLH} vs Load Capacitance
8 Outputs Switching, $T_A = 25^\circ\text{C}$



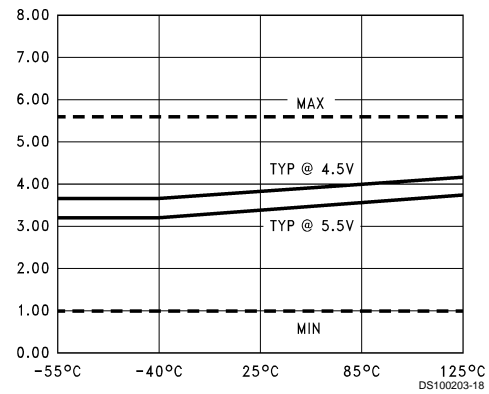
t_{PHL} vs Load Capacitance
8 Outputs Switching, $T_A = 25^\circ\text{C}$



t_{PLZ} vs Temperature (T_A)
 $C_L = 50$ pF, 1 Output Switching



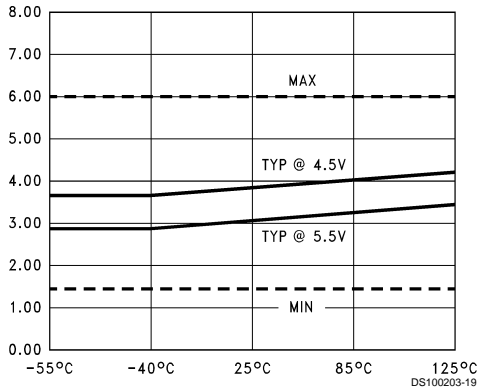
t_{PLZ} vs Temperature (T_A)
 $C_L = 50$ pF, 1 Output Switching



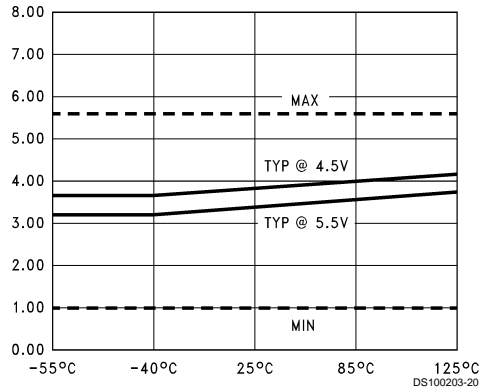
Dashed lines represent design characteristics; for specified guarantees refer to AC Characteristics Table.

Capacitance (Continued)

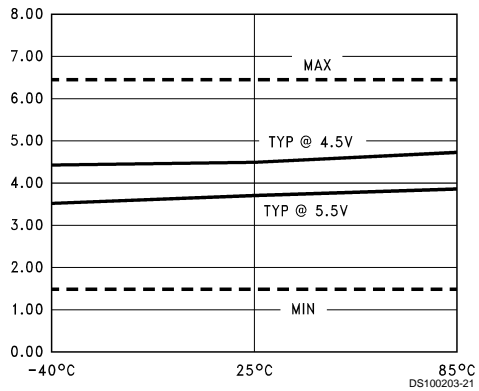
t_{PZH} vs Temperature (T_A)
 $C_L = 50$ pF, 1 Output Switching



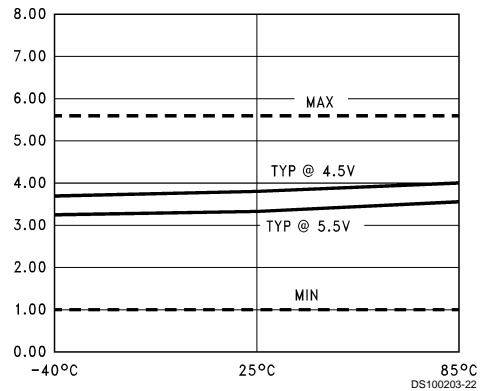
t_{PHZ} vs Temperature (T_A)
 $C_L = 50$ pF, 1 Output Switching



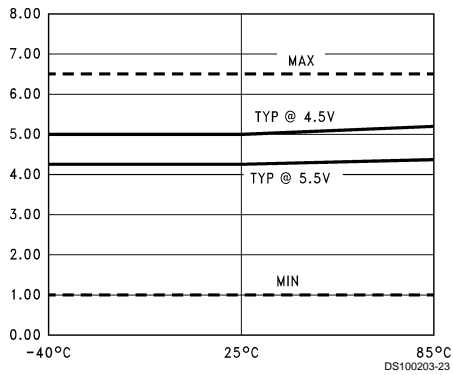
t_{PZH} vs Temperature (T_A)
 $C_L = 50$ pF, 8 Outputs Switching



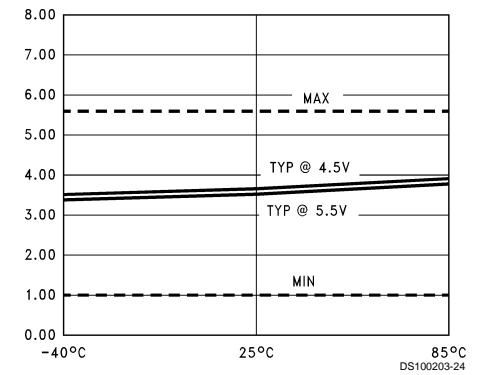
t_{PHZ} vs Temperature (T_A)
 $C_L = 50$ pF, 8 Outputs Switching



t_{PZL} vs Temperature (T_A)
 $C_L = 50$ pF, 8 Outputs Switching



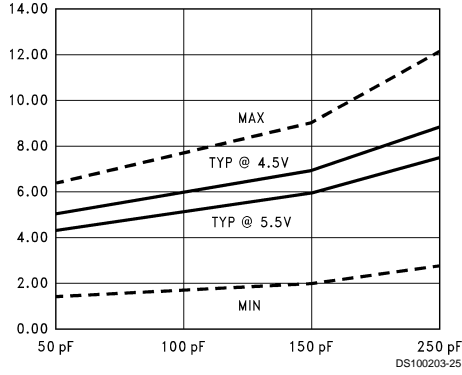
t_{PLZ} vs Temperature (T_A)
 $C_L = 50$ pF, 8 Outputs Switching



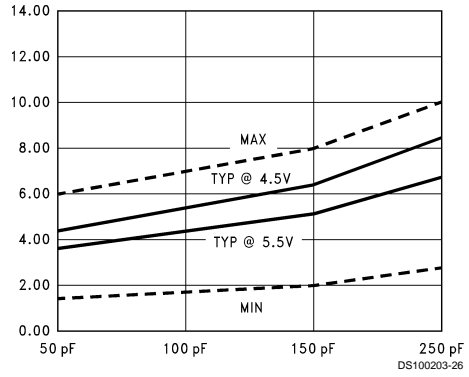
Dashed lines represent design characteristics; for specified guarantees refer to AC Characteristics Table.

Capacitance (Continued)

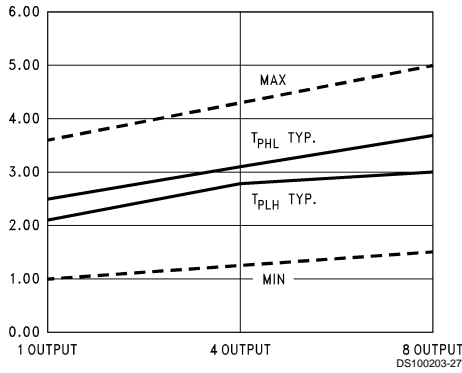
t_{PZL} vs Load Capacitance
8 Outputs Switching
 $T_A = 25^\circ\text{C}$



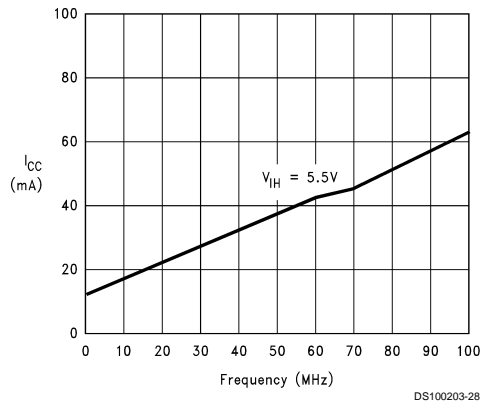
t_{PZH} vs Load Capacitance
8 Outputs Switching
 $T_A = 25^\circ\text{C}$



t_{PLH} and t_{PHL} vs Number
Outputs Switching $V_{CC} = 5.0\text{V}$,
 $T_A = 25^\circ\text{C}$, $C_L = 50\text{ pF}$

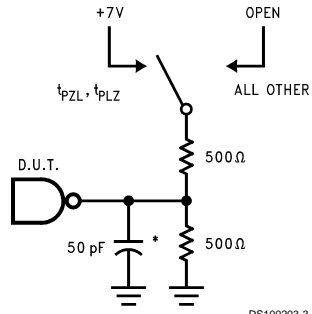


I_{CC} vs Frequency,
Average, $T_A = 25^\circ\text{C}$,
All Outputs Unloaded/Unterminated



Dashed lines represent design characteristics; for specified guarantees refer to AC Characteristics Table.

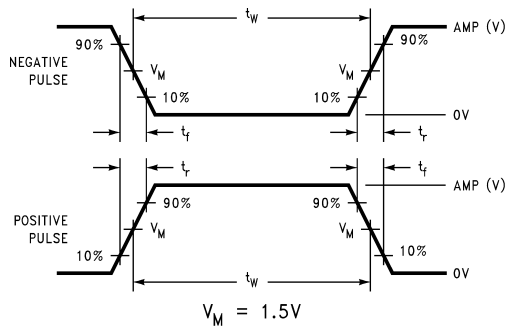
AC Loading



DS100203-3

*Includes jig and probe capacitance

FIGURE 1. Standard AC Test Load



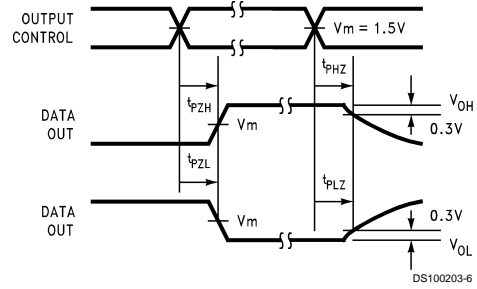
DS100203-5

FIGURE 2. Test Input Signal Levels

Amplitude	Rep. Rate	t_w	t_r	t_f
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

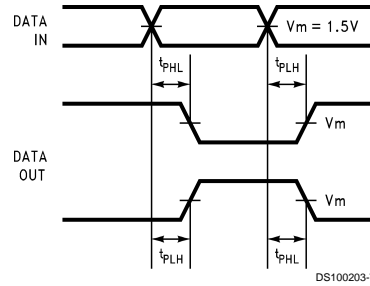
FIGURE 3. Test Input Signal Requirements

AC Waveforms



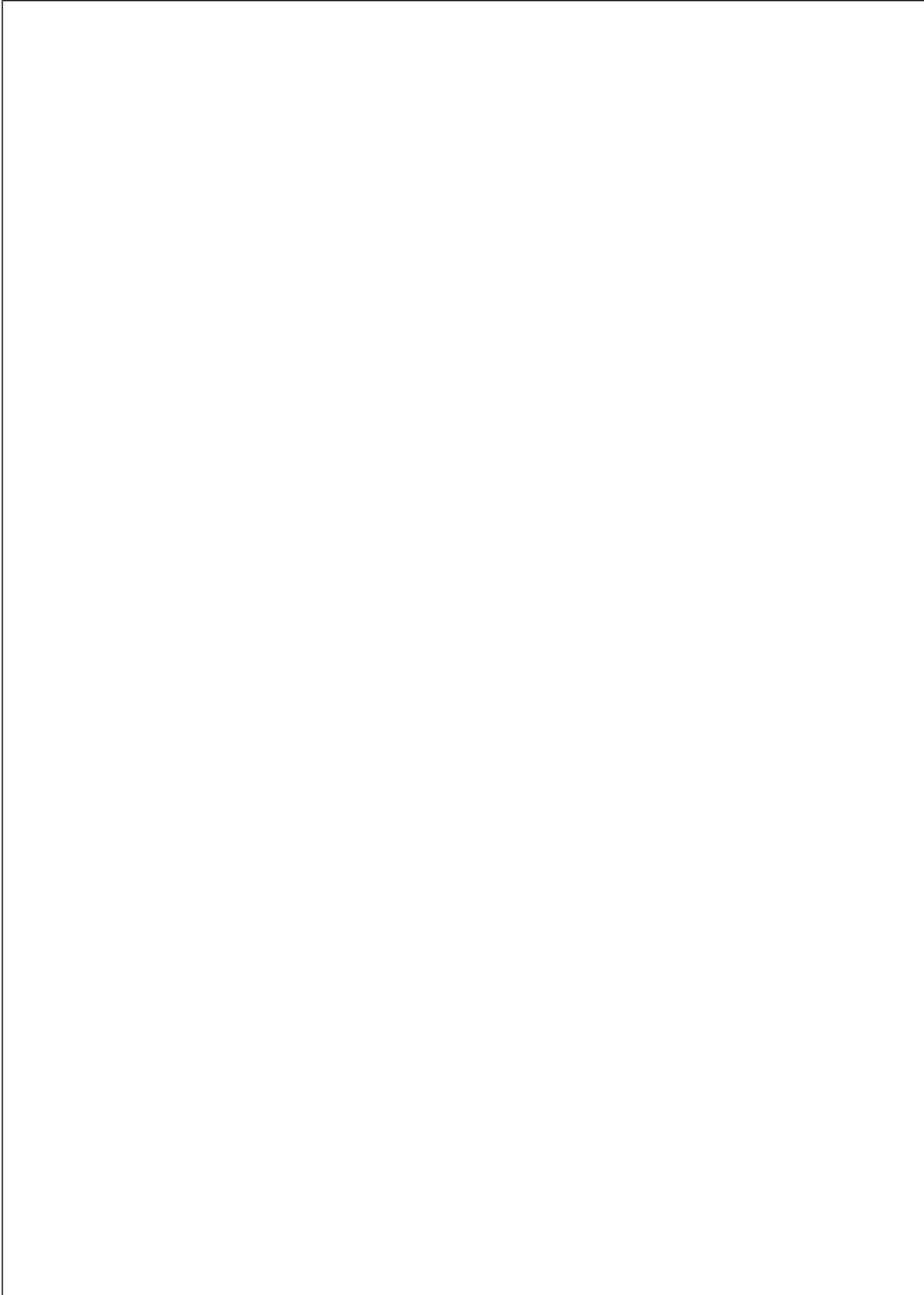
DS100203-6

FIGURE 4. TRI-STATE Output HIGH and LOW Enable and Disable Times

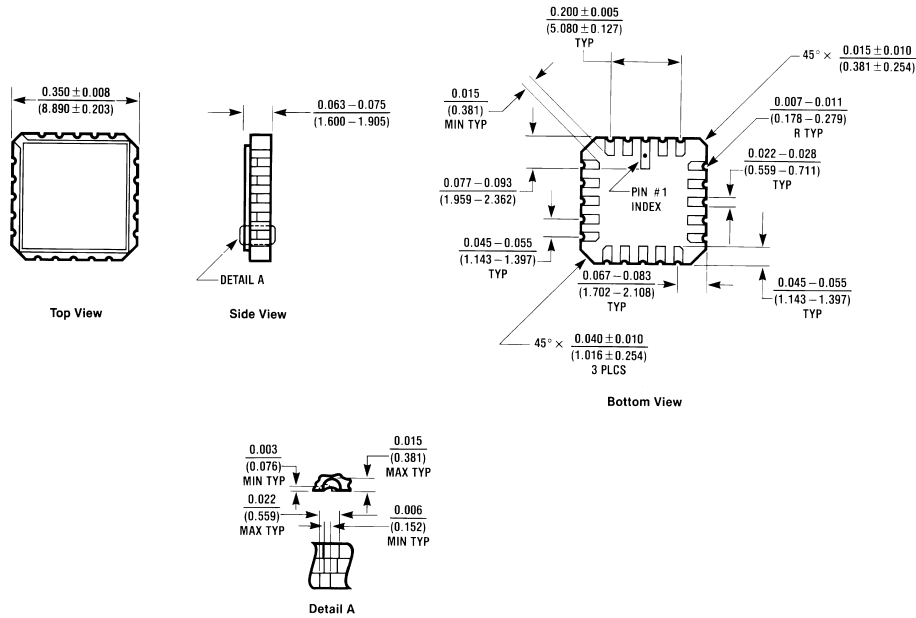


DS100203-7

FIGURE 5. Propagation Delay Waveforms for Inverting and Non-Inverting Functions

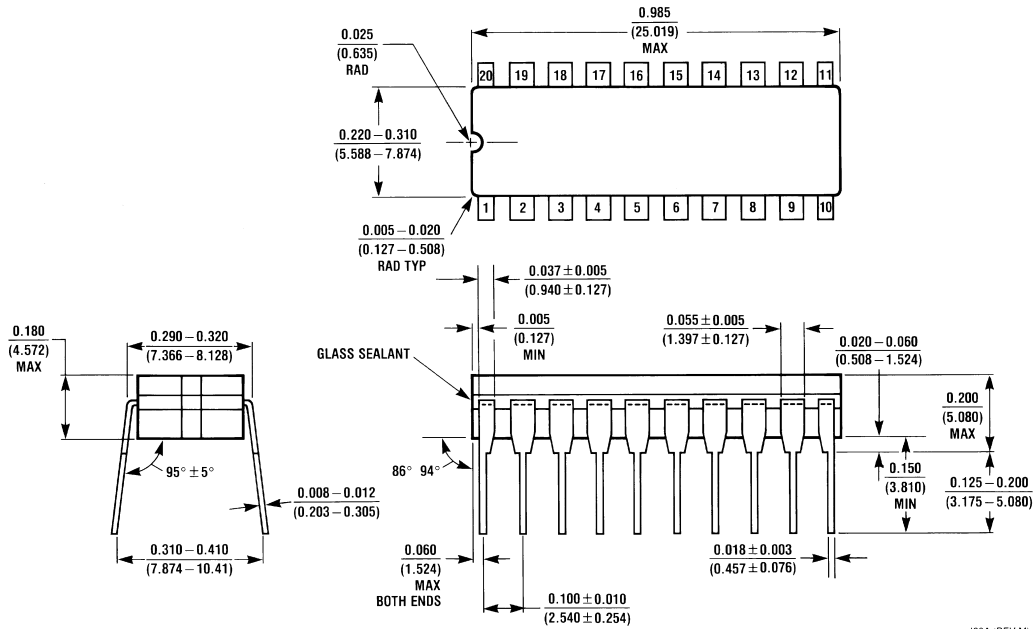


Physical Dimensions inches (millimeters) unless otherwise noted



E20A (REV D)

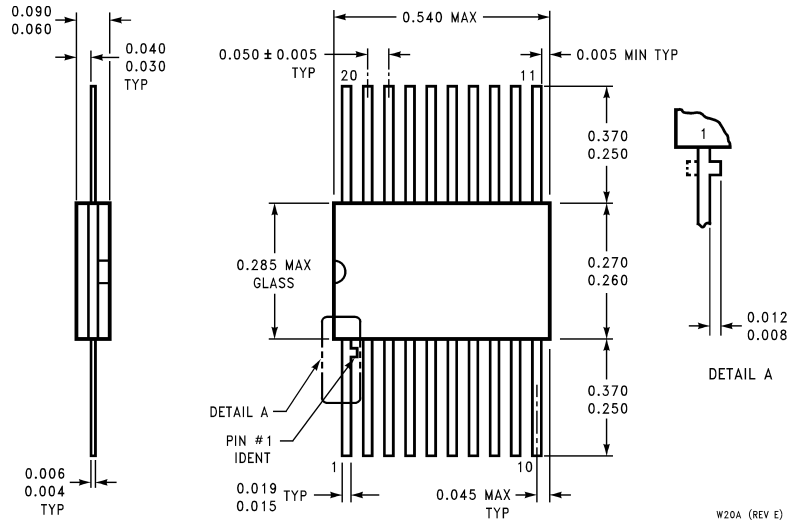
20-Terminal Ceramic Chip Carrier (L)
NS Package Number E20A



J20A (REV M)

20-Lead Ceramic Dual-In-Line (D)
NS Package Number J20A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**20-Lead Ceramic Flatpak (F)
NS Package Number W20A**

W20A (REV E)

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