



July 1998

54ABT245 Octal Bidirectional Transceiver with TRI-STATE® Outputs

General Description

The 'ABT245 contains eight non-inverting bidirectional buffers with TRI-STATE outputs and is intended for bus-oriented applications. Current sinking capability is 48 mA on both the A and B ports. The Transmit/Receive (T/R) input determines the direction of data flow through the bidirectional transceiver. Transmit (active HIGH) enables data from A ports to B ports; Receive (active LOW) enables data from B ports to A ports. The Output Enable input, when HIGH, disables both A and B ports by placing them in a High Z condition.

- Guaranteed output skew
- Guaranteed multiple output switching specifications
- Output switching specified for both 50 pF and 250 pF loads
- Guaranteed simultaneous switching, noise level and dynamic threshold performance
- Guaranteed latchup protection
- High impedance glitch-free bus loading during entire power up and power down cycle
- Non-destructive hot insertion capability
- Disable time is less than enable time to avoid bus contention
- Standard Microcircuit Drawing (SMD) 5962-9214801

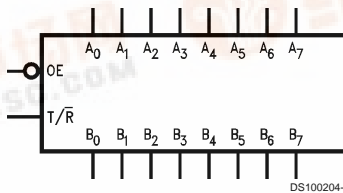
Features

- Bidirectional non-inverting buffers
- A and B output sink capability of 48 mA, source capability of 24 mA

Ordering Code:

Military	Package Number	Package Description
54ABT245J-QML	J20A	20-Lead Ceramic Dual-In-Line
54ABT245W-QML	W20A	20-Lead Cerpak
54ABT245E-QML	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C

Logic Symbol



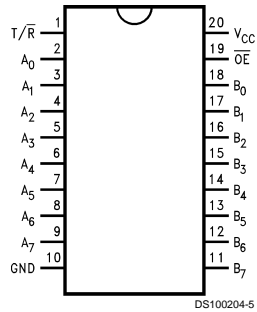
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54ABT245 Octal Bidirectional Transceiver with TRI-STATE Outputs



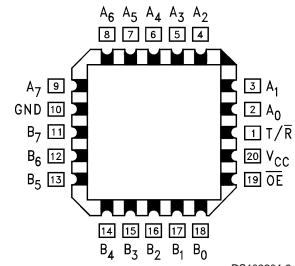
Connection Diagrams

Pin Assignment for DIP and Flatpak.



DS100204-5

Pin Assignment for LCC



DS100204-3

Pin Descriptions

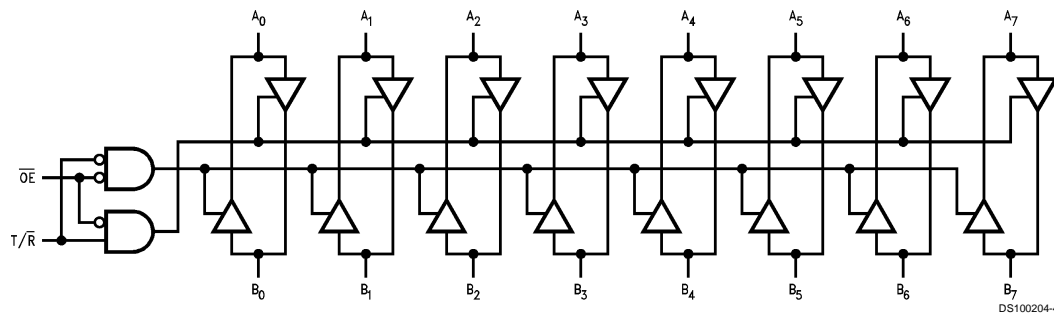
Pin Names	Description
\overline{OE}	Output Enable Input (Active LOW)
T/\overline{R}	Transmit/Receive Input
A_0 – A_7	Side A Inputs or TRI-STATE Outputs
B_0 – B_7	Side B Inputs or TRI-STATE Outputs

Truth Table

Inputs		Output
\overline{OE}	T/\overline{R}	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High Z State

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram



DS100204-4

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	
Ceramic	-55°C to +175°C
V _{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Any Output in the Disabled or Power-off State	-0.5V to 5.5V
in the HIGH State	-0.5V to V _{CC}
Current Applied to Output	

in LOW State (Max)	twice the rated I _{OL} (mA)
DC Latchup Source Current	-500 mA
Over Voltage Latchup (I/O)	10V

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	-55°C to +125°C
Supply Voltage	
Military	+4.5V to +5.5V
Minimum Input Edge Rate	(ΔV/Δt)
Data Input	50 mV/ns
Enable Input	20 mV/ns

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter		ABT245			Units	V _{CC}	Conditions	
			Min	Typ	Max				
V _{IH}	Input HIGH Voltage		2.0			V		Recognized HIGH Signal	
V _{IL}	Input LOW Voltage					0.8	V	Recognized LOW Signal	
V _{CD}	Input Clamp Diode Voltage					-1.2	V	Min	
V _{OH}	Output HIGH Voltage	54ABT	2.5			V	Min	I _{IN} = -18 mA (\overline{OE} , T/ \overline{R})	
		54ABT	2.0			V	Min	I _{OH} = -3 mA (A _n , B _n) I _{OH} = -24 mA (A _n , B _n)	
V _{OL}	Output LOW Voltage	54ABT				0.55	V	Min	
I _{IH}	Input HIGH Current					5	μA	Max	V _{IN} = 2.7V (\overline{OE} , T/ \overline{R}) (Note 3) V _{IN} = V _{CC} (\overline{OE} , T/ \overline{R})
						5			
I _{BVI}	Input HIGH Current Breakdown Test					7	μA	Max	V _{IN} = 7.0V (\overline{OE} , T/ \overline{R})
I _{BVIT}	Input HIGH Current Breakdown Test (I/O)					100	μA	Max	V _{IN} = 5.5V (A _n , B _n)
I _{IL}	Input LOW Current					-5	μA	Max	V _{IN} = 0.5V (\overline{OE} , T/ \overline{R}) (Note 3) V _{IN} = 0.0V (\overline{OE} , T/ \overline{R})
						-5			
V _{ID}	Input Leakage Test		4.75				V	0.0	I _{ID} = 1.9 μA (\overline{OE} , T/ \overline{R}) All Other Pins Grounded
I _{IH} + I _{OZH}	Output Leakage Current					50	μA	0 - 5.5V	V _{OUT} = 2.7V (A _n , B _n); \overline{OE} = 2.0V
I _{IL} + I _{OZL}	Output Leakage Current					-50	μA	0 - 5.5V	V _{OUT} = 0.5V (A _n , B _n); \overline{OE} = 2.0V
I _{OS}	Output Short-Circuit Current		-100	-275			mA	Max	V _{OUT} = 0.0V (A _n , B _n)
I _{CEX}	Output High Leakage Current					50	μA	Max	V _{OUT} = V _{CC} (A _n , B _n)
I _{ZZ}	Bus Drainage Test					100	μA	0.0	V _{OUT} = 5.5V (A _n , B _n); All Others GND
I _{CCH}	Power Supply Current					50	μA	Max	All Outputs HIGH
I _{CCL}	Power Supply Current					30	mA	Max	All Outputs LOW
I _{CCZ}	Power Supply Current					50	μA	Max	\overline{OE} = V _{CC} , T/ \overline{R} = GND or V _{CC} ; All Other GND or V _{CC}
I _{CCT}	Additional I _{CC} /Input	Outputs Enabled	2.5			mA	Max		V _I = V _{CC} - 2.1V \overline{OE} , T/ \overline{R} V _I = V _{CC} - 2.1V Data Input V _I = V _{CC} - 2.1V All Others at V _{CC} or GND.
		Outputs TRI-STATE	2.5			mA			
		Outputs TRI-STATE	50			μA			

DC Electrical Characteristics (Continued)

Symbol	Parameter	ABT245			Units	V _{CC}	Conditions
		Min	Typ	Max			
I _{CCD}	Dynamic I _{CC} No Load (Note 3)			0.1	mA/ MHz	Max	Outputs Open $\overline{OE} = \text{GND}$, $T/\overline{R} = \text{GND}$ or V_{CC} One Bit Toggling, 50% Duty Cycle (Note 4)

Note 3: Guaranteed but not tested.

Note 4: For 8 bits toggling, I_{CCD} < 0.8 mA/MHz.

DC Electrical Characteristics

Symbol	Parameter	Min	Max	Units	V _{CC}	Conditions
						C _L = 50 pF, R _L = 500Ω
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}		1.1	V	5.0	T _A = 25°C (Note 5)
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}		-0.45	V	5.0	T _A = 25°C (Note 5)

Note 5: Max number of outputs defined as (n), n – 1 data inputs are driven 0V to 3V. One output at LOW.

AC Electrical Characteristics

Symbol	Parameter	54ABT		Units
		T _A = -55°C to +125°C V _{CC} = 4.5V–5.5V C _L = 50 pF		
		Min	Max	
t _{PLH}	Propagation Delay	1.0	4.8	ns
t _{PHL}	Data to Outputs	1.0	4.8	
t _{PZH}	Output Enable	1.0	6.7	ns
t _{PZL}	Time	2.0	7.5	
t _{PHZ}	Output Disable	1.7	7.4	ns
t _{PLZ}	Time	1.7	6.5	

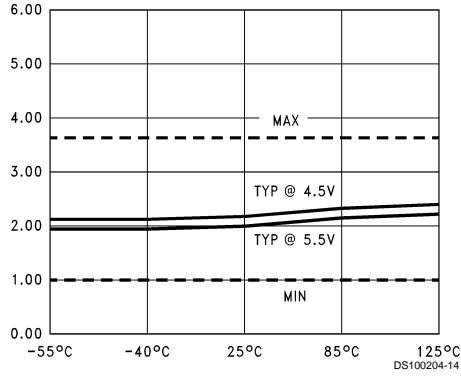
Capacitance

Symbol	Parameter	Typ	Units	Conditions
C _{IN}	Input Capacitance	5.0	pF	T _A = 25°C V _{CC} = 0V (\overline{OE} , T/ \overline{R})
C _{I/O} (Note 6)	I/O Capacitance	11.0	pF	V _{CC} = 5.0V (A _n , B _n)

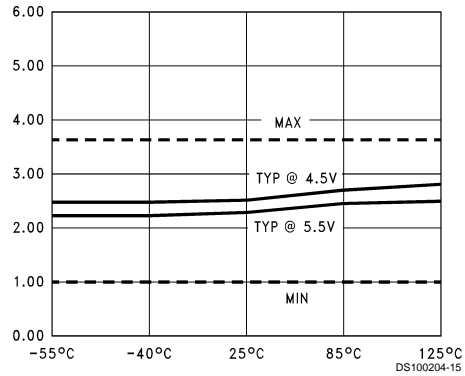
Note 6: C_{I/O} is measured at frequency f = 1 MHz, per MIL-STD-883B, Method 3012.

Capacitance (Continued)

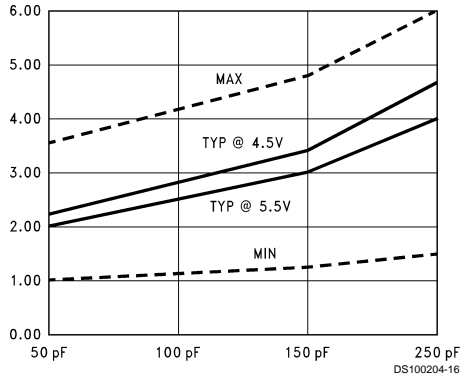
t_{PLH} vs Temperature (T_A)
 $C_L = 50$ pF, 1 Output Switching



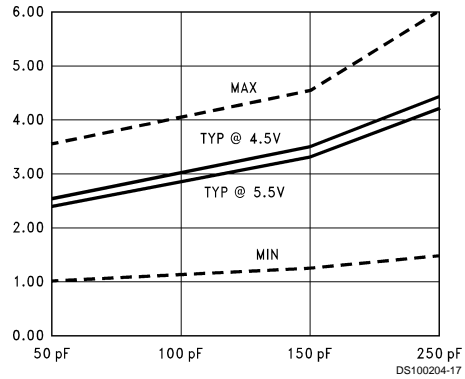
t_{PHL} vs Temperature (T_A)
 $C_L = 50$ pF, 1 Output Switching



t_{PLH} vs Load Capacitance
 1 Output Switching, $T_A = 25^\circ\text{C}$

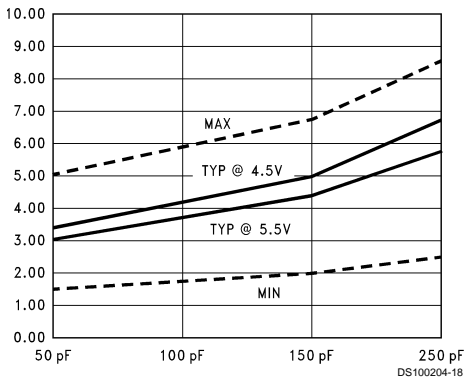


t_{PHL} vs Load Capacitance
 1 Output Switching, $T_A = 25^\circ\text{C}$

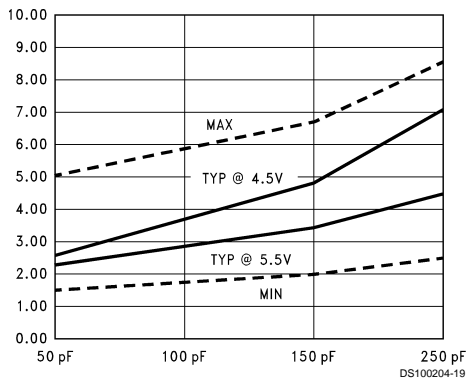


Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Table.

t_{PLH} vs Load Capacitance
 8 Outputs Switching, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$

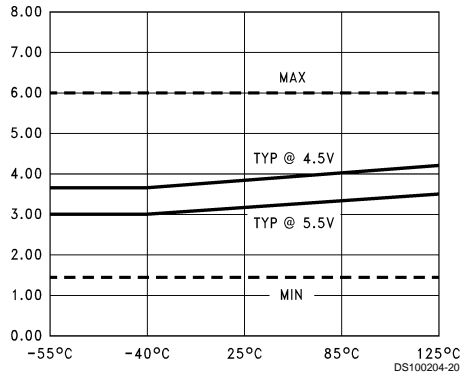


t_{PHL} vs Load Capacitance
 8 Outputs Switching, $T_A = 25^\circ\text{C}$

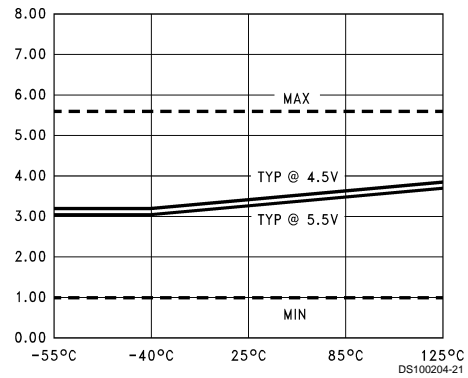


Capacitance (Continued)

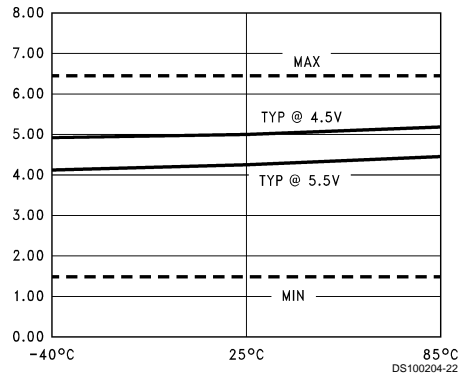
t_{PZL} vs Temperature (T_A)
 $C_L = 50$ pF, 1 Output Switching



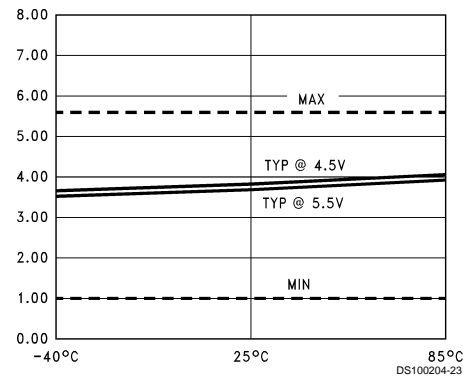
t_{PLZ} vs Temperature (T_A)
 $C_L = 50$ pF, 1 Output Switching



t_{PZL} vs Temperature (T_A)
 $C_L = 50$ pF, 8 Outputs Switching

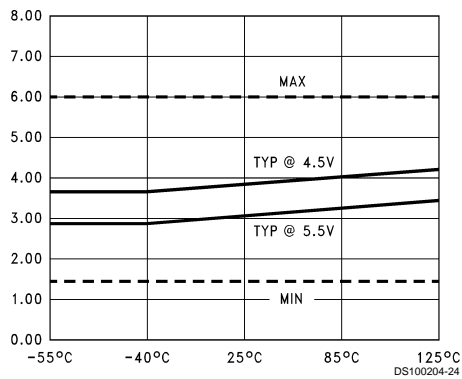


t_{PLZ} vs Temperature (T_A)
 $C_L = 50$ pF, 8 Outputs Switching

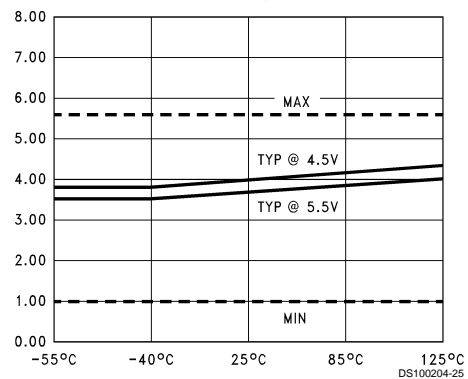


Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Table.

t_{PZH} vs Temperature (T_A)
 $C_L = 50$ pF, 1 Output Switching

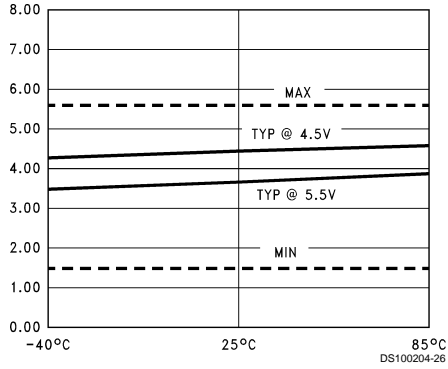


t_{PHZ} vs Temperature (T_A)
 $C_L = 50$ pF, 1 Output Switching

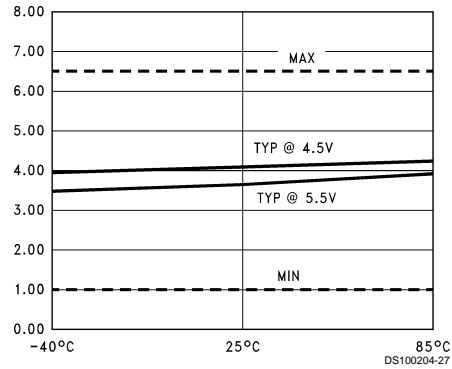


Capacitance (Continued)

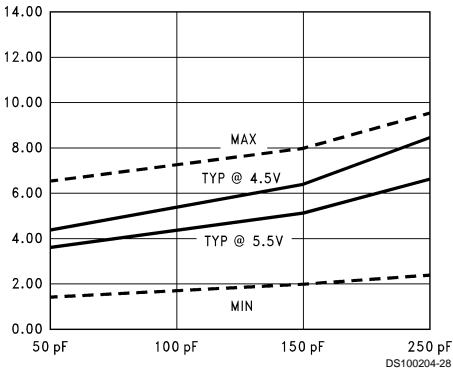
t_{PZH} vs Temperature (T_A)
 $C_L = 50$ pF, 8 Outputs Switching



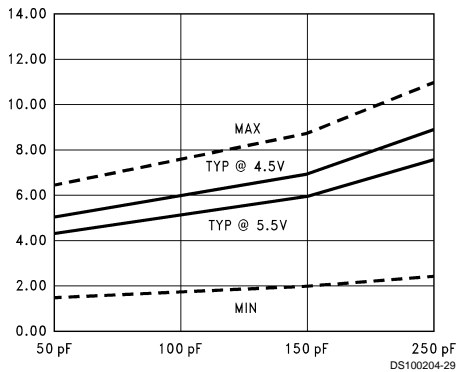
t_{PHZ} vs Temperature (T_A)
 $C_L = 50$ pF, 8 Outputs Switching



t_{PZH} vs Load Capacitance
 8 Outputs Switching, $T_A = 25^\circ\text{C}$

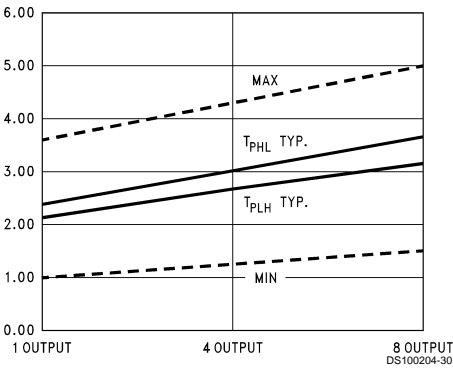


t_{PZL} vs Load Capacitance
 8 Outputs Switching, $T_A = 25^\circ\text{C}$

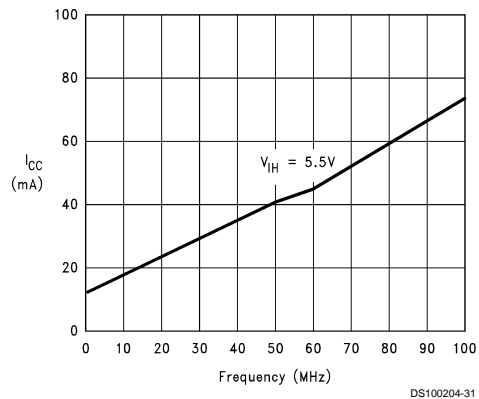


Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Table.

t_{PLH} and t_{PHL} vs Number Outputs Switching
 $V_{CC} = 5.0\text{V}$, $T_A = 25^\circ\text{C}$, $C_L = 50$ pF

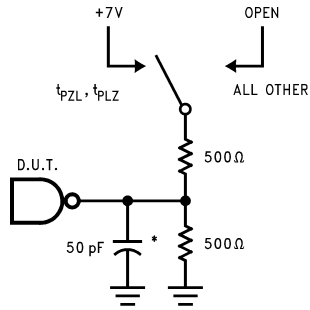


**I_{CC} vs Frequency, Average, $T_A = 25^\circ\text{C}$,
 All Outputs Unloaded/Unterminated**



Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Table.

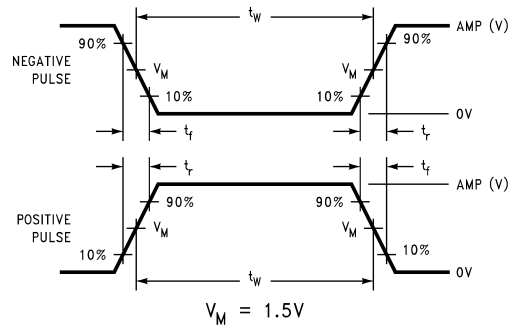
AC Loading



DS100204-6

*Includes jig and probe capacitance

FIGURE 1. Standard AC Test Load



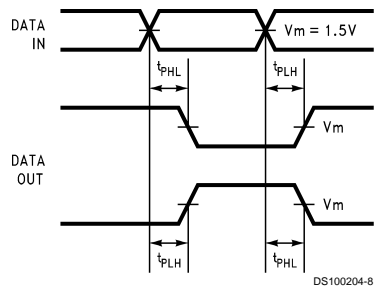
DS100204-7

FIGURE 2. Test Input Signal Levels

Amplitude	Rep. Rate	t_w	t_r	t_f
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

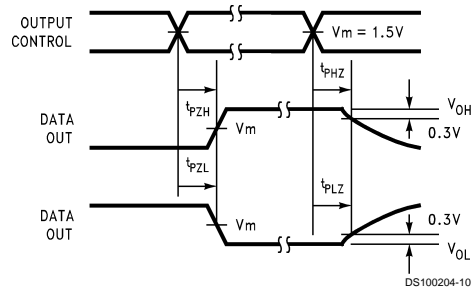
FIGURE 3. Test Input Signal Requirements

AC Waveforms



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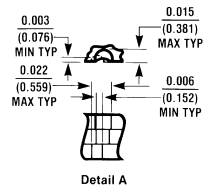
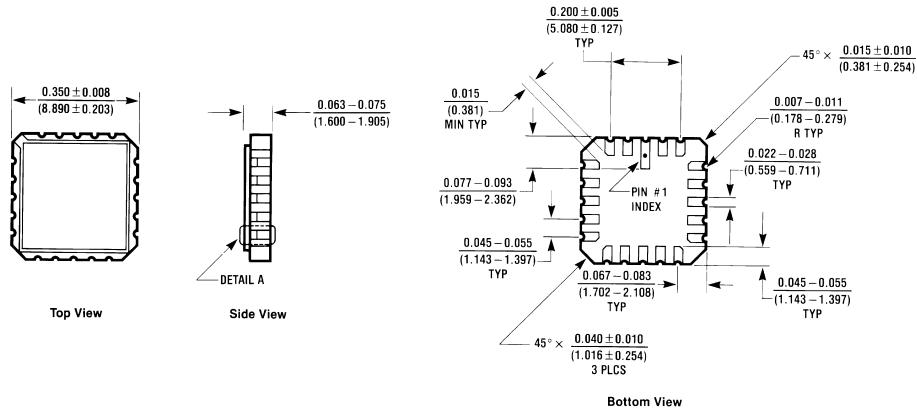
FIGURE 4. Propagation Delay Waveforms for Inverting and Non-Inverting Functions



DS100204-10

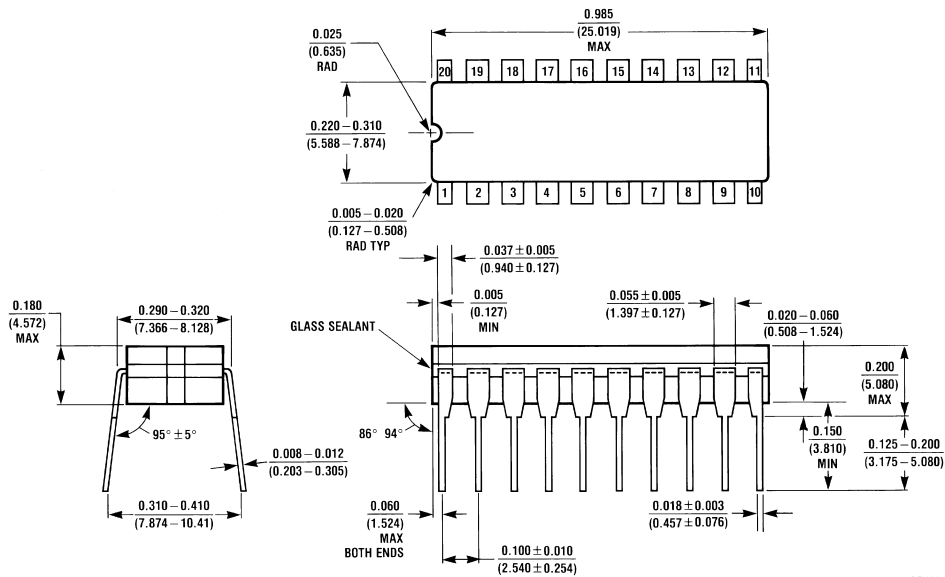
FIGURE 5. TRI-STATE Output HIGH and LOW Enable and Disable Times

Physical Dimensions inches (millimeters) unless otherwise noted



E20A (REV D)

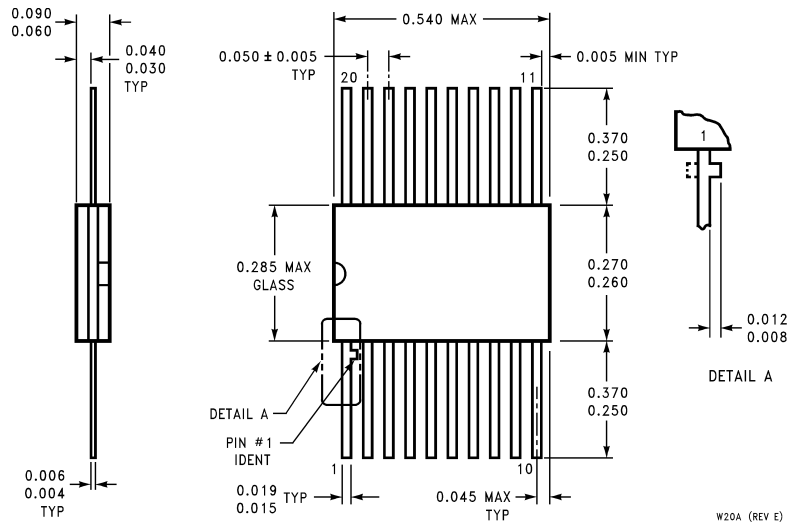
20-Terminal Ceramic Chip Carrier (L)
NS Package Number E20A



J20A (REV M)

20-Lead Ceramic Dual-In-Line Package (D)
NS Package Number J20A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**20-Lead Ceramic Flatpak (F)
NS Package Number W20A**

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