



November 1994

54F/74F174 Hex D Flip-Flop with Master Reset

General Description

The 'F174 is a high-speed hex D flip-flop. The device is used primarily as a 6-bit edge-triggered storage register. The information on the D inputs is transferred to storage during the LOW-to-HIGH clock transition. The device has a Master Reset to simultaneously clear all flip-flops.

Features

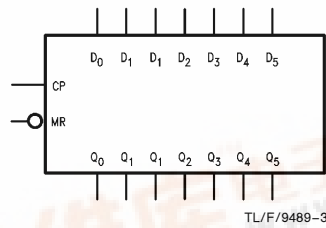
- Edge-triggered D-type inputs
- Buffered positive edge-triggered clock
- Asynchronous common reset
- Guaranteed 4000V minimum ESD protection

Commercial	Military	Package Number	Package Description
74F174PC		N16E	16-Lead (0.300" Wide) Molded Dual-In-Line
	54F174DM (Note 2)	J16A	16-Lead Ceramic Dual-In-Line
74F174SC (Note 1)		M16A	16-Lead (0.150" Wide) Molded Small Outline, JEDEC
74F174SJ (Note 1)		M16D	16-Lead (0.300" Wide) Molded Small Outline, EIAJ
	54F174FM (Note 2)	W16A	16-Lead Cerpack
	54F174LM (Note 2)	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C

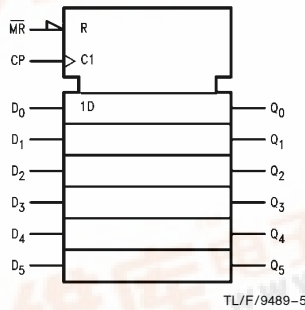
Note 1: Devices also available in 13" reel. Use Suffix = SCX and SJX.

Note 2: Military grade device with environmental and burn-in processing. Use suffix = DMQB, FMQB and LMQB.

Logic Symbols

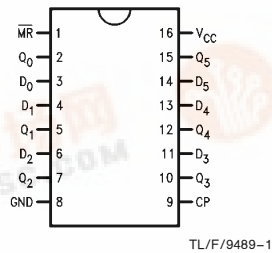


IEEE/IEC

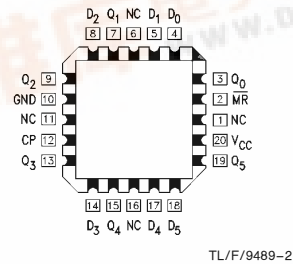


Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



Pin Assignment for LCC



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54F/74F174 Hex D Flip-Flop with Master Reset





Unit Loading/Fan Out

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I _{IH} /I _{IL} Output I _{OH} /I _{OL}
D ₀ -D ₅	Data Inputs	1.0/1.0	20 μA/ -0.6 mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 μA/ -0.6 mA
\overline{MR}	Master Reset Input (Active LOW)	1.0/1.0	20 μA/ -0.6 mA
Q ₀ -Q ₅	Outputs	50/33.3	-1 mA/20 mA

Functional Description

The 'F174 consists of six edge-triggered D flip-flops with individual D inputs and Q outputs. The Clock (CP) and Master Reset (\overline{MR}) are common to all flip-flops. Each D input's state is transferred to the corresponding flip-flop's output following the LOW-to-HIGH Clock (CP) transition. A LOW input to the Master Reset (\overline{MR}) will force all outputs LOW independent of Clock or Data inputs. The 'F174 is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

Truth Table

Inputs			Outputs
\overline{MR}	CP	D _n	Q _n
L	X	X	L
H		H	H
H		L	L

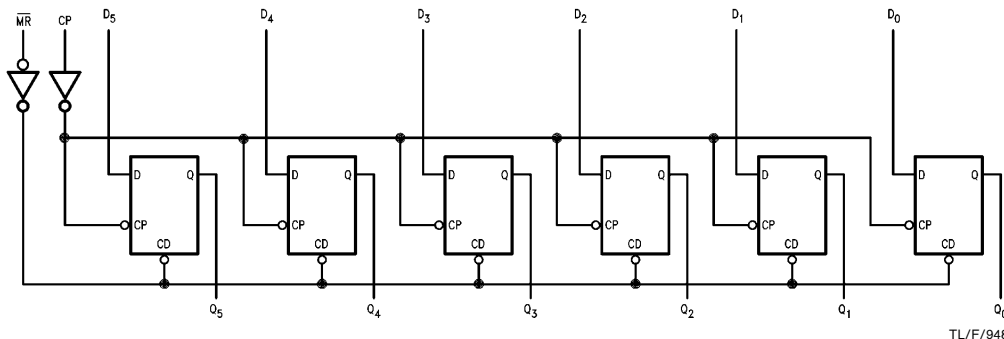
H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

 = LOW-to-HIGH Clock Transition

Logic Diagram



TL/F/9489-4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
Plastic	-55°C to +150°C
V _{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V _{CC} = 0V)	
Standard Output	-0.5V to V _{CC}
TRI-STATE® Output	-0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I _{OL} (mA)
ESD Last Passing Voltage (Min)	4000V


Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	-55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter		54F/74F			Units	V _{CC}	Conditions
			Min	Typ	Max			
V _{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage					V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage					V	Min	I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	54F 10% V _{CC} 74F 10% V _{CC} 74F 5% V _{CC}	2.5 2.5 2.7			V	Min	I _{OH} = -1 mA I _{OH} = -1 mA I _{OH} = -1 mA
V _{OL}	Output LOW Voltage	54F 10% V _{CC} 74F 10% V _{CC}	0.5 0.5			V	Min	I _{OL} = 20 mA I _{OL} = 20 mA
I _{IH}	Input HIGH Current	54F 74F	20.0 5.0			μA	Max	V _{IN} = 2.7V
I _{BVI}	Input HIGH Current Breakdown Test	54F 74F	100 7.0			μA	Max	V _{IN} = 7.0V
I _{CEX}	Output HIGH Leakage Current	54F 74F	250 50			μA	Max	V _{OUT} = V _{CC}
V _{ID}	Input Leakage Test	74F	4.75			V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded
I _{OD}	Output Leakage Circuit Current	74F	3.75			μA	0.0	V _{ID} = 150 mV All Other Pins Grounded
I _{IL}	Input LOW Current		-0.6			mA	Max	V _{IN} = 0.5V
I _{OS}	Output Short-Circuit Current		-60 -150			mA	Max	V _{OUT} = 0V
I _{CCH}	Power Supply Current		30 45			mA	Max	CP =  D _n = $\overline{\text{MR}}$ = HIGH
I _{CCL}	Power Supply Current		30 45			mA	Max	V _O = LOW

AC Electrical Characteristics

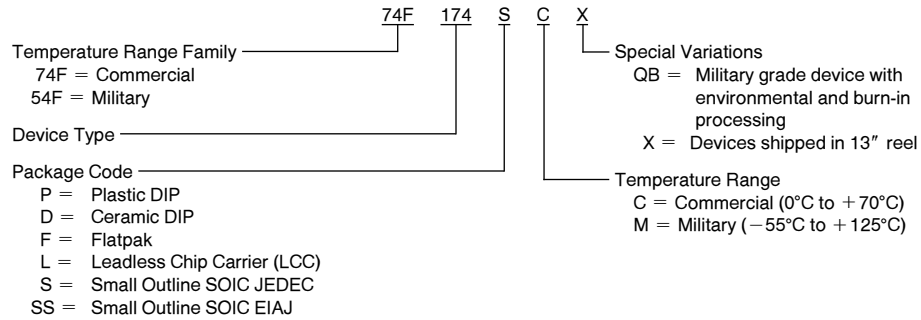
Symbol	Parameter	74F			54F		74F		Units
		T _A = +25°C V _{CC} = +5.0V C _L = 50 pF			T _A , V _{CC} = Mil C _L = 50 pF		T _A , V _{CC} = Com C _L = 50 pF		
		Min	Typ	Max	Min	Max	Min	Max	
f _{max}	Maximum Clock Frequency	80			70		80		MHz
t _{PLH} t _{PHL}	Propagation Delay CP to Q _n	3.5 4.0	5.5 7.0	8.0 10.0	3.0 4.0	10.0 12.0	3.5 4.0	9.0 11.0	ns
t _{PHL}	Propagation Delay \overline{MR} to Q _n	5.0	10.0	14.0	5.0	16.0	5.0	15.0	ns

AC Operating Requirements

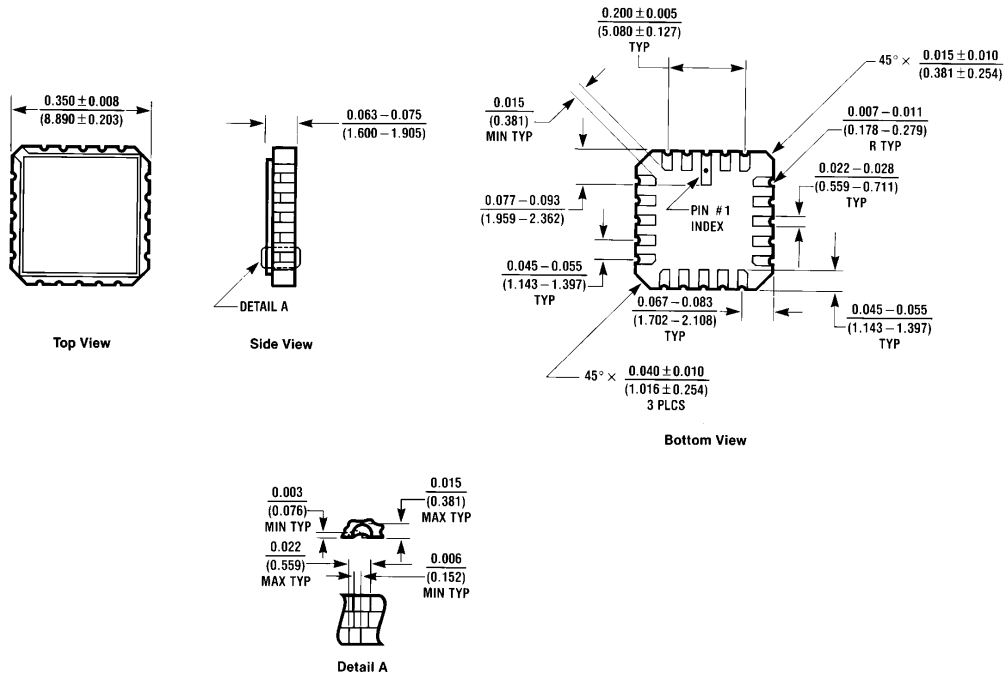
Symbol	Parameter	74F		54F		74F		Units
		T _A = +25°C V _{CC} = +5.0V		T _A , V _{CC} = Mil		T _A , V _{CC} = Com		
		Min	Max	Min	Max	Min	Max	
t _s (H) t _s (L)	Setup Time, HIGH or LOW D _n to CP	4.8 4.0		5.0 5.0		4.8 4.0		ns
t _h (H) t _h (L)	Hold Time, HIGH or LOW D _n to CP	0 0		2.0 2.0		0 0		ns
t _w (H) t _w (L)	CP Pulse Width HIGH or LOW	4.0 6.0		5.0 7.5		4.0 6.0		ns
t _w (L)	\overline{MR} Pulse Width, LOW	5.0		6.5		5.0		ns
t _{rec}	Recovery Time, \overline{MR} to CP	5.0		6.0		5.0		

Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



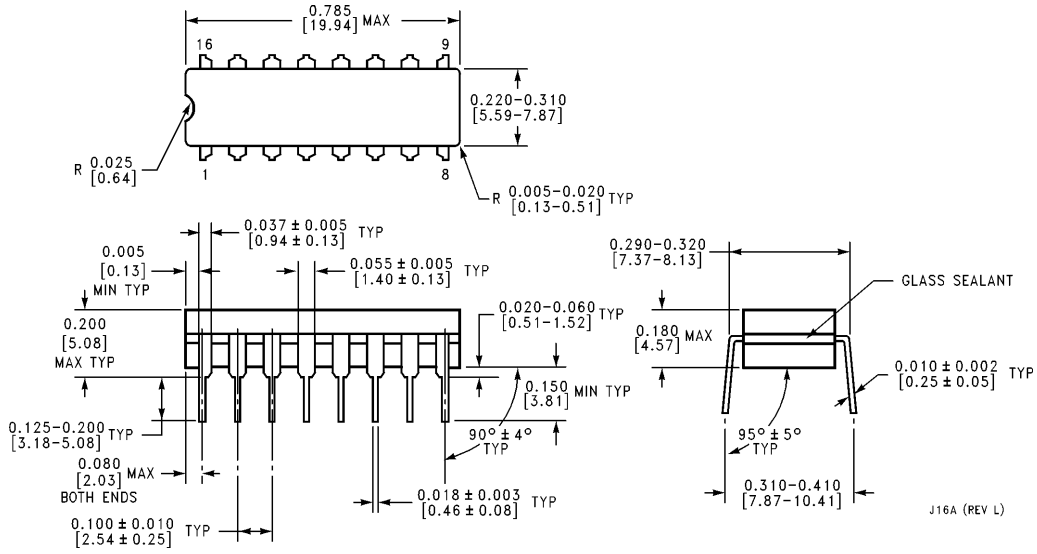
Physical Dimensions inches (millimeters)



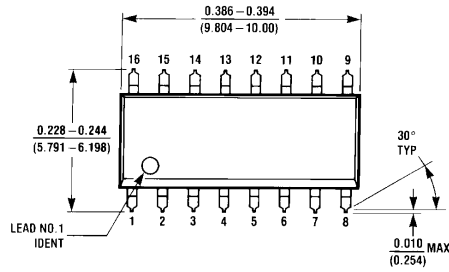
20-Terminal Ceramic Leadless Chip Carrier (L)
NS Package Number E20A

E20A (REV D)

Physical Dimensions inches (millimeters) (Continued)

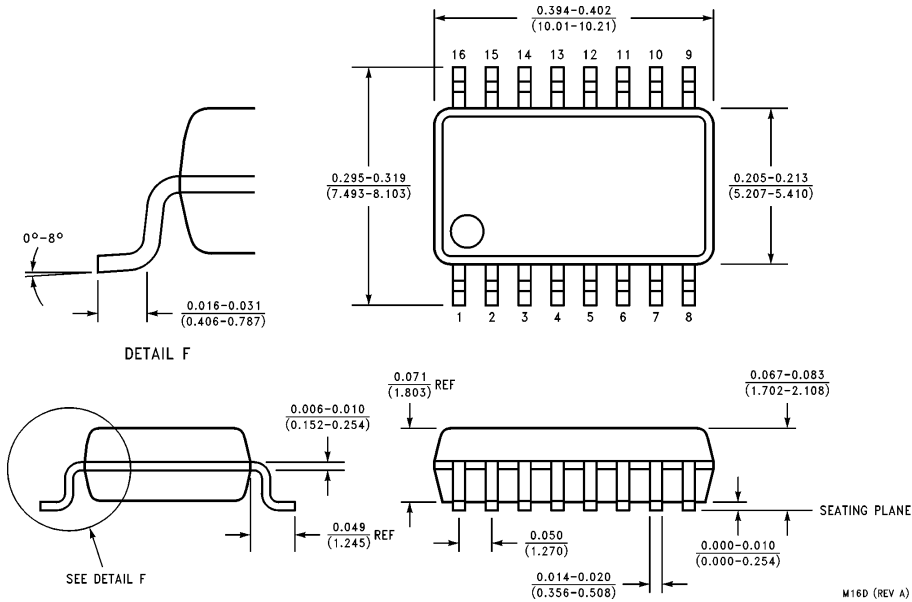


16-Lead Ceramic Dual-In-Line Package (D)
NS Package Number J16A

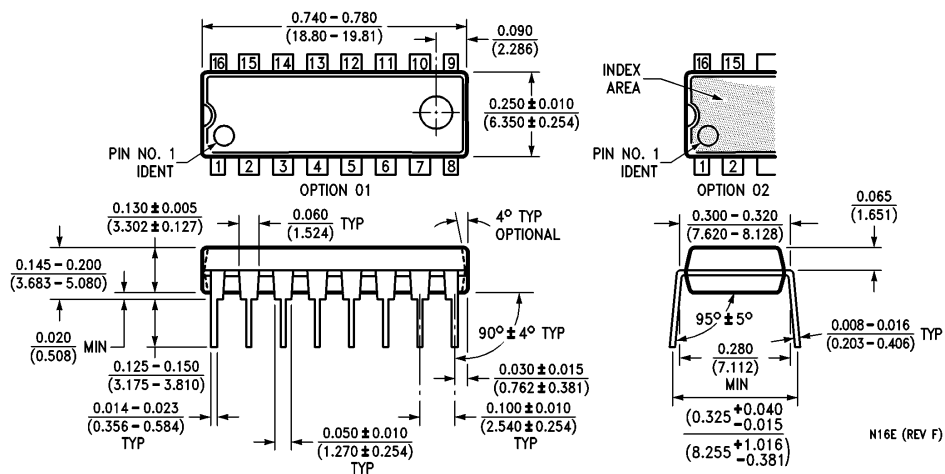


16-Lead (0.150" Wide) Molded Small Outline Package, JEDEC (S)
NS Package Number M16A

Physical Dimensions inches (millimeters) (Continued)

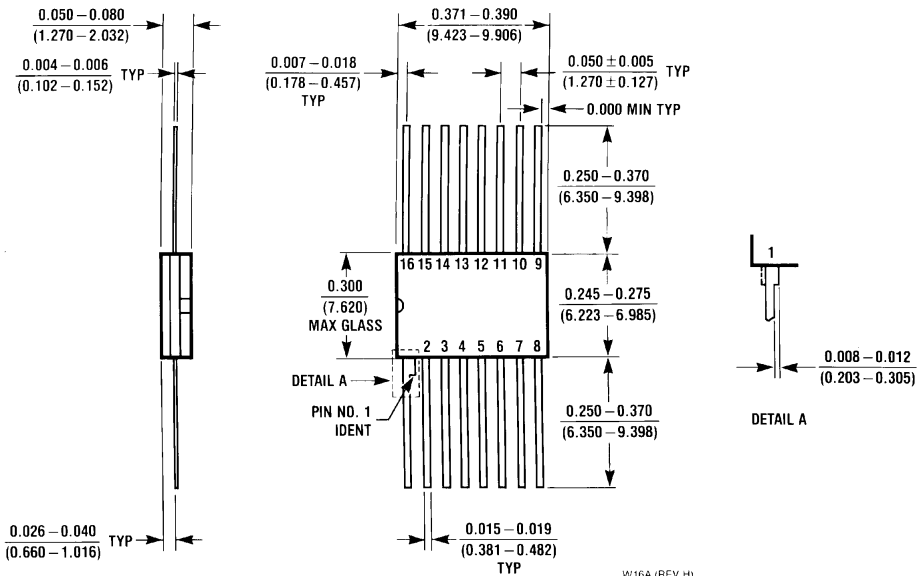


16-Lead (0.300" Wide) Molded Small Outline Package, EIAJ (SJ)
NS Package Number M16D



16-Lead (0.300" Wide) Molded Dual-In-Line Package (P)
NS Package Number N16E

Physical Dimensions inches (millimeters) (Continued)



**16 Lead Ceramic Flatpak (F)
NS Package Number W16A**

W16A (REV H)

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National Semiconductor Corporation
2900 Semiconductor Drive
P.O. Box 58090
Santa Clara, CA 95052-8090
Tel: 1(800) 272-9959
TWX: (910) 339-9240

National Semiconductor GmbH
Livry-Gargan-Str. 10
D-82256 Fürstenfeldbruck
Germany
Tel: (81-41) 35-0
Telex: 527649
Fax: (81-41) 35-1

National Semiconductor Japan Ltd.
Sumitomo Chemical
Engineering Center
Bldg. 7F
1-7-1, Nakase, Mihama-Ku
Chiba-City,
Ciba Prefecture 261
Tel: (043) 299-2300
Fax: (043) 299-2500

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductores Do Brazil Ltda.
Rue Deputado Lacerda Franco
120-3A
Sao Paulo-SP
Brazil 05418-000
Tel: (55-11) 212-5066
Telex: 391-1131931 NSBR BR
Fax: (55-11) 212-1181

National Semiconductor (Australia) Pty, Ltd.
Building 16
Business Park Drive
Monash Business Park
Nottingham, Melbourne
Victoria 3168 Australia
Tel: (3) 558-9999
Fax: (3) 558-9998

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