CY7C133
CY7C143

2K x 16 Dual-Port Static RAM

Features

- **True dual-ported memory cells which allow simultaneous reads of the same memory location**
- **2K x 16 organization**
- **0.65-micron CMOS for optimum speed/power**
- **High-speed access: 25/35/55 ns**
- **Low operating power: I_{CC} = 150 mA (typ.)**
- **Fully asynchronous operation**
- **Master CY7C133 expands data bus width to 32 bits or more using slave CY7C143**
- **BUSY output flag on CY7C133; BUSY input flag on CY7C143**
- **Available in 68-pin PLCC**

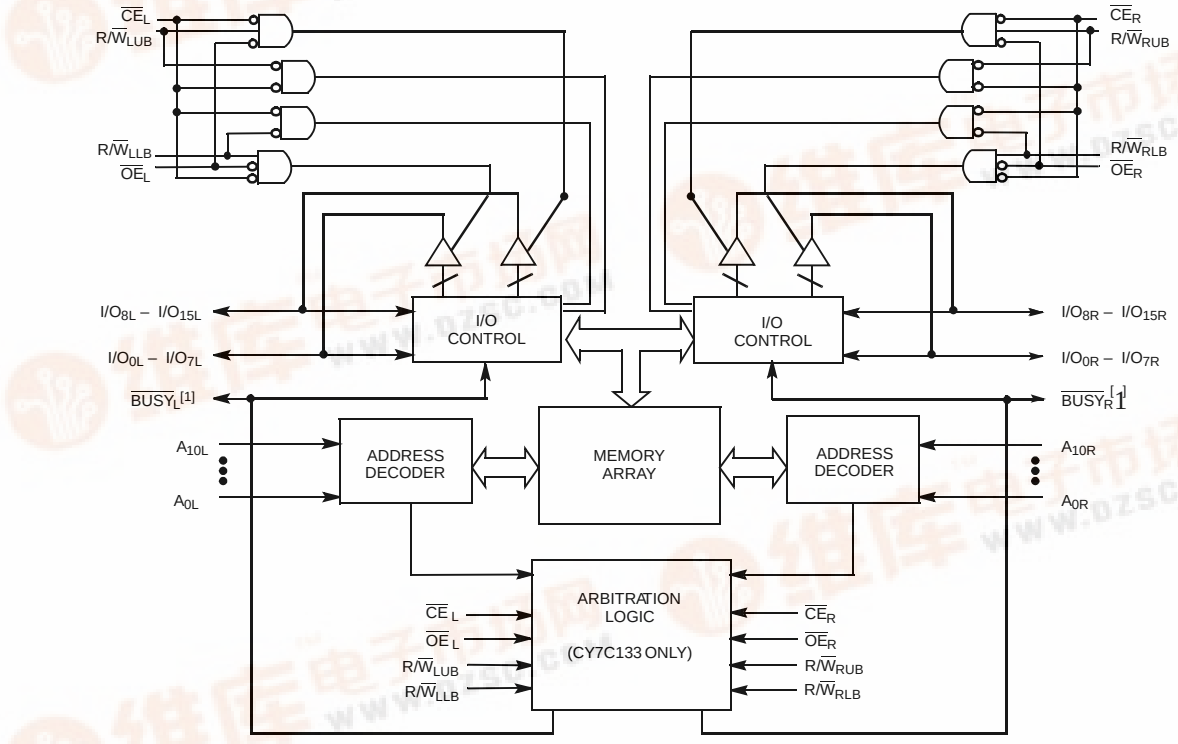
Functional Description

The CY7C133 and CY7C143 are high-speed CMOS 2K by 16 dual-port static RAMs. Two ports are provided permitting independent access to any location in memory. The CY7C133 can be utilized as either a stand-alone 16-bit dual-port static RAM or as a master dual-port RAM in conjunction with the CY7C143 slave dual-port device in systems requiring 32-bit or greater word widths. It is the solution to applications requiring shared or buffered data, such as cache memory for DSP, bit-slice, or multiprocessor designs.

Each port has independent control pins; Chip Enable ($\overline{CE}$), Write Enable ($R/\overline{W}_{UB}$, $R/\overline{W}_{LB}$), and Output Enable ($\overline{OE}$). $\overline{BUSY}$ signals that the port is trying to access the same location currently being accessed by the other port. An automatic power-down feature is controlled independently on each port by the Chip Enable ($\overline{CE}$) pin.

The CY7C133 and CY7C143 are available in 68-pin PLCC.

Logic Block Diagram

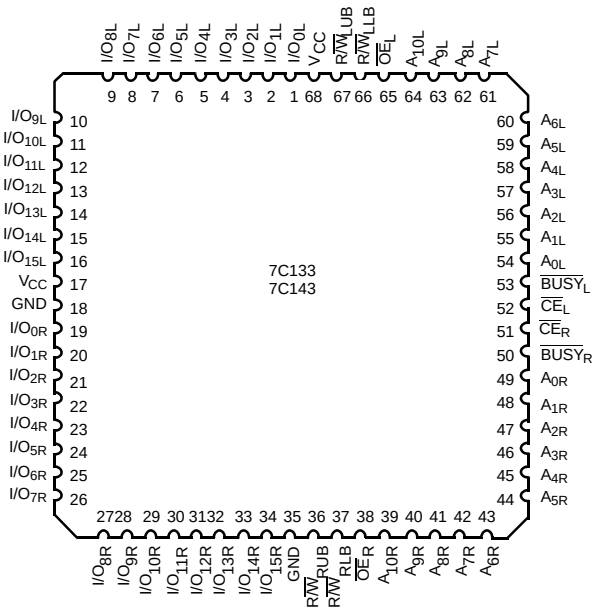


Note:

1. CY7C133 (Master): $\overline{BUSY}$ is open drain output and requires pull-up resistor. CY7C143 (Slave): $\overline{BUSY}$ is input.

Pin Configuration

68-Pin LCC/PLCC
Top View



Selection Guide

	7C133-25 7C143-25	7C133-35 7C143-35	7C133-55 7C143-55	Unit
Maximum Access Time	25	35	55	ns
Typical Operating Current I_{CC}	170	160	150	mA
Typical Standby Current for I_{SB1}	40	30	20	mA

Architecture

The CY7C133 (master) and CY7C143 (slave) consist of an array of 2K words of 16 bits each of dual-port RAM cells, I/O and address lines, and control signals (CE, OE, R/W). These control pins permit independent access for reads or writes to any location in memory. To handle simultaneous writes/reads to the same location, a BUSY pin is provided on each port. The CY7C133 and CY7C143 have an automatic power-down feature controlled by CE. Each port is provided with its own output enable control (OE), which allows data to be read from the device.

Functional Description

Write Operation

Data must be set up for a duration of t_{SD} before the rising edge of R/W in order to guarantee a valid write. A write operation is controlled by either the R/W pin (see Write Cycle No. 1 waveform) or the CE pin (see Write Cycle No. 2 waveform). Two R/W pins (R/W_{UB} and $R/W_{\overline{LB}}$) are used to separate the upper and lower bytes of IO. Required inputs for non-contention operations are summarized in *Table 1*.

If a location is being written to by one port and the opposite port attempts to read that location, a port-to-port flow-through delay must occur before the data is read on the output; otherwise the data read is not deterministic. Data will be valid on the port t_{DDD} after the data is presented on the other port.

Read Operation

When reading the device, the user must assert both the OE and CE pins. Data will be available t_{ACE} after CE or t_{DOE} after OE is asserted.

Busy

The CY7C133 (master) provides on-chip arbitration to resolve simultaneous memory location access (contention). *Table 2* shows a summery of conditions where BUSY is asserted. If both ports' CEs are asserted and an address match occurs within t_{PS} of each other, the busy logic will determine which port has access. If t_{PS} is violated, one port will definitely gain permission to the location, but which one is not predictable. BUSY will be asserted t_{BLA} after an address match or t_{BLC} after CE is taken LOW. The results of all eight arbitration possibilities are summarized in *Table 3*. BUSY is an open drain output and requires a pull-up resistor.

One master and as many slaves as necessary may be connected in parallel to expand the data bus width in 16 bit increments. The BUSY output of the master is connected to the BUSY input of the slave. Writing to slave devices must be delayed until after the BUSY input has settled (t_{BLC} or t_{BLA}). Otherwise, the slave chip may begin a write cycle during a contention situation.

Flow-Through Operation

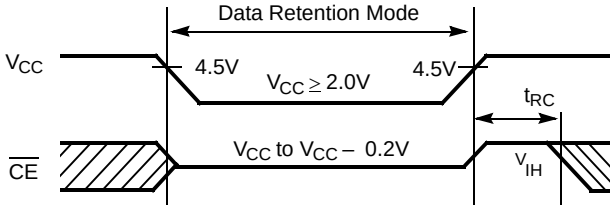
The CY7C133/143 has a flow-through architecture that facilitates repeating (actually extending) an operation when a BUSY is received by a losing port. The BUSY signal should be interpreted as a NOT READY. If a BUSY to a port is active, the port should wait for BUSY to go inactive, and then extend the operation it was performing for another cycle. The timing diagram titled, "Timing waveform with port to port delay" illustrates the case where the right port is writing to an address and the left port reads the same address. The data that the right port has just written flows through to the left, and is valid either t_{DDD} after the falling edge of the write strobe of the left port, or t_{DDD} after the data being written becomes stable.

Data Retention Mode

The CY7C133/143 is designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention:

1. Chip enable (CE) must be held HIGH during data retention, within V_{CC} to V_{CC} – 0.2V.
2. CE must be kept between V_{CC} – 0.2V and 70% of V_{CC} during the power-up and power-down transitions.
3. The RAM can begin operation >t_{RC} after V_{CC} reaches the minimum operating voltage (4.5V).

Timing



Parameter	Test Conditions[2]	Max.	Unit
ICC_{DR1}	@ VCC_{DR} = 2V	1.5	mA

Note:
2. CE = V_{CC}, V_{in} = GND to V_{CC}, T_A = 25°C. This parameter is guaranteed but not tested.

Table 1. Non-Contending Read/Write Control

Control				I/O		
R/W_{LB}	R/W_{UB}	$\overline{CE}$	$\overline{OE}$	$I/O_0–I/O_8$	$I/O_9–I/O_{17}$	Operation
X	X	H	X	High Z	High Z	Deselected: Power-Down
L	L	L	X	Data In	Data In	Write to Both Bytes
L	H	L	L	Data In	Data Out	Write Lower Byte, Read Upper Byte
H	L	L	L	Data Out	Data In	Read Lower Byte, Write Upper Byte
L	H	L	H	Data In	High Z	Write to Lower Byte
H	L	L	H	High Z	Data In	Write to Upper Byte
H	H	L	L	Data Out	Data Out	Read to Both Bytes
H	H	L	H	High Z	High Z	High Impedance Outputs

Table 2. Address BUSY Arbitration

Inputs			Outputs		
$\overline{CE}_L$	$\overline{CE}_R$	$Address_L$ $Address_R$	$\overline{BUSY}_L$	$\overline{BUSY}_R$	Function
X	X	No Match	H	H	Normal
H	X	Match	H	H	Normal
X	H	Match	H	H	Normal
L	L	Match	Note 3	Note 3	Write Inhibit[4]

32-Bit Master/Slave Dual-Port Memory Systems

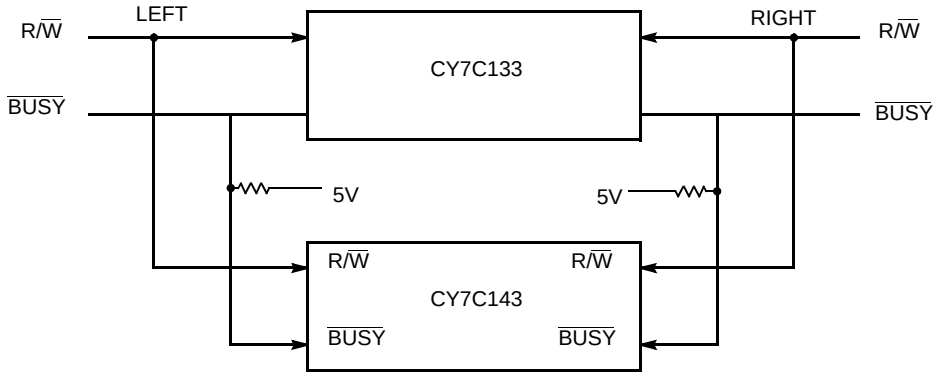


Table 3. Arbitration Results

Case	Port		Winning Port	Result
	Left	Right		
1	Read	Read	L	Both ports read
2	Read	Read	R	Both ports read
3	Read	Write	L	L port reads OK R port write inhibited
4	Read	Write	R	R port writes OK L port data may be invalid
5	Write	Read	L	L port writes OK R port data may be invalid
6	Write	Read	R	R port reads OK L port write inhibited
7	Write	Write	L	L port writes OK R port write inhibited
8	Write	Write	R	R port writes OK L port write inhibited

Notes:
3. The loser of the port arbitration will receive $\overline{BUSY}$ = "L" ($\overline{BUSY}_L$ or $\overline{BUSY}_R$ = "L"). $\overline{BUSY}_L$ and $\overline{BUSY}_R$ cannot both be LOW simultaneously.
4. Writes are inhibited to the left port when $\overline{BUSY}_L$ is LOW. Writes are inhibited to the right port when $\overline{BUSY}_R$ is LOW.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied..... –55°C to +125°C

Supply Voltage to Ground Potential (Pin 48 to Pin 24)..... –0.5V to +7.0V

DC Voltage Applied to Outputs in High-Z State..... –0.5V to +7.0V

DC Input Voltage..... –3.5V to +7.0V

Output Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage..... >2001V (per MIL-STD-883, Method 3015)

Latch-up Current..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	–40°C to +85°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		7C133-25 7C143-25 Min.	Typ.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA		2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 4.0 mA				0.4	V
		I_{OL} = 16.0 mA[5]				0.5	
V_{IH}	Input HIGH Voltage			2.2			V
V_{IL}	Input LOW Voltage					0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		–5		+5	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		–5		+5	µA
I_{OS}	Output Short Circuit Current[6,7]	V_{CC} = Max., V_{OUT} = GND				–200	mA
I_{CC}	V_{CC} Operating Supply Current	$\overline{CE}$ = V_{IL}, Outputs Open, f = f_{MAX}[8]	Com'l		170	250	mA
			Ind.		170	290	
I_{SB1}	Standby Current Both Ports, TTL Inputs	$\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[8]	Com'l		40	60	mA
			Ind.		40	75	
I_{SB2}	Standby Current One Port, TTL Inputs	$\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{IH}, Active Port Outputs Open, f = f_{MAX}[8]	Com'l		100	140	mA
			Ind.		100	160	
I_{SB3}	Standby Current Both Ports, CMOS Inputs	Both Ports $\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{CC} – 0.2V, V_{IN} ≥ V_{CC} – 0.2V or V_{IN} ≤ 0.2V, f = 0	Com'l		3	15	mA
			Ind.		3	15	
I_{SB4}	Standby Current One Port, CMOS Inputs	One Port $\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{CC} – 0.2V, V_{IN} ≥ V_{CC} – 0.2V or V_{IN} ≤ 0.2V, Active Port Outputs Open, f = f_{MAX}[8]	Com'l		90	120	mA
			Ind.		90	140	

Electrical Characteristics Over the Operating Range (continued)

Parameter	Description	Test Conditions	7C133-35 7C143-35 Min.	Typ.	Max.	7C133-55 7C143-55 Min.	Typ.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA	2.4			2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 4.0 mA			0.4			0.4	V
		I_{OL} = 16.0 mA[5]			0.5			0.5	
V_{IH}	Input HIGH Voltage		2.2			2.2			V
V_{IL}	Input LOW Voltage				0.8			0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}	–5		+5	–5		+5	µA

Notes:

5. $\overline{BUSY}$ pin only.
6. Duration of the short circuit should not exceed 30 seconds.
7. Tested initially and after any design or process changes that may affect these parameters.
8. At f=f_{MAX}, address and data inputs are cycling at the maximum frequency of read cycle of 1/t_{RC} and using AC Test Waveforms input levels of GND to 3V.

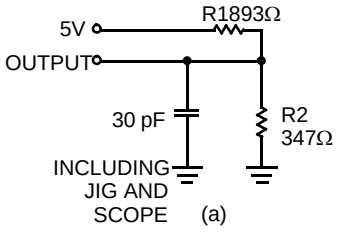
Electrical Characteristics Over the Operating Range (continued)

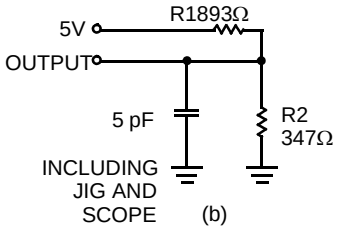
Parameter	Description	Test Conditions		7C133-35 7C143-35 Min.	Typ.	Max.	7C133-55 7C143-55 Min.	Typ.	Max.	Unit
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		–5		+5	–5		–5	µA
I_{OS}	Output Short Circuit Current[6, 7]	V_{CC} = Max., V_{OUT} = GND				–200			–200	mA
I_{CC}	V_{CC} Operating Supply Current	$\overline{CE}$ = V_{IL}, Outputs Open, f = f_{MAX}[8]	Com'l		160	230		150	220	mA
			Ind.		160	260		150	250	
I_{SB1}	Standby Current Both Ports, TTL Inputs	$\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[8]	Com'l		30	50		20	40	mA
			Ind.		30	65		20	55	
I_{SB2}	Standby Current One Port, TTL Inputs	$\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{IH}, Active Port Outputs Open, f = f_{MAX}[8]	Com'l		85	125		75	110	mA
			Ind.		85	140		75	125	
I_{SB3}	Standby Current Both Ports, CMOS Inputs	Both Ports $\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{CC} - 0.2V, V_{IN} ≥ V_{CC} – 0.2V or V_{IN} ≤ 0.2V, f = 0	Com'l		3	15		3	15	mA
			Ind.		3	15		3	15	
I_{SB4}	Standby Current One Port, CMOS Inputs	One Port $\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{CC} – 0.2V, V_{IN} ≥ V_{CC} – 0.2V or V_{IN} ≤ 0.2V, Active Port Outputs Open, f = f_{MAX}[8]	Com'l		80	105		70	90	mA
			Ind.		80	120		70	105	

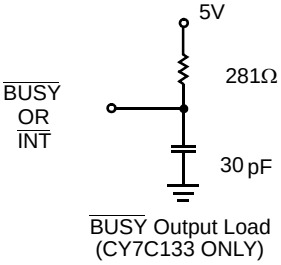
Capacitance[7]

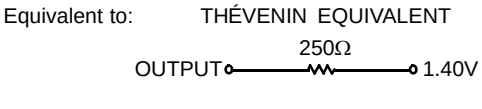
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

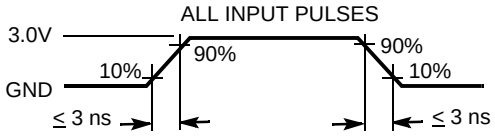
AC Test Loads and Waveforms











Switching Characteristics Over the Operating Range[9]

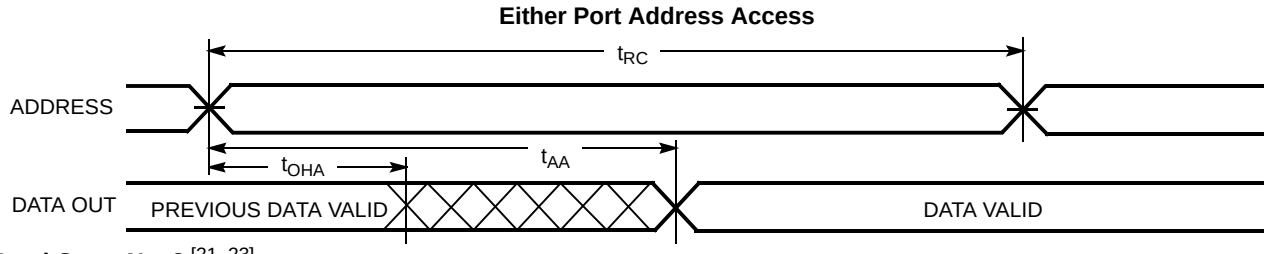
Parameter	Description	7C133-25 7C143-25		7C133-35 7C143-35		7C133-55 7C143-55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t_{RC}	Read Cycle Time	25		35		55		ns
t_{AA}	Address to Data Valid[10]		25		35		55	ns
t_{OHA}	Data Hold from Address Change	0		0		0		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid[10]		25		35		55	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid[10]		20		25		30	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[11, 12,13]	3		3		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[11, 12,13]		15		20		25	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[11, 12,13]	3		5		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[11, 12,13]		15		20		20	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up[13]	0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down[13]		25		25		25	ns
Write Cycle[14]								
t_{WC}	Write Cycle Time	25		35		55		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	20		25		40		ns
t_{AW}	Address Set-up to Write End	20		25		40		ns
t_{HA}	Address Hold from Write End	2		2		2		ns
t_{SA}	Address Set-up to Write Start	0		0		0		ns
t_{PWE}	R/$\overline{W}$ Pulse Width	20		25		35		ns
t_{SD}	Data Set-up to Write End	15		20		20		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{HZWE}	R/$\overline{W}$ LOW to High Z[12,13]		15		20		20	ns
t_{LZWE}	R/$\overline{W}$ HIGH to Low Z[12,13]	0		0		0		ns
Busy/Interrupt Timing (for master CY7C133)								
t_{BLA}	$\overline{BUSY}$ Low from Address Match		25		35		50	ns
t_{BHA}	$\overline{BUSY}$ High from Address Mismatch		20		30		40	ns
t_{BLC}	$\overline{BUSY}$ Low from $\overline{CE}$ LOW		20		25		35	ns
t_{BHC}	$\overline{BUSY}$ High from $\overline{CE}$ HIGH		20		20		30	ns
t_{WDD}	Write Pulse to Data Delay[15]		50		60		80	ns
t_{DDD}	Write Data Valid to Read Data Valid[15]		35		45		55	ns
t_{BDD}	$\overline{BUSY}$ High to Valid Data[16]		Note 16		Note 16		Note 16	ns
t_{PS}	Arbitration Priority Set Up Time[17]	5		5		5		ns
Busy Timing (for slave CY7C143)								
t_{WB}	Write to $\overline{BUSY}$[18]	0		0		0		ns
t_{WH}	Write Hold After $\overline{BUSY}$[19]	20		25		30		ns
t_{WDD}	Write Pulse to Data Delay[20]		50		60		80	ns
t_{DDD}	Write Data Valid to Read Data Valid[20]		35		45		55	ns

Notes:

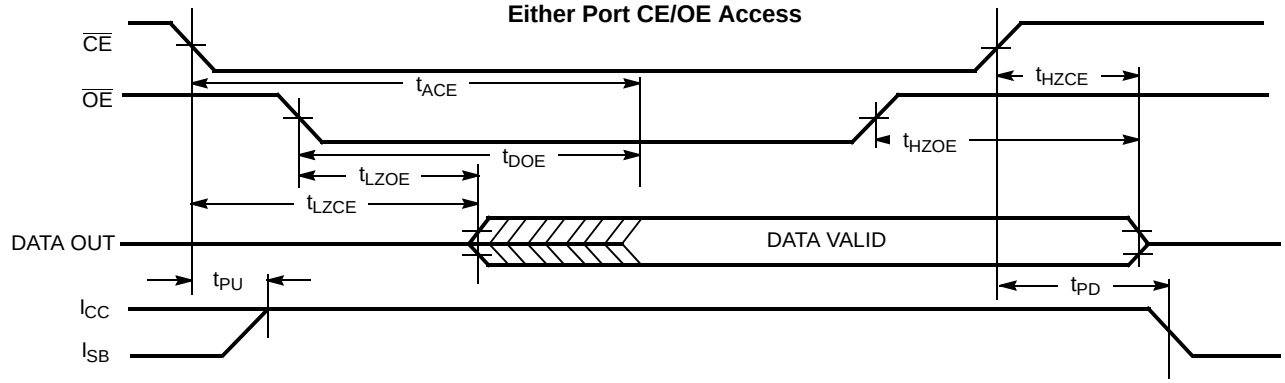
9. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH}, and 30-pF load capacitance.
10. AC Test Conditions use V_{OH} = 1.6V and V_{OL} = 1.4V.
11. At any given temperature and voltage condition for any given device, t_{LZCE} is less than t_{HZCE} and t_{LZOE} is less than t_{HZOE}.
12. t_{LZCE}, t_{LZWE}, t_{HZOE}, t_{LZOE}, t_{HZCE} and t_{HZWE} are tested with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
13. This parameter is guaranteed but not tested.
14. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and R/$\overline{W}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
15. Port-to-port delay through RAM cells from writing port to reading port. Refer to timing waveform of "Read with BUSY, Master: CY7C133."
16. t_{BDD} is a calculated parameter and is greater of 0,t_{WDD}–t_{WP} (actual) or t_{DDD}–t_{DW} (actual).
17. To ensure that the earlier of the two ports wins.
18. To ensure that write cycle is inhibited during contention.
19. To ensure that a write cycle is completed after contention.
20. Port-to-port delay through RAM cells from writing port to reading port. Refer to timing waveform of "Read with Port-to-port Delay."

Switching Waveforms

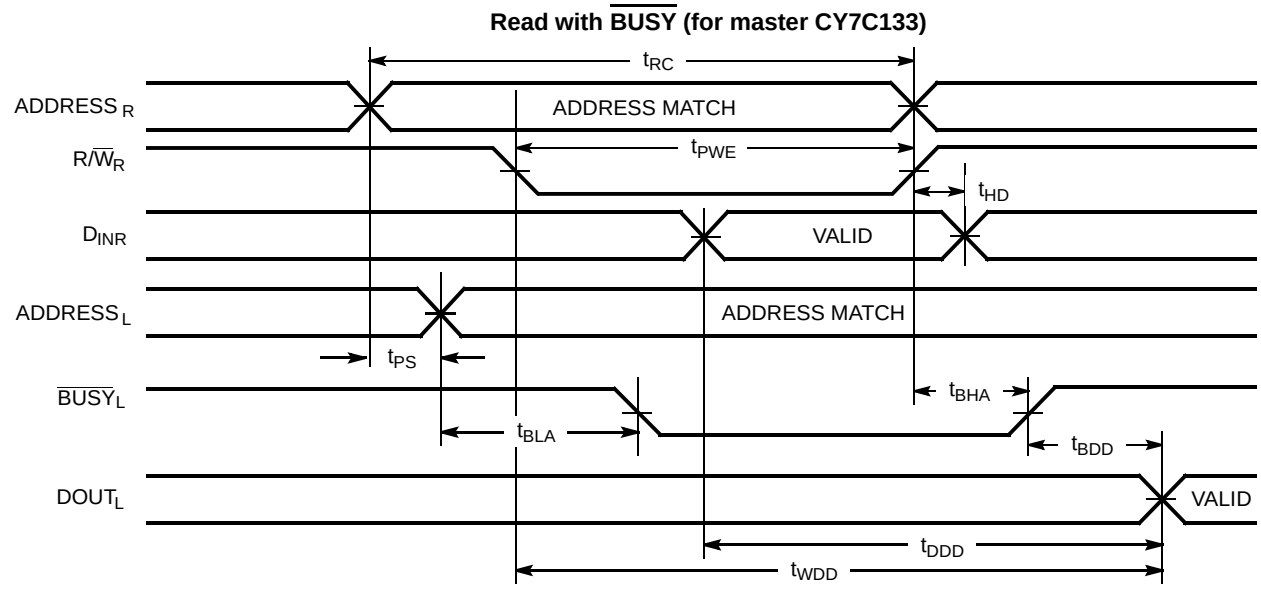
Read Cycle No.1 [21, 22]



Read Cycle No. 2 [21, 23]



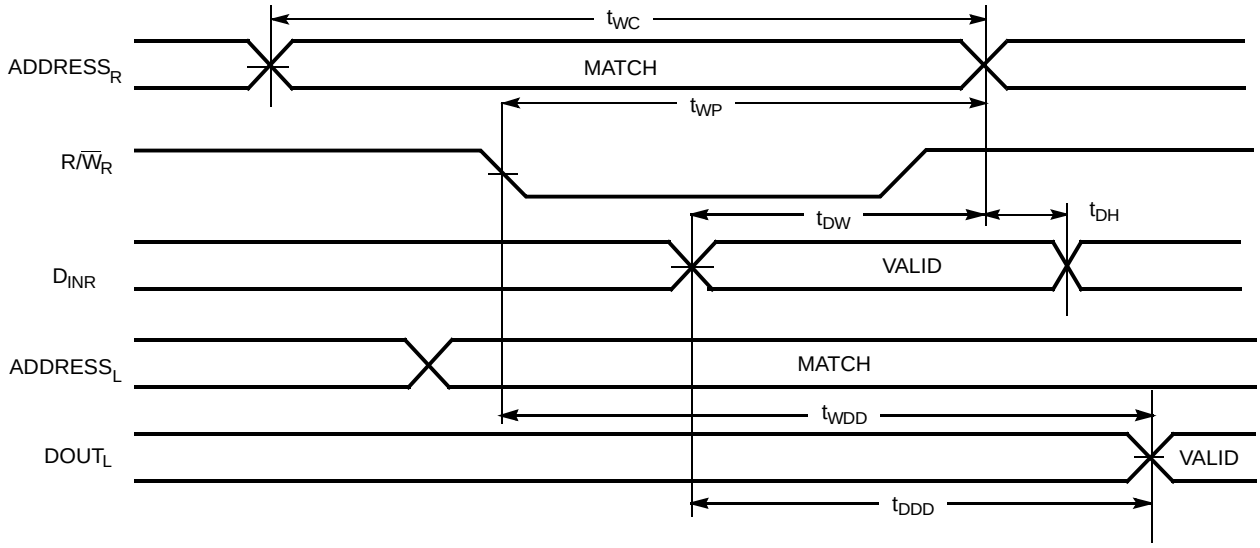
Read Cycle No. 3 [22]



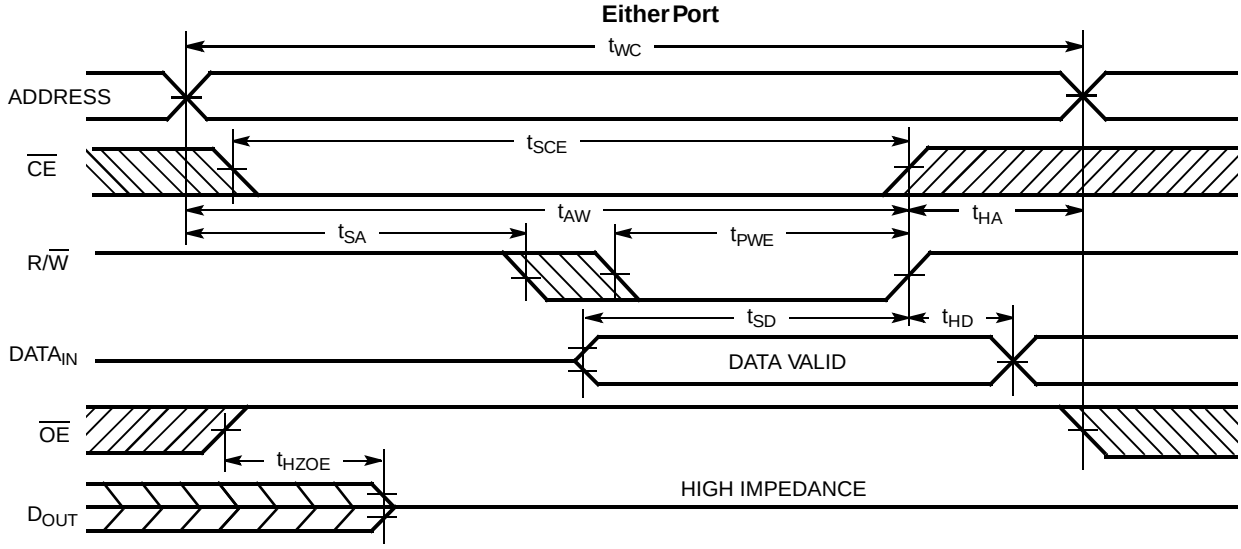
Note:
21. R/W is HIGH for read cycle.
22. Device is continuously selected, CE = V_{IL} and OE = V_{IL}.
23. Address valid prior to or coincidence with CE transition LOW.

Switching Waveforms (continued)

Timing Waveform of Read with Port-to-port Delay No. 4 (for slave CY7C143) [24, 25, 26]



Write Cycle No. 1 (OE Three-States Data I/Os - Either Port) [17, 27]

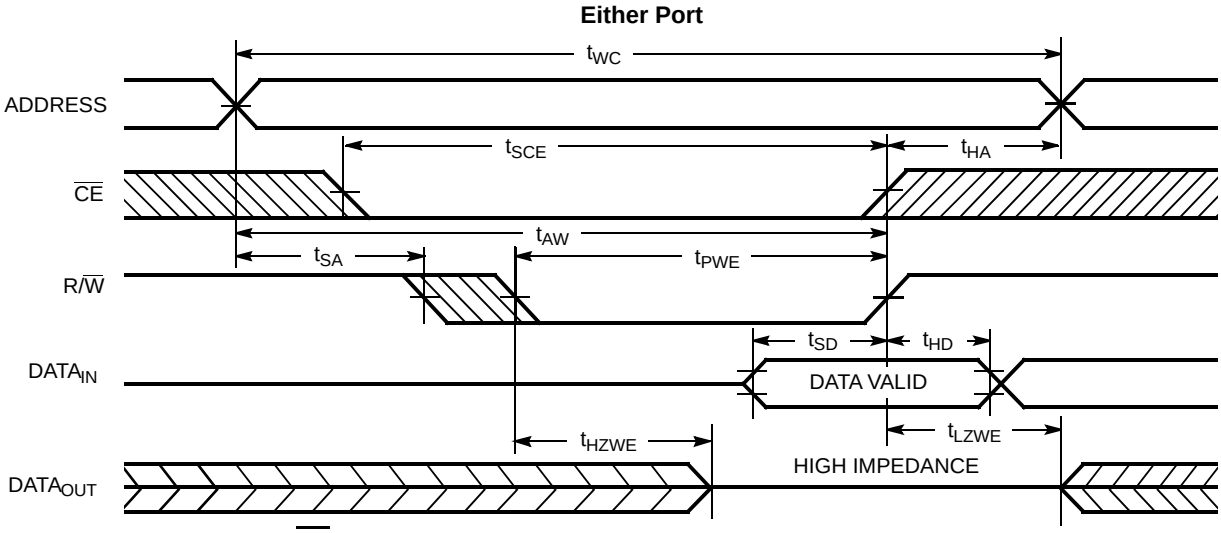


Notes:

24. Assume $\overline{BUSY}$ input at V_{IH} for the writing port and at V_{IL} for the reading port.l
25. Write cycle parameters should be adhered to in order to ensure proper writing.
26. Device is continuously enabled for both ports.
27. If OE is LOW during a R/W controlled write cycle, the write pulse width must be the larger of t_{PWE} or $t_{HZWE} + t_{SD}$ to allow the data I/O pins to enter high impedance and for data to be placed on the bus for the required t_{SD}.

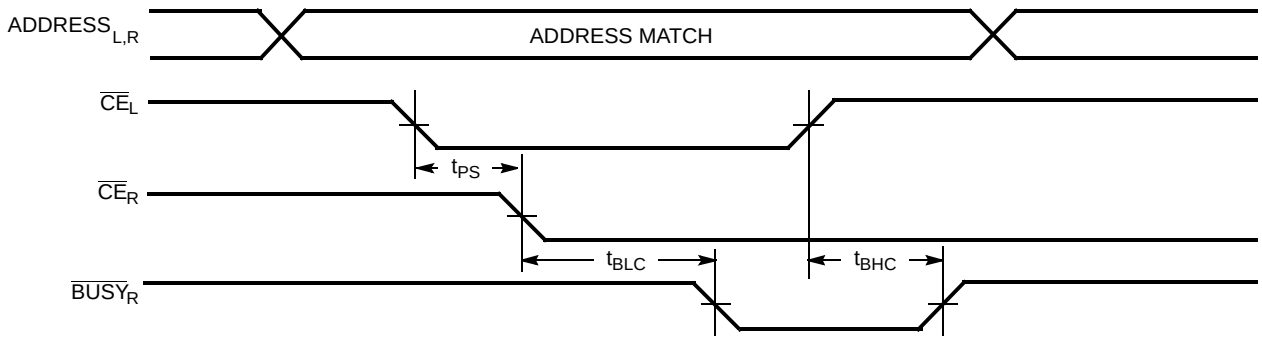
Switching Waveforms (continued)

Write Cycle No. 2 (R/W Three-States Data I/Os—Either Port) [23, 28]

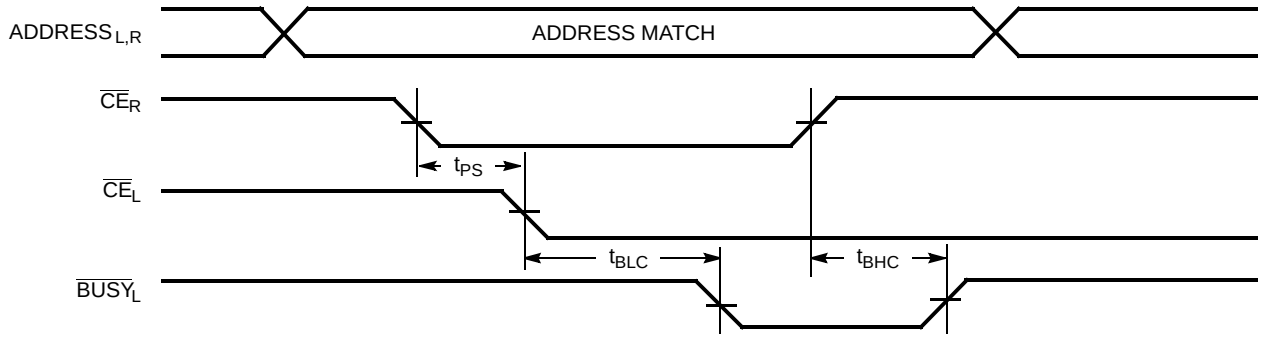


Busy Timing Diagram No. 1 ($\overline{CE}$ Arbitration)

$\overline{CE_L}$ Valid First:



$\overline{CE_R}$ Valid First:



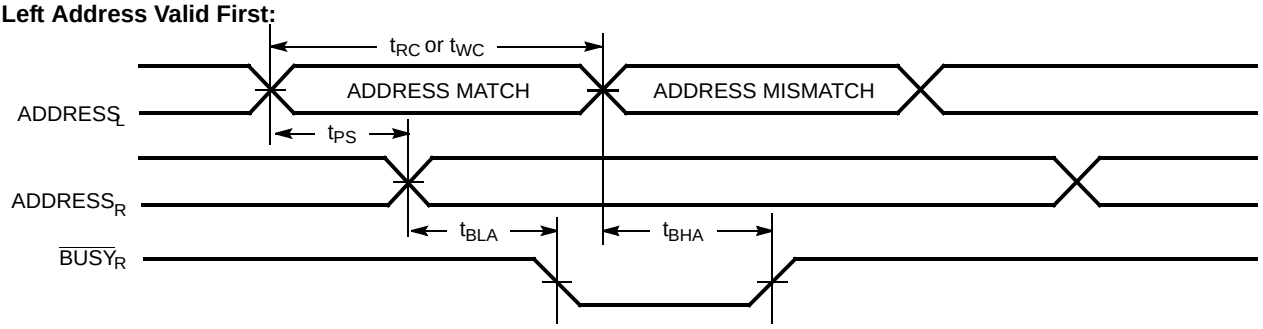
Note:

28. If the CE LOW transition occurs simultaneously with or after the R/W LOW transition, the outputs remain in the high-impedance state.

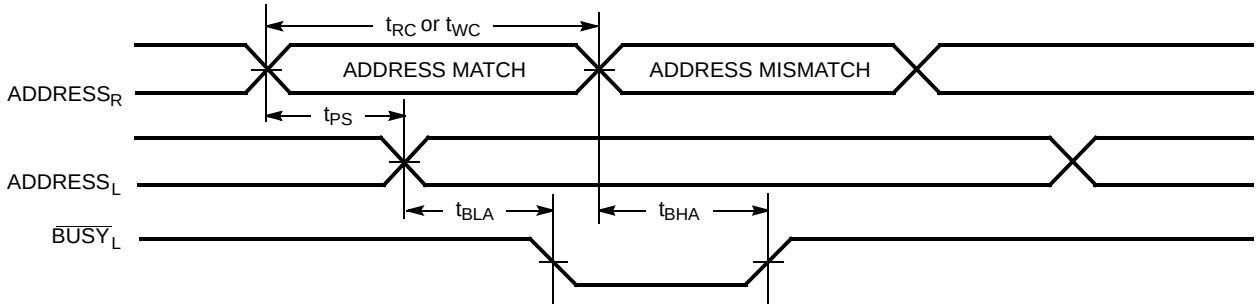
Switching Waveforms (continued)

Busy Timing Diagram No. 2 (Address Arbitration)

Left Address Valid First:

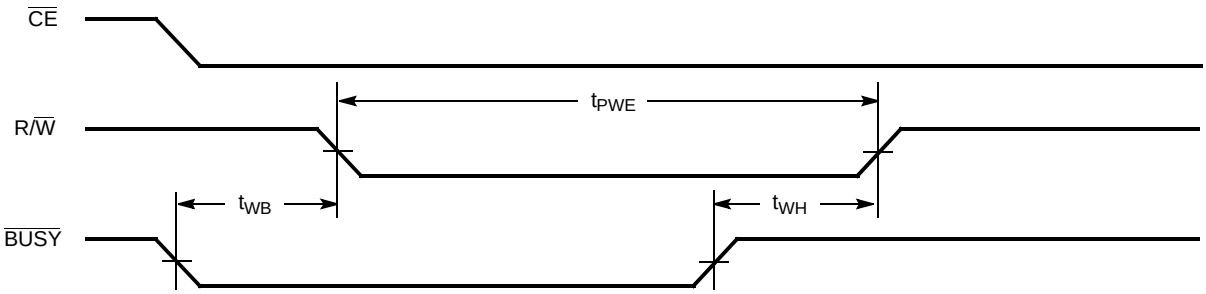


Right Address Valid First:



Busy Timing Diagram No. 3

Write with $\overline{\text{BUSY}}$ (For Slave CY7C143)



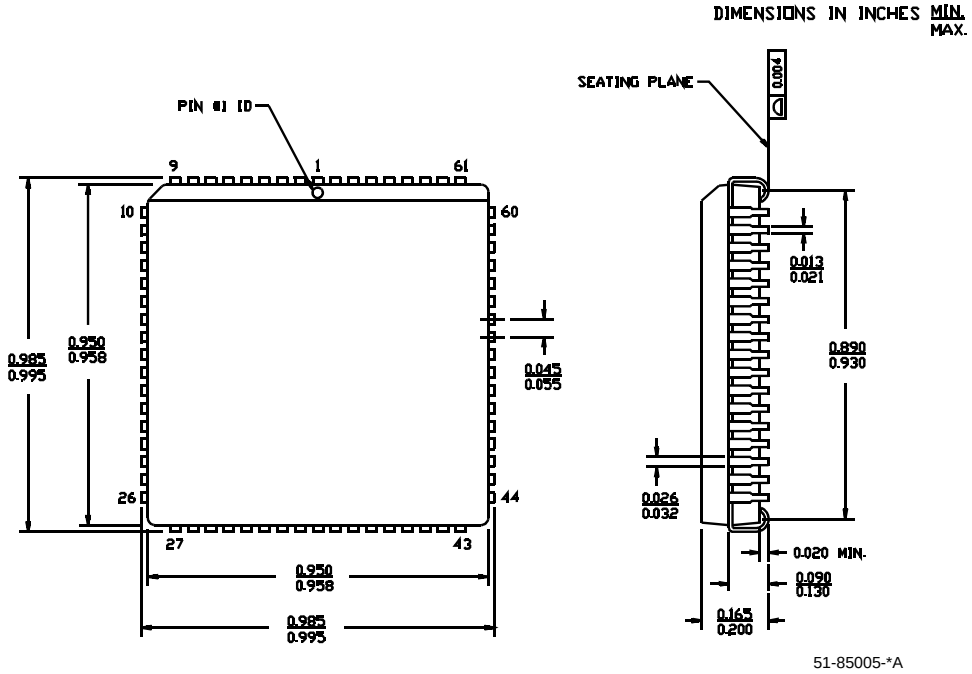
Ordering Information

2K x 16 Master Dual-Port SRAM

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CY7C133-25JC	J81	68-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C133-25JI	J81	68-Lead Plastic Leaded Chip Carrier	Industrial
35	CY7C133-35JC	J81	68-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C133-35JI	J81	68-Lead Plastic Leaded Chip Carrier	Industrial
55	CY7C133-55JC	J81	68-Lead Plastic Leaded Chip Carrier	Commercial

Package Diagram

68-Lead Plastic Leaded Chip Carrier J81



51-85005-*A

Document History Page

Document Title: CY7C133/CY7C143 2K x 16 Dual-Port Static RAM Document Number: 38-06036				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	110178	09/22/01	SZV	Change from Spec number: 38-00414 to 38-06036
*A	127954	08/27/03	FSG	Logic Block Diagram: fixed busy I/O flag on devices (typo) Removed obsolete parts from ordering information table: –CY7C133-55JI –CY7C143-25JC –CY7C143-25JI –CY7C143-35JC –CY7C143-35JI –CY7C143-55JC –CY7C143-55JI
*B	236761	See ECN	YDT	Removed cross information from features section