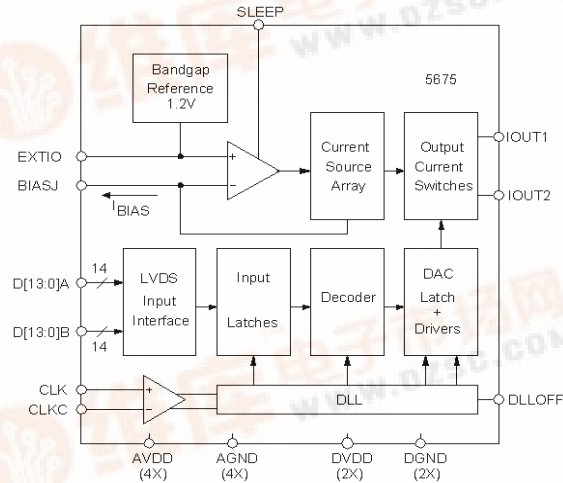
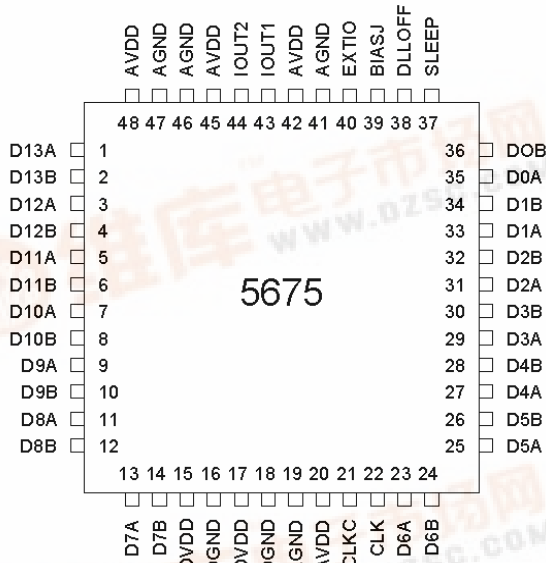




# 5675

## 14-BIT, 400MSPS

### DIGITAL-TO-ANALOG CONVERTER



Functional Block Diagram

### FEATURES:

- 400-MSPS Update Rate
- LVDS-Compatable Input Interface
- Differential Scalable Current Outputs: 2mA to 20mA
- On-Chip 1.2-V Reference
- Single 3.3-V Supply Operation
- Power Dissipation: 820 mW at  $f_{CLK} = 400\text{MHz}$ ,  $f_O = 70\text{MHz}$

### DESCRIPTION:

Maxwell Technologies 5675 is a 14-bit resolution high-speed digital to analog converter. The 5675 is designed for high-speed digital data transmission in wired and wireless communication systems. The 5675 has excellent spurious free dynamic range (SFDR) at high intermediate frequencies.

The 5675 operates from a single-supply voltage of 3.3V. Power dissipation is 820 mW at  $f_{CLK} = 400\text{MSPS}$ ,  $f_{out} = 70\text{MHz}$ . The 5675 provides a nominal full-scale differential current output of 20mA, supporting both single-ended and differential applications. The output can be directly fed to the load with no additional external output buffered required.

Maxwell Technologies' patented RAD-PAK<sup>®</sup> packaging technology incorporates radiation shielding in the micro-circuit package. It eliminates the need for box shielding while providing the required radiation shielding for a lifetime in orbit or space mission. In a GEO orbit, RAD-PAK<sup>®</sup> provides greater than 100 krad(Si) radiation dose tolerance. This product is available with screening up to Class S.



TABLE 1. PINOUT DESCRIPTION

PIN	SYMBOL	DESCRIPTION
19, 41, 46, 47	AGND	Analog Negative Supply Voltage (Ground)
20, 42, 45, 48	AVDD	Analog Positive Supply Voltage
39	BIASJ	Full-scale Output Current Bias
22	CLK	External Clock Input
21	CLKC	Complementary External Clock Input
1, 3, 5, 7, 9, 13, 23 25, 27, 29, 31, 33, 35	D9(13:0)A	LVDS Positive Input, data bits 13 through 0 D13A is most significant data bit (MSB) D0A is the least significant bit (LSB)
2, 4, 6, 8, 10, 14, 24 26, 28, 30, 32, 34, 36	D(13:0)B	LVDS Positive Input, data bits 13 through 0 D13B is most significant data bit (MSB) D0B is the least significant bit (LSB)
16, 18	DGND	Digital Negative Supply Voltage (Ground)
38	DLLOFF	High = DLL Off / Low = DLL On
15, 17	DVDD	Digital Positive Supply Voltage
40	EXTIO	Internal reference out put or external reference input. Requires a 0.1uf decoupling capacitor to ground when used as reference output.
43	IOUT1	DAC current output. Full scale when all inputs are set to 1. Connect reference side DAC load resistors to AVDD
44	IOUT2	DAC complimentary current output. Full scale when all inputs are set to 0. Connect reference side DAC load resistors to AVDD
37	SLEEP	Asynchronous hardware power down input. Active high. Internally pulldown.

TABLE 2. 5675 ABSOLUTE MAXIMUM RATINGS <sup>1</sup>

PARAMETER	SYMBOL	MIN	MAX	UNIT
Supply Voltage Range	$AV_{DD}$	-0.3	3.6	V
	$DV_{DD}$	-0.3	3.6	V
	$AV_{DD}$ to $DV_{DD}$	-3.6	3.6	V
Voltage between AGND and DGND	--	-0.3	0.5	V
CLK, CLKC, SLEEP	--	-0.3 to DVDD	DVDD to 0.3	V
Digital input D[13:0]A, D[13:0]B	--	-0.3 to DVDD	DVDD to 0.3	V
IOUT1, IOUT2	--	-1.0 to DVDD	AVDD to 0.3	V
EXTIO, BIASJ	--	-0.3 to DVDD	AVDD to 0.3	V
Peak Input Current (any input)			20	mA
Peak Total Input Current (any input)			-30	mA
Storage temperature range		-65	150	°C

TABLE 2. 5675 ABSOLUTE MAXIMUM RATINGS <sup>1</sup>

PARAMETER	SYMBOL	MIN	MAX	UNIT
Operating Temperature range		-55	125	°C

1. Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

TABLE 3. DELTA LIMITS

PARAMETER	VARIATION
I <sub>AVDD</sub>	±10% of specified value in Table 5
I <sub>DVDD</sub>	±10% of specified value in Table 5

TABLE 4. 5675 RECOMMENDED OPERATING CONDITIONS <sup>1</sup>

PARAMETER		MIN	TYP	MAX	UNIT
Output Update Rate	DLL disable, DLLOFF=1			100	MSPS
	DLL enable, DLLOFF=0	100		400	
Analog Supply Voltage, AVDD		3.15	3.3	3.6	V
Digital Supply Voltage, DVDD		3.15	3.3	3.6	V
Input Reference Voltage, EXTIO		0.6	1.2	1.25	V
Full-scale output current I <sub>O(FS)</sub>		2		20	mA
Output compliance range	AVDD=3.15 to 3.45V, I <sub>O(FS)</sub> =20mA	AVDD-1		AVDD+0.3	V
Clock Differential Input Voltage, CLK-CLKC		0.4		0.8	V
Clock Pulse Width High, t <sub>WH</sub>			1.25		nS
Clock Pulse Width Low, t <sub>LH</sub>			1.25		nS
Clock Duty Cycle		40		60	%

1. All unused control inputs of the device must be held at high or low ensure proper device operation.

TABLE 5. 5675 DC ELECTRICAL CHARACTERISTICS

(DVDD = 3.3±10%, AVDD = 3.3±10%, T<sub>A</sub> = -55 TO +125 °C, UNLESS OTHERWISE SPECIFIED)

PARAMETER	TEST CONDITIONS	SYMBLE	SUBGROUPS	MIN	TYP	MAX	UNIT
<b>Resolution</b>				14			Bits
<b>DC Accuracy<sup>1</sup></b>							
Integral Nonlinearity	T <sub>MIN</sub> TO T <sub>MAX</sub>	INL		-4	±2	4	LSB
DIFFERENTIAL NONLINEARITY	T <sub>MIN</sub> TO T <sub>MAX</sub>	DNL		-2	±1.5	2	LSB
MONOTICITY				Monotonic 12-bit Level			

TABLE 5. 5675 DC ELECTRICAL CHARACTERISTICS  
 (DVDD = 3.3±10%, AVDD = 3.3±10%, T<sub>A</sub> = -55 TO +125 °C, UNLESS OTHERWISE SPECIFIED)

PARAMETER	TEST CONDITIONS	SYMBLE	SUBGROUPS	MIN	TYP	MAX	UNIT
<b>ANALOG OUTPUT</b>							
OFFSET ERROR					0.02		%FSR
GAIN ERROR	Without Internal Reference			-10		10	%FSR
	With Internal Reference			-10		10	%FSR
OUTPUT RESISTANCE					300		K
OUTPUT CAPACITANCE					5		pf
<b>REFERENCE OUTPUT</b>							
REFERENCE VOLTAGE			EXTIO	1.17	1.23	1.29	V
REFERENCE OUTPUT CURRENT <sup>2</sup>					100		nA
<b>REFERENCE INPUT</b>							
INPUT RESISTANCE					1		M
SMALL SIGNAL BANDWIDTH					1.4		MHz
INPUT CAPACITANCE					100		pf
<b>TEMPERATURE COEFFICIENTS</b>							
OFFSET DRIFT					0		ppm of FSR/°C
GAIN DRIFT	Without Internal Reference				±50		ppm of FSR/°C
REFERENCE VOLTAGE DRIFT			VEXTIO		±50		ppm of FSR/°C
<b>POWER SUPPLY</b>							
ANALOG SUPPLY CURRENT <sup>3</sup>		I <sub>AVDD</sub>			175		mA
DIGITAL SUPPLY CURREN <sup>3T</sup>		I <sub>DVDD</sub>			100		mA
ANALOG SUPPLY CURRENT <sup>4</sup>	Sleep Mode	I <sub>AVDD</sub>			45		mA
POWER DISSIPATION	AV <sub>dd</sub> = 3.3V, DV <sub>dd</sub> = 3.3V	P <sub>D</sub>					
ANALOG AND DIGITAL POWER SUPPLY REJECTION RATIO	AV <sub>dd</sub> = 3.15 to 3.45V	A <sub>PSRR</sub>		-0.5		0.5	%FS <sub>m</sub> WR/V
		D <sub>PSRR</sub>		-0.5		0.5	
<b>LVDS INTERFACE: NODE D[13:0]A; D[13:0]B</b>							
POSITIVE-GOING DIFFERENTIAL INPUT VOLTAGE THRESHOLD	See LVDS min/max threshold voltage table	V <sub>ITH+</sub>			100		mV
NEGATIVE-GOING DIFFERENTIAL INPUT VOLTAGE THRESHOLD		V <sub>ITH-</sub>			-100		
INTERNAL TERMINATION IMPEDANCE		Z <sub>T</sub>		90		132	Ohms
INPUT CAPACITANCE		C <sub>i</sub>			2		pF
<b>CMOS INTERFACE: NODE SLEEP</b>							

TABLE 5. 5675 DC ELECTRICAL CHARACTERISTICS  
 (DVDD = 3.3±10%, AVDD = 3.3±10%, T<sub>A</sub> = -55 TO +125 °C, UNLESS OTHERWISE SPECIFIED)

PARAMETER	TEST CONDITIONS	SYMBLE	SUBGROUPS	MIN	TYP	MAX	UNIT
HIGH-LEVEL INPUT VOLTAGE		V <sub>IH</sub>		2	3.3		V
LOW-LEVEL INPUT VOLTAGE		V <sub>IL</sub>			0	0.8	V
HIGH-LEVEL INPUT CURRENT		I <sub>IH</sub>		-10		10	uA
LOW-LEVEL INPUT CURRENT		I <sub>IL</sub>		-10		10	uA
INPUT CAPACITANCE					2		pF
<b>CLOCK INTERFACE: NODE CLK, CLCKC</b>							
INPUT RESISTANCE	node CLK, CLKC				670		Ohms
INPUT CAPACITANCE	node CLK, CLKC				2		pF
INPUT RESISTANCE	Differential				1.3		Kohms
INPUT CAPACITANCE	Differential				1		pF
<b>TIMING</b>							
INPUT SETUP TIME		t <sub>SU</sub>			1.5		nS
INPUT HOLD TIME		t <sub>H</sub>			0.25		nS
INPUT LATCH PULSE HIGH TIME		T <sub>LPH</sub>			2		nS
DIGITAL DELAY TIME		T <sub>DD</sub>			1		clk

1. Measured Differential at IOU1 and IOU2. 2.5Ohms to AVDD
2. Use an external buffer amplifier with high impedance input drive to drive any external load.
3. Measured at f<sub>CLK</sub> = 400 MSPS and F<sub>OUT</sub> = 70 MHz
4. Measured for 50 Ohms R<sub>I</sub> at IOU1 and IOU2, f<sub>CLK</sub> = 400 MSPS and f<sub>OUT</sub> = 70MHz

TABLE 6. 5675 AC ELECTRICAL CHARACTERISTICS  
(DVDD = 3.3±10%, AVDD = 3.3±10%, T<sub>A</sub> = -55 TO +125 °C, UNLESS OTHERWISE SPECIFIED)

PARAMETER	TEST CONDITIONS	SYMBOL	SUBGROUPS	V <sub>CC</sub> = 3.3V ± 0.3			UNIT
				MIN	TYP	MAX	
<b>ANALOG OUTPUT</b>							
OUTPUT SETTLING TIME	MID-SCALE TRANSITION (CODE 8191-8192)	T <sub>s</sub> (DAC)	9, 10, 11		5		nS
OUTPUT PROPAGATION DELAY		T <sub>PD</sub>	9, 10, 11		1		nS
OUTPUT RISE TIME 10% TO 90%		T <sub>R</sub> (I <sub>OUT</sub> )	9, 10, 11		2		nS
OUTPUT FALL TIME 90% TO 10%			9, 10, 11		2		nS
OUTPUT NOISE	I <sub>OUTFS</sub> = 20mA		9, 10, 11		55		pA/ 2 <sup>^</sup> Hz
	I <sub>OUTFS</sub> = 2mA				30		pA/ 2 <sup>^</sup> Hz
<b>AC LINEARITY</b>							
TOTAL HARMONIC DISTORTION	t <sub>CLK</sub> = 100 MSPS, f <sub>OUT</sub> =20MHZ, T <sub>A</sub> = 25C	THD			72		dBc
	t <sub>CLK</sub> = 160 MSPS, f <sub>OUT</sub> =41MHZ, T <sub>A</sub> = 25C				67		
	t <sub>CLK</sub> = 200 MSPS, f <sub>OUT</sub> =70MHZ, T <sub>A</sub> = 25C				63		
	t <sub>CLK</sub> = 400 MSPS, f <sub>OUT</sub> =20 MHz, T <sub>MIN</sub> to T <sub>MAX</sub>				72		
	t <sub>CLK</sub> = 400 MSPS, f <sub>OUT</sub> =70MHZ, T <sub>A</sub> = 25C				64		
	t <sub>CLK</sub> = 400 MSPS, f <sub>OUT</sub> =140MHZ, T <sub>A</sub> = 25C				58		
SPURIOUS FREE DYNAMIC RANGE TO NYQUIST	t <sub>CLK</sub> = 100 MSPS, f <sub>OUT</sub> =20MHZ, T <sub>A</sub> = 25C	SFDR			77		dBc
	t <sub>CLK</sub> = 160 MSPS, f <sub>OUT</sub> =41MHZ, T <sub>A</sub> = 25C				70		
	t <sub>CLK</sub> = 200 MSPS, f <sub>OUT</sub> =701MHZ, T <sub>A</sub> = 25C				70		
	t <sub>CLK</sub> = 400 MSPS, f <sub>OUT</sub> =20 MHz, T <sub>MIN</sub> to T <sub>MAX</sub>				73		
	t <sub>CLK</sub> = 400 MSPS, f <sub>OUT</sub> =70MHZ, T <sub>A</sub> = 25C				69		
	t <sub>CLK</sub> = 400 MSPS, f <sub>OUT</sub> =140MHZ, T <sub>A</sub> = 25C				58		

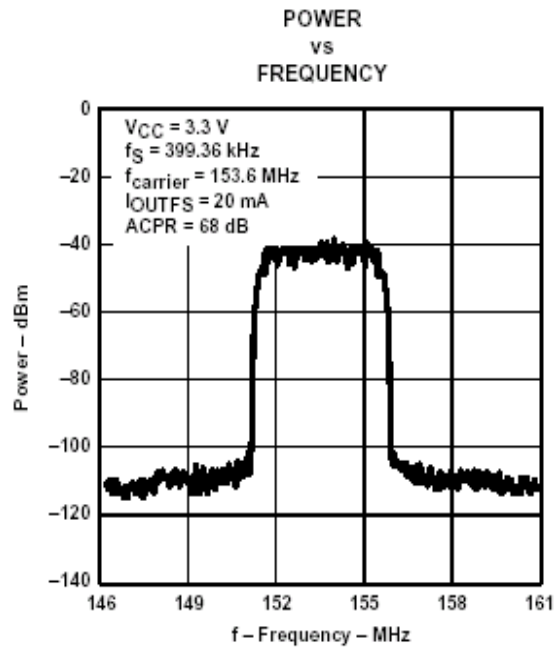
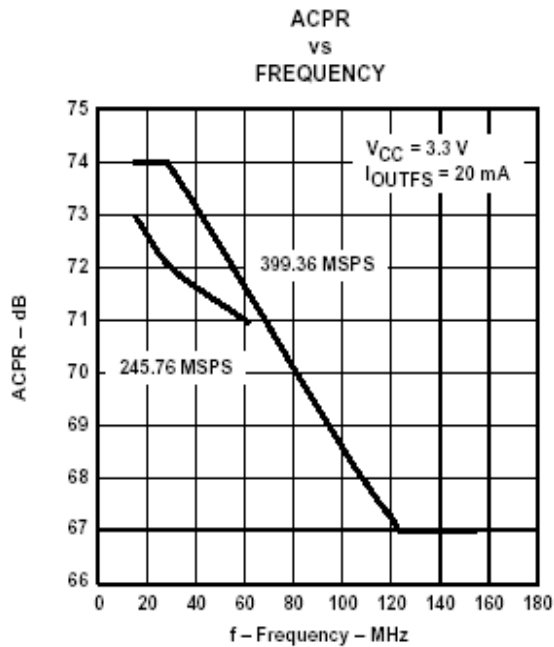
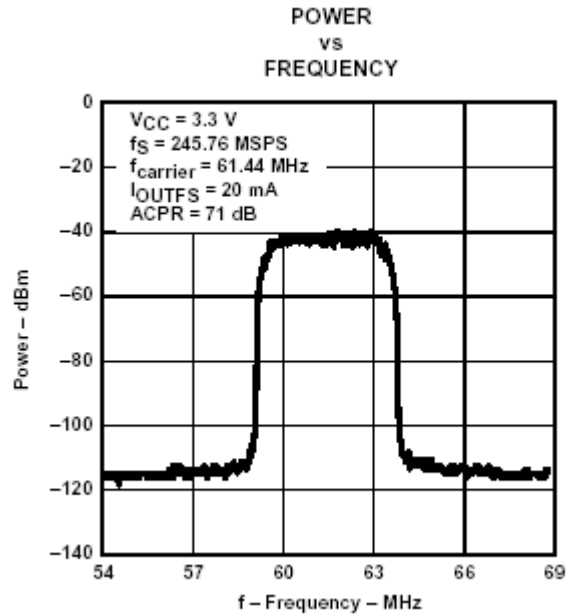
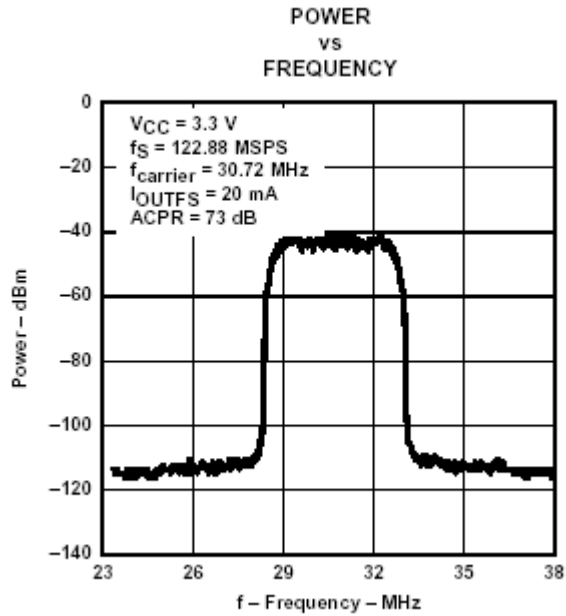
TABLE 6. 5675 AC ELECTRICAL CHARACTERISTICS  
 (DVDD = 3.3±10%, AVDD = 3.3±10%, T<sub>A</sub> = -55 TO +125 °C, UNLESS OTHERWISE SPECIFIED)

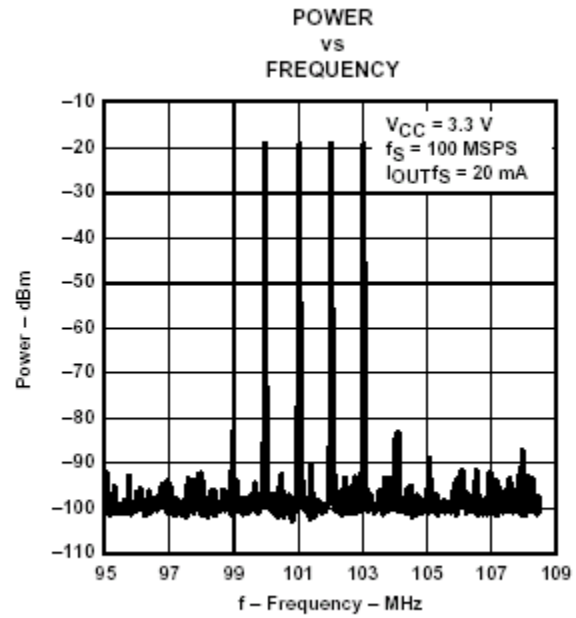
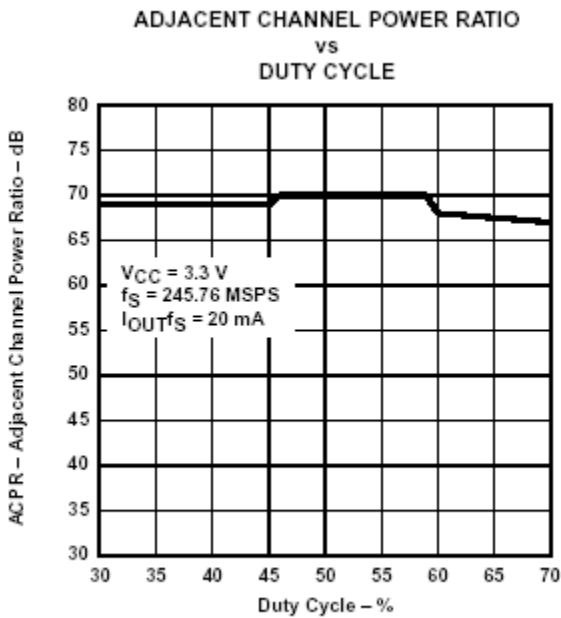
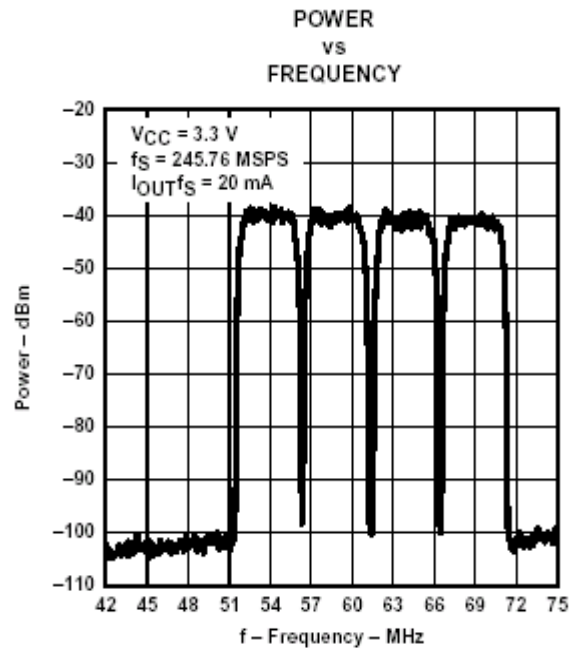
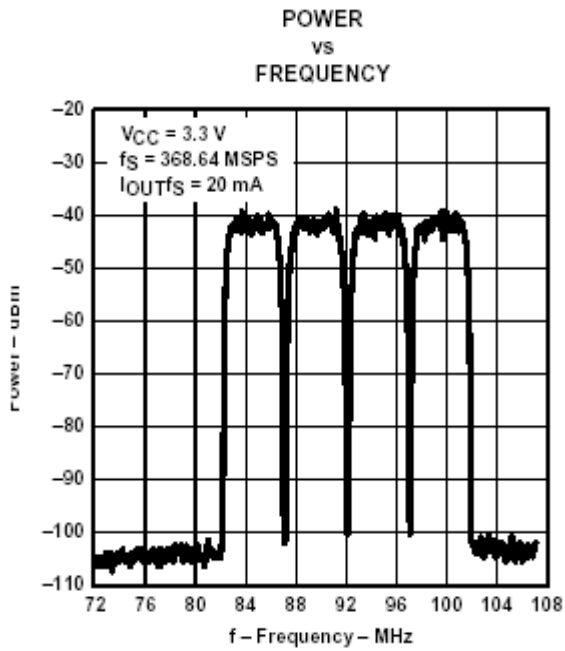
PARAMETER	TEST CONDITIONS	SYMBOL	SUBGROUPS	V <sub>CC</sub> = 3.3V ± 0.3			UNIT
				MIN	TYP	MAX	
SPURIOUS FREE DYNAMIC RANGE WITHIN A WINDOW, 5-MHz SPAN	t <sub>CLK</sub> = 100 MSPS, f <sub>OUT</sub> =20MHz, T <sub>A</sub> = 25C	SFDR			88		dBc
	t <sub>CLK</sub> = 160 MSPS, f <sub>OUT</sub> =41MHz, T <sub>A</sub> = 25C			83			
	t <sub>CLK</sub> = 200 MSPS, f <sub>OUT</sub> =70MHz, T <sub>A</sub> = 25C			80			
	t <sub>CLK</sub> = 400 MSPS, f <sub>OUT</sub> =20 MHz, T <sub>MIN</sub> to T <sub>MAX</sub>			88			
	t <sub>CLK</sub> = 400 MSPS, f <sub>OUT</sub> =70MHz, T <sub>A</sub> = 25C			80			
	t <sub>CLK</sub> = 400 MSPS, f <sub>OUT</sub> =140MHz, T <sub>A</sub> = 25C			73			
ADJACENT CHANNEL POWER RATIO WCDMA WITH 3.84 MHz BW, 5MHz CHANNEL SPACING	f <sub>CLK</sub> =122.8 MSPS, IF=30.72 MHz, T <sub>A</sub> =25C	ACPR			73		dB
	f <sub>CLK</sub> =245.76 MSPS, IF=61.44 MHz, T <sub>A</sub> =25C			71			
	f <sub>CLK</sub> =399.32 MSPS, IF=153.36 MHz, T <sub>A</sub> =25C			68			
TWO-TONE INTERMODULATION TO NYQUIST (EACH TONE AT -6 DBFS)	f <sub>CLK</sub> =400MHz, f <sub>OUT1</sub> =70MHz, f <sub>OUT2</sub> =141MHz, T <sub>A</sub> =25C	IMD			67		dBc
	f <sub>CLK</sub> =400MHz, f <sub>OUT1</sub> =140MHz, f <sub>OUT2</sub> =141MHz, T <sub>A</sub> =25C			63			
FOUR-TONE INTERMODULATION, 15MHz SPAN, MISSING CENTER TONE (EACH TONE AT -6 DBFS)	f <sub>CLK</sub> =400MHz, f <sub>OUT1</sub> =70MHz, f <sub>OUT2</sub> =141MHz, T <sub>A</sub> =25C				72		
	f <sub>CLK</sub> =400MHz, f <sub>OUT1</sub> =140MHz, f <sub>OUT2</sub> =141MHz, T <sub>A</sub> =25C				74		

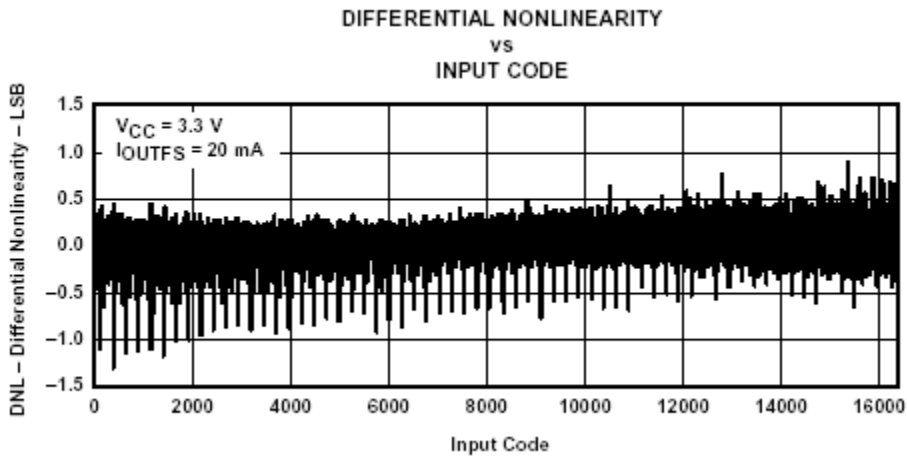
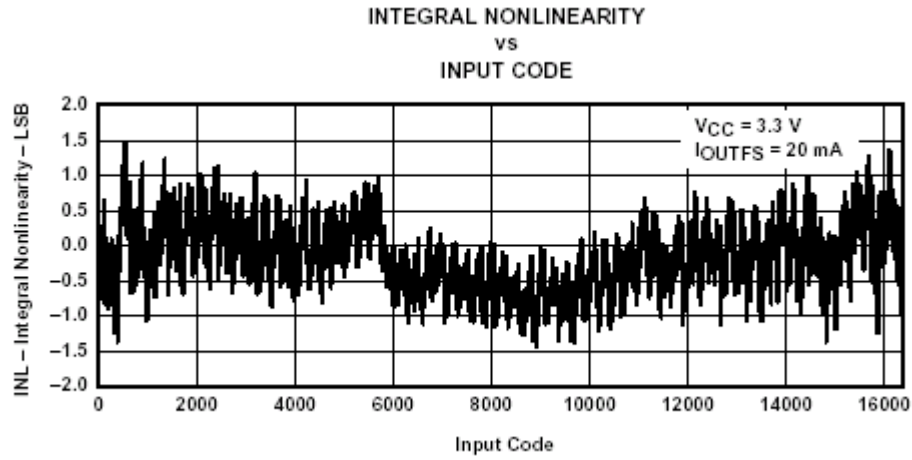
TABLE 7. LVDS INPUT THRESHOLDS AND LOGICAL BIT EQUIVALENT

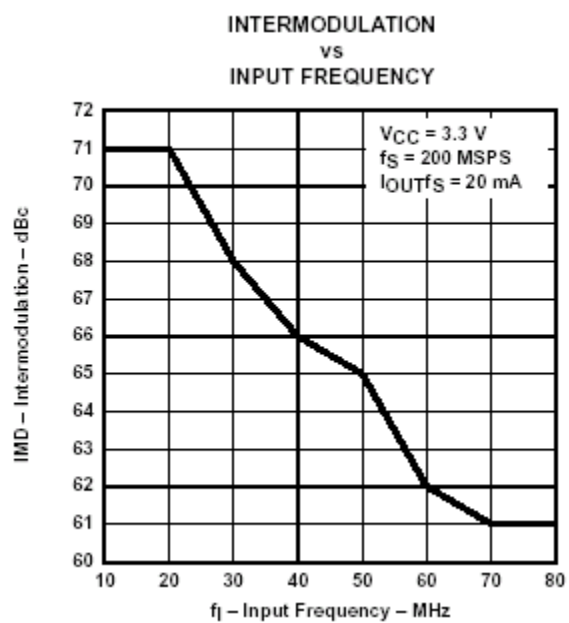
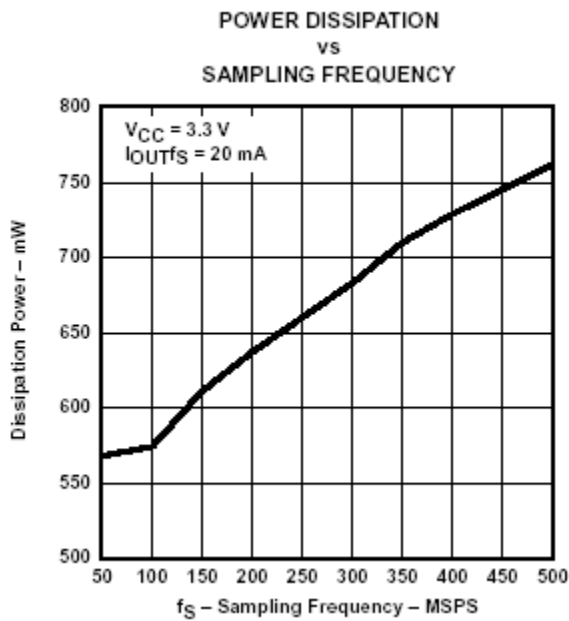
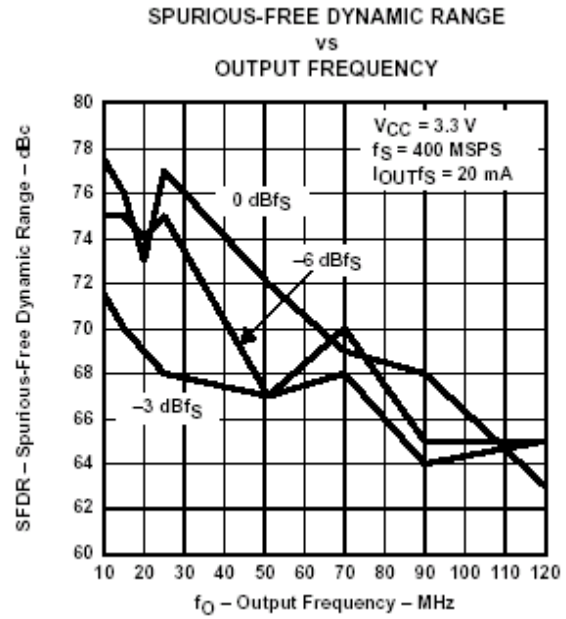
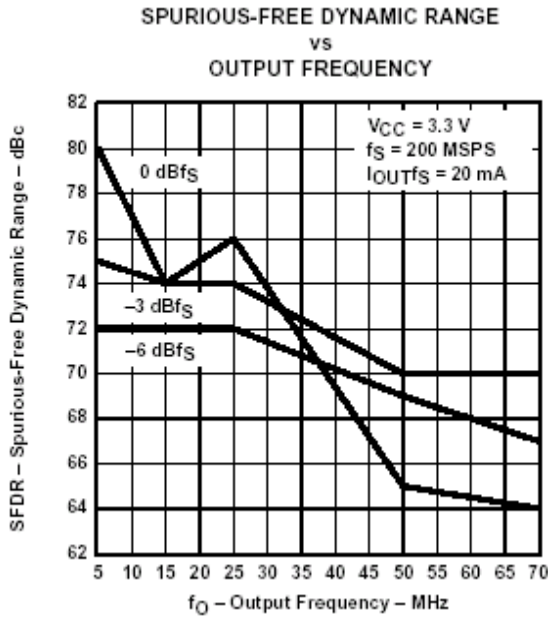
APPIED VOLTAGE		RESULTING DIFFERENTIAL INPUT VOLTAGE	RESULTING COMMON-MODE INPUT VOLTAGE	LOGICAL BIT BINARY EQUIVALENT	COMMENT
$V_A$ [V]	$V_B$ [V]	$V_{A,B}$ [mV]	$V_{COM}$ [V]		
1.25	1.15	200	1.2	1	Operation with minimum differential voltage( $\pm 200$ mV) applied to the complimentary inputs versus common mode range
1.15	1.25	-200	1.2	0	
2.4	2.3	200	1.35	1	
2.3	2.4	-200	2.35	0	
0.1	0	200	0.05	1	
0	0.1	-200	0.05	0	
1.5	0.9	600	1.2	1	Operation with minimum differential voltage( $\pm 600$ mV) applied to the complimentary inputs versus common mode range
0.9	1.5	-600	1.2	0	
2.4	1.8	600	2.1	1	
1.8	2.4	-600	2.1	0	
0.6	0	600	0.3	1	
0	0.6	-600	0.3	0	

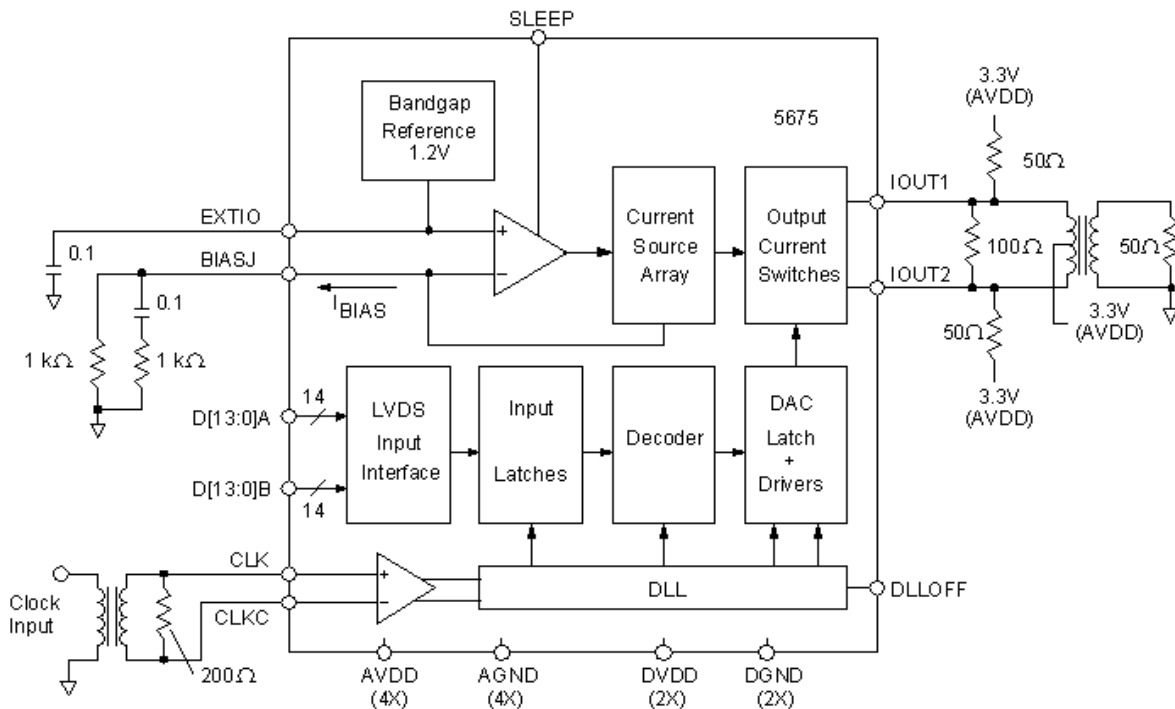
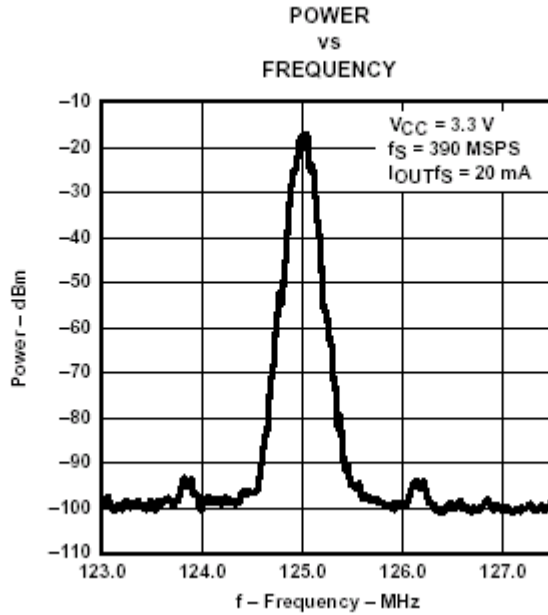




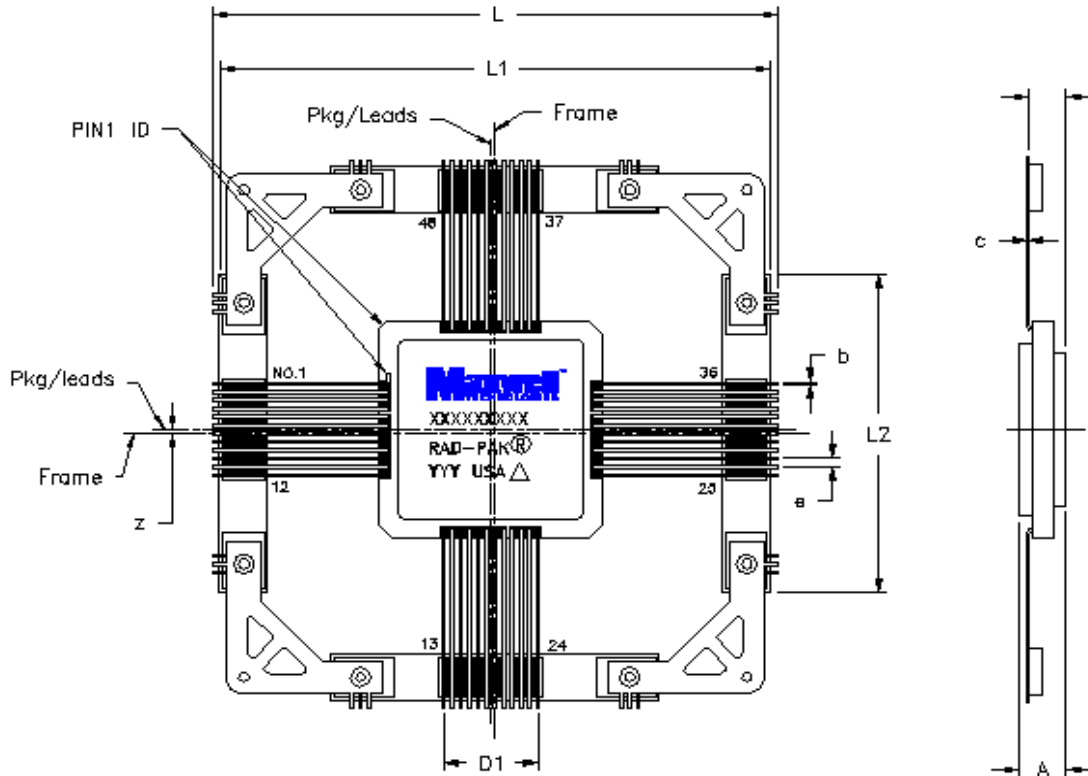








Applications Schematic



48 PIN RAD-PAK® QUAD FLAT PACKAGE

SYMBOL	DIMENSION			
	CENTER LINE	MIN	NOM	MAX
A	--	.121	.135	.149
b	--	.008	.010	.012
c	--	.006	.008	.010
D	PKG/leads	.645	.650	.655
D1	PKG/leads	.270	.275	.280
e	--	--	.025	--
L	Frame		1.645	
L1	Frame	1.585	1.605	1.625
L2	Frame	.945	.956	.965
A1	--	--	.108	--
Z	--	--	.0125	--
N	--		48	

Note: All dimensions in inches

## Important Notice:

These data sheets are created using the chip manufacturer's published specifications. Maxwell Technologies verifies functionality by testing key parameters either by 100% testing, sample testing or characterization.

The specifications presented within these data sheets represent the latest and most accurate information available to date. However, these specifications are subject to change without notice and Maxwell Technologies assumes no responsibility for the use of this information.

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# 14-BIT, 400MSPS DIGITAL-TO-ANALOG Converter

# 5675

## Product Ordering Options

