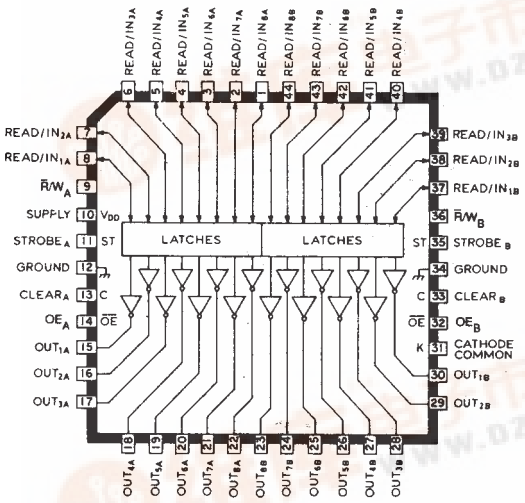
5881

Data Sheet
26180.16

BiMOS II DUAL 8-BIT LATCHED DRIVER WITH READ BACK



Dwg. No. A-14,225

ABSOLUTE MAXIMUM RATINGS

Output Voltage, V_{OUT} . . . . . **20 V**
Output Sustaining Voltage, $V_{CE(sus)}$ . . . **15 V**
Output Current, I_{OUT} . . . . . **50 mA**
Input Voltage Range,
V_{IN} . . . . . **-0.3 V to V_{DD} + 0.3 V**
Logic Supply Voltage, V_{DD} . . . . . **15 V**
Package Power Dissipation,
P_D . . . . . **See Graph**
Operating Temperature Range,
T_A . . . . . **-20°C to +85°C**
Storage Temperature Range,
T_S . . . . . **-55°C to +150°C**

Caution: CMOS devices have input static protection, but are susceptible to damage when exposed to extremely high static electrical charges.

With 16 CMOS data latches (two sets of eight), CMOS control circuitry for each set of latches, and a bipolar saturated driver for each latch, the UCN5881EP provides low-power interface with maximum flexibility. The driver includes thermal shutdown circuitry to protect against damage from high junction temperatures and clamp diodes for inductive load transient suppression.

The CMOS inputs cause minimal circuit loading and are compatible with standard CMOS, PMOS, and NMOS circuits. TTL or DTL circuits may require the use of appropriate pull up resistors. When reading back, each data input will sink 8 mA (if its corresponding latch is low) or source 400 µA (if its corresponding latch is high). The read back feature is for error checking. It allows the system to verify that data has been received and latched.

The bipolar outputs are suitable for use with low-power relays, solenoids, and stepping motors. The very-low output saturation voltage makes this device well-suited for driving LED arrays. The output transistors are capable of sinking 50 mA and will maintain at least 20 V in the OFF state. Outputs may be paralleled for higher current capability.

The UCN5881EP dual 8-bit latched sink driver is rated for operation over the temperature range of -20°C to +85°C and is supplied in a plastic 44-lead chip carrier conforming to the JEDEC MS-007AB outline.

FEATURES

- 4.4 MHz Minimum Data-Input Rate
- Low-Power CMOS Logic
- 20 V, 50 mA (Max.) Outputs
- Transient-Protected Outputs
- Thermal Shutdown Protection
- Low-Profile Leaded Chip Carrier

Always order by complete part number: UCN5881EP .

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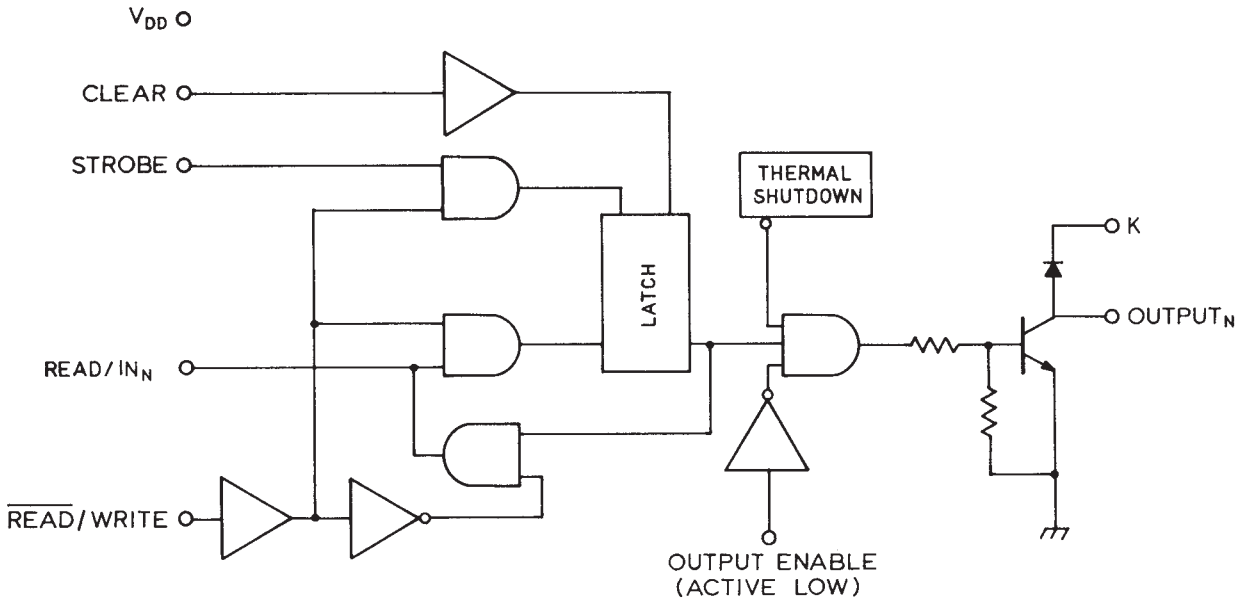
BiMOS II DUAL 8-BIT LATCHED DRIVER

FUNCTIONAL BLOCK DIAGRAM
(1 of 16 Channels)



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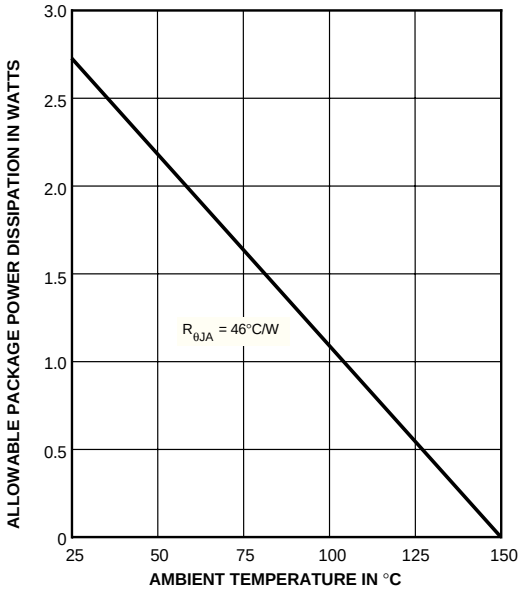

Dwg. GP-025-1A

TRUTH TABLE

Read/In	Strobe	Clear	Output Enable	$\overline{\text{Read}}$/Write	Latch Contents	Output
X	X	X	1	X	X	OFF
0	1	0	0	1	0	OFF
1	1	0	0	1	1	ON
X	0	0	0	1	n-1	n-1
X	X	1	X	X	0	OFF
n	X	0	X	0	n	n

n = Present Latch Contents
n-1 = Previous Latch Contents
X = Irrelevant

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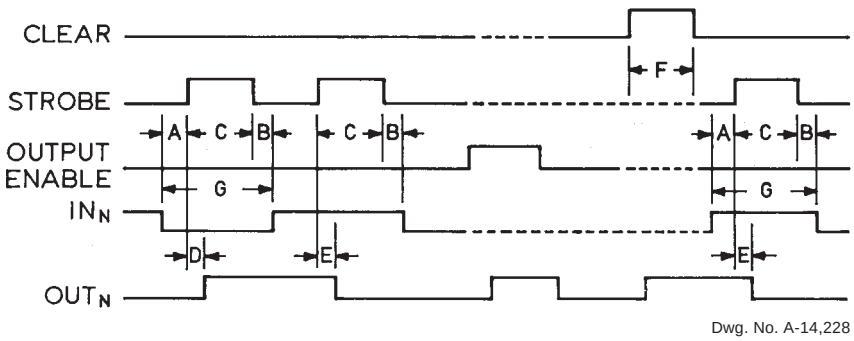
BiMOS II DUAL 8-BIT LATCHED DRIVER

ELECTRICAL CHARACTERISTICS at T_A = 25°C, V_{DD} = 5 V (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output Leakage Current	I_{CEX}	V_{OUT} = 20 V	—	50	µA
Output Saturation Voltage	$V_{CE(SAT)}$	I_{OUT} = 10 mA	—	0.1	V
		I_{OUT} = 25 mA	—	0.5	V
Output Sustaining Voltage	$V_{CE(sus)}$	I_{OUT} = 25 mA, L = 2 mH	15	—	V
Input Voltage	$V_{IN(0)}$		-0.3	0.8	V
	$V_{IN(1)}$		3.5	5.3	V
Input Current	$I_{IN(0)}$	V_{IN} = 0.8 V	—	-10	µA
	$I_{IN(1)}$	V_{IN} = 5 V	—	10	µA
Readback Output Voltage	$V_{OUT(1)}$	I_{OUT} = -400 µA	3.5	—	V
	$V_{OUT(0)}$	I_{OUT} = 5.0 mA	—	0.8	V
Logic Supply Current	I_{DD}	All Drivers ON	—	14	mA
		All Drivers OFF	—	3.0	mA
Clamp Diode Leakage Current	I_R	V_R = 20 V	—	50	µA
Clamp Diode Forward Voltage	V_F	I_F = 50 mA	—	1.5	V



Dwg. No. A-14,228

TIMING CONDITIONS

(V_{DD} = 5.0 V, Logic Levels are V_{DD} and Ground)

A. Minimum Data Active Time Before Strobe Enabled (Data Set-Up Time) . . . . . **50 ns**

B. Minimum Data Active Time After Strobe Disabled (Data Hold Time) . . . . . **50 ns**

C. Minimum Strobe Pulse Width . . . . . **125 ns**

D. Typical Time Between Strobe Activation and Output ON to OFF Transition . . . . . **5 µs**

E. Typical Time Between Strobe Activation and Output OFF to ON Transition . . . . . **500 ns**

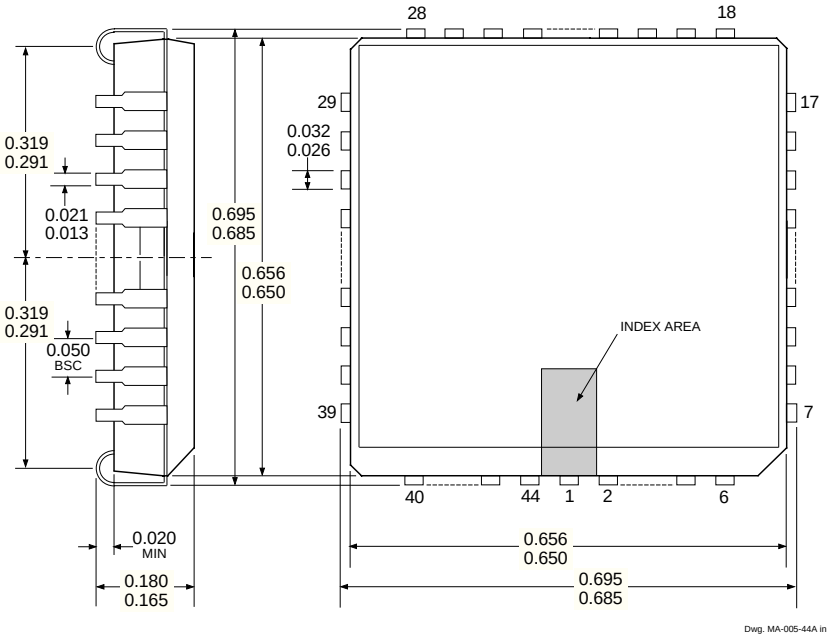
F. Minimum Clear Pulse Width . . . . . **225 ns**

G. Minimum Data Pulse Width . . . . . **225 ns**

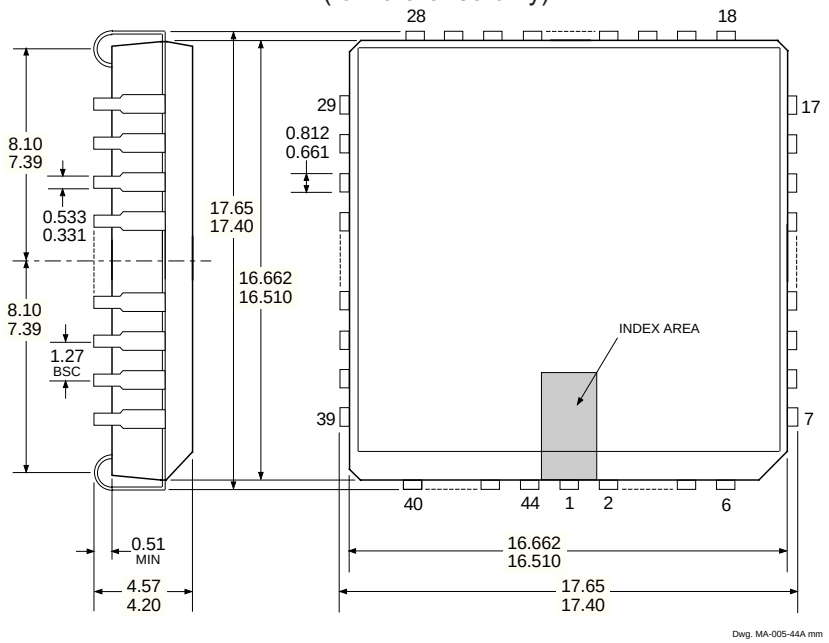
A high on the $\overline{\text{READ}}$/WRITE input allows the circuit to accept data in. Information then present at an input is transferred to its latch when the STROBE is high. A high CLEAR input will set all latches to the output OFF condition regardless of the data or STROBE input levels. A high OUTPUT ENABLE will set all outputs to the OFF condition regardless of any other input conditions. When the OUTPUT ENABLE is low, the outputs depend on the state of their respective latches.

A low on the $\overline{\text{READ}}$/WRITE input will allow the latched data to be read back on the data input lines. Allow a minimum of 750 ns delay (will increase with capacitive loading) before reading back the state of the latches. The read back feature is for error checking applications and allows the system to verify that data has been received and latched.

Dimensions in Inches
(controlling dimensions)



Dimensions in Millimeters
(for reference only)



NOTES: 1. Exact body and lead configuration at vendor's option within limits shown.
2. Lead spacing tolerance is non-cumulative.