DATA SHEET

74LV259
8-bit addressable latch

Product specification
Supersedes data of 1997 Jun 06
IC24 Data Handbook

1998 May 20

Philips
Semiconductors

8-bit addressable latch 74LV259

FEATURES

- Optimized for low voltage applications: 1.0 to 3.6 V
- Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V
- Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25°C
- Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25°C
- Combines demultiplexer and 8-bit latch
- Serial-to-parallel capability
- Output from each storage bit available
- Random (addressable) data entry
- Easily expandable
- Common reset input
- Useful as a 3-to-8 active HIGH decoder
- Output capability: standard
- I_{CC} category: MSI

DESCRIPTION

The 74LV259 is a low-voltage CMOS device and is pin and function compatible with 74HC/HCT259.

The 74LV259 is a high-speed 8-bit addressable latch designed for general purpose storage applications in digital systems. The 74LV259 is a multifunction device capable of storing single-line data in eight addressable latches, and also 3-to-8 decoder and demultiplexer, with active HIGH outputs (Q_0 to Q_7), functions are available. The 74LV259 also incorporate an active LOW common reset ($\overline{MR}$) for resetting all latches, as well as an active LOW enable input ($\overline{LE}$). The 74LV259 has four modes of operation as shown in the mode select table. In the addressable latch mode, data on the data line (D) is written into the addressed latch. The addressed latch will follow the data input with all non-addressed latches remaining in their previous states. In the memory mode, all latches remain in their previous states and are unaffected by the data or address inputs.

In the 3-to-8 decoding or demultiplexing mode, the addressed output follows the state of the D input with all other outputs in the LOW state. In the reset mode all outputs are LOW and unaffected by the address (A_0 to A_2) and date (D) input. When operating the 74LV259 as an addressable latch, changing more than one bit of address could impose a transient-wrong address. Therefore, this should only be done while in the memory mode. The mode select table summarizes the operations of the 74LV259.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay D, A_n to Q_n $\overline{LE}$ to Q_n $\overline{MR}$ to Q_n	C_L = 15 pF; V_{CC} = 3.3 V	 17 16 14	ns
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per latch	V_I = GND to V_{CC}[1]	19	pF

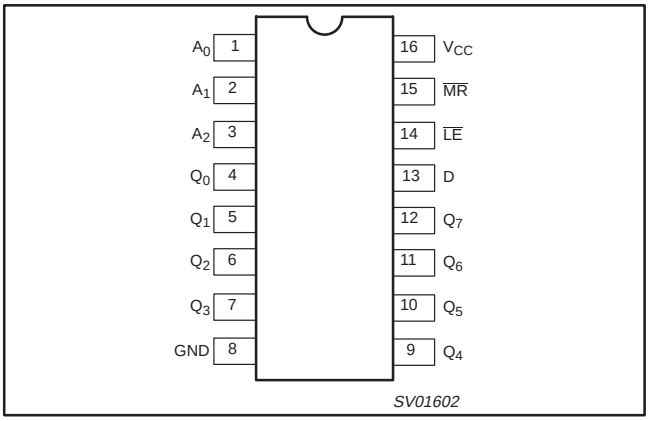
NOTE:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
16-Pin Plastic DIL	–40°C to +125°C	74LV259 N	74LV259 N	SOT38-4
16-Pin Plastic SO	–40°C to +125°C	74LV259 D	74LV259 D	SOT109-1
16-Pin Plastic SSOP Type II	–40°C to +125°C	74LV259 DB	74LV259 DB	SOT338-1
16-Pin Plastic TSSOP Type I	–40°C to +125°C	74LV259 PW	74LV259PW DH	SOT403-1

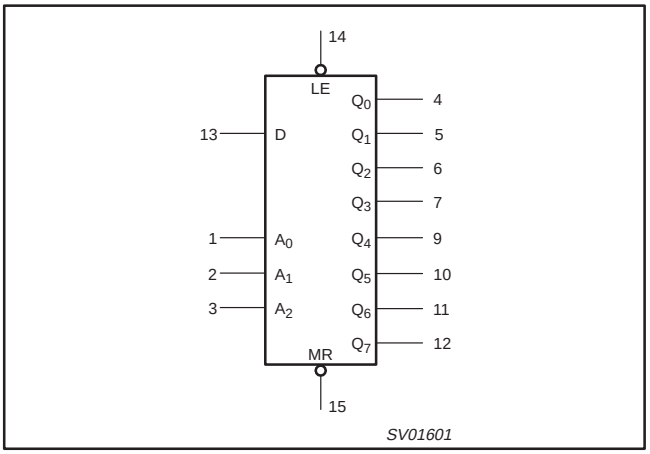
PIN CONFIGURATION



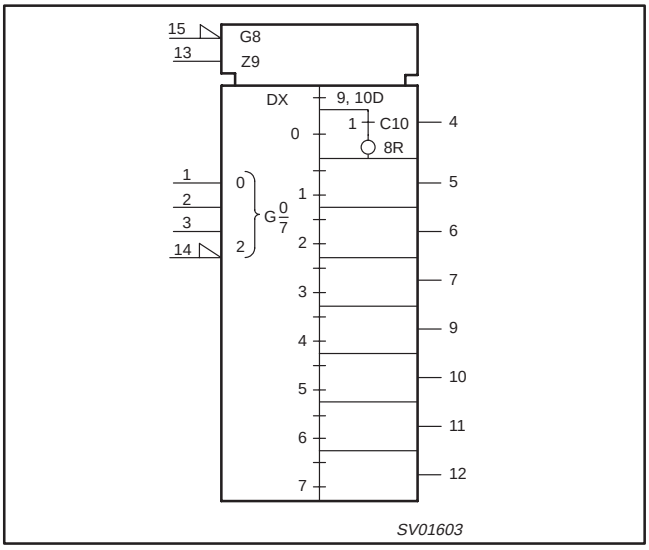
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1, 2, 3	A_0 to A_2	Address inputs
4, 5, 6, 7, 9, 10, 11, 12	Q_0 to Q_7	Latch outputs
8	GND	Ground (0 V)
13	D	Data input
14	$\overline{LE}$	Latch enable input (active LOW)
15	$\overline{MR}$	Conditional reset input (active LOW)
16	V_{CC}	Positive supply voltage

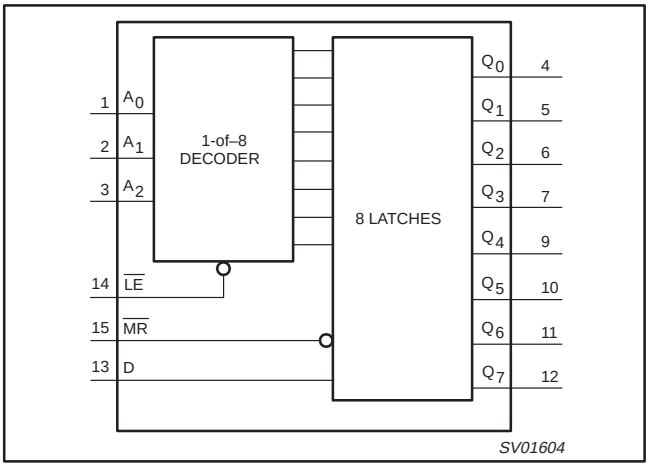
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



FUNCTIONAL DIAGRAM



MODE SELECT TABLE

$\overline{LE}$	$\overline{MR}$	MODE
L	H	Addressable latch
H	H	Memory
L	L	Active HIGH 8-channel demultiplexer
H	L	Reset

FUNCTION TABLE

OPERATING MODES	INPUTS						OUTPUTS							
	$\overline{MR}$	$\overline{LE}$	D	A_0	A_1	A_2	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7
Master reset	L	H	X	X	X	X	L	L	L	L	L	L	L	L
Demultiplex (active HIGH) decoder (when D = H)	L	L	d	L	L	L	Q=d	L	L	L	L	L	L	L
	L	L	d	H	L	L	L	Q=d	L	L	L	L	L	L
	L	L	d	L	H	L	L	L	Q=d	L	L	L	L	L
	L	L	d	H	H	L	L	L	L	Q=d	L	L	L	L
	L	L	d	L	L	H	L	L	L	L	Q=d	L	L	L
	L	L	d	H	L	H	L	L	L	L	L	Q=d	L	L
	L	L	d	L	H	H	L	L	L	L	L	L	Q=d	L
	L	L	d	H	H	H	L	L	L	L	L	L	L	Q=d
Store (do nothing)	H	H	X	X	X	X	q0	q1	q2	q3	q4	q5	q6	q7
Addressable latch	H	L	d	L	L	L	Q=d	q1	q2	q3	q4	q5	q6	q7
	H	L	d	H	L	L	q0	Q=d	q2	q3	q4	q5	q6	q7
	H	L	d	L	H	L	q0	q1	Q=d	q3	q4	q5	q6	q7
	H	L	d	H	H	L	q0	q1	q2	Q=d	q4	q5	q6	q7
	H	L	d	L	L	H	q0	q1	q2	q3	Q=d	q5	q6	q7
	H	L	d	H	L	H	q0	q1	q2	q3	q4	Q=d	q6	q7
	H	L	d	L	H	H	q0	q1	q2	q3	q4	q5	Q=q	q7
	H	L	d	H	H	H	q0	q1	q2	q3	q4	q5	q6	Q=d

NOTES:
H = HIGH voltage level
L = LOW voltage level
X = don't care
d = HIGH or LOW data one set-up time prior to the LOW-to-HIGH $\overline{LE}$ transition
q = lower case letters indicate the state of the referenced output established during the last cycle established during the last cycle in which it was addressed or cleared

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	DC supply voltage	See Note 1	1.0	3.3	3.6	V
V_I	Input voltage		0	–	V_{CC}	V
V_O	Output voltage		0	–	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics	–40 –40		+85 +125	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.0V to 2.0V V_{CC} = 2.0V to 2.7V V_{CC} = 2.7V to 3.6V	– – –	– – –	500 200 100	ns/V

NOTE:
1. The LV is guaranteed to function down to V_{CC} = 1.0V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2V to V_{CC} = 5.5V.

ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
$\pm I_{IK}$	DC input diode current	$V_I < –0.5$ or $V_I > V_{CC} + 0.5V$	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < –0.5$ or $V_O > V_{CC} + 0.5V$	50	mA
$\pm I_O$	DC output source or sink current – standard outputs	$–0.5V < V_O < V_{CC} + 0.5V$	25	mA
$\pm I_{GND}$, $\pm I_{CC}$	DC V_{CC} or GND current for types with – standard outputs		50	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package – plastic DIL – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: –40 to +125°C above +70°C derate linearly with 12 mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 750 500 400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP[1]	MAX	MIN	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2 V	0.9			0.9		V
		V_{CC} = 2.0 V	1.4			1.4		
		V_{CC} = 2.7 to 3.6 V	2.0			2.0		
V_{IL}	LOW level Input voltage	V_{CC} = 1.2 V			0.3		0.3	V
		V_{CC} = 2.0 V			0.6		0.6	
		V_{CC} = 2.7 to 3.6 V			0.8		0.8	
V_{OH}	HIGH level output voltage; all outputs	V_{CC} = 1.2 V; $V_I = V_{IH}$ or V_{IL}; $–I_O$ = 100µA		1.2				V
		V_{CC} = 2.0 V; $V_I = V_{IH}$ or V_{IL}; $–I_O$ = 100µA	1.8	2.0		1.8		
		V_{CC} = 2.7 V; $V_I = V_{IH}$ or V_{IL}; $–I_O$ = 100µA	2.5	2.7		2.5		
		V_{CC} = 3.0 V; $V_I = V_{IH}$ or V_{IL}; $–I_O$ = 100µA	2.8	3.0		2.8		
V_{OH}	HIGH level output voltage; STANDARD outputs	V_{CC} = 3.0 V; $V_I = V_{IH}$ or V_{IL}; $–I_O$ = 6mA	2.40	2.82		2.20		V
V_{OL}	LOW level output voltage; all outputs	V_{CC} = 1.2 V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0				V
		V_{CC} = 2.0 V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 2.7 V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 3.0 V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
V_{OL}	LOW level output voltage; STANDARD outputs	V_{CC} = 3.0 V; $V_I = V_{IH}$ or V_{IL}; I_O = 6mA		0.25	0.40		0.50	V

DC ELECTRICAL CHARACTERISTICS (Continued)

Over recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP[1]	MAX	MIN	MAX	
I_I	Input leakage current	V_{CC} = 3.6 V; V_I = V_{CC} or GND			1.0		1.0	µA
I_{CC}	Quiescent supply current; MSI	V_{CC} = 3.6 V; V_I = V_{CC} or GND; I_O = 0			20.0		160	µA
ΔI_{CC}	Additional quiescent supply current per input	V_{CC} = 2.7 V to 3.6 V; V_I = V_{CC} – 0.6 V			500		850	µA

NOTE:
1. All typical values are measured at T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0V; $t_r = t_f \leq 2.5$ns; C_L = 50pF; R_L = 1KΩ

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS					UNIT
				–40 to +85 °C			–40 to +125 °C		
			V_{CC}(V)	MIN	TYP[1]	MAX	MIN	MAX	
t_{PHL}/t_{PLH}	Propagation delay D to Q_n	Figure 2	1.2		105				ns
			2.0		36	49		61	
			2.7		26	36		45	
			3.0 to 3.6		20[2]	29		36	
t_{PHL}/t_{PLH}	Propagation delay A_n to Q_n	Figure 3	1.2		105				ns
			2.0		36	49		61	
			2.7		26	36		45	
			3.0 to 3.6		20[2]	29		36	
t_{PHL}/t_{PLH}	Propagation delay $\overline{LE}$ to Q_n	Figure 1	1.2		100				ns
			2.0		34	48		60	
			2.7		25	35		44	
			3.0 to 3.6		19[2]	28		35	
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	Figure 4	1.2		90				ns
			2.0		31	43		53	
			2.7		23	31		39	
			3.0 to 3.6		17[2]	25		31	
t_w	$\overline{LE}$ pulse width HIGH or LOW	Figure 1	2.0	34	10		41		ns
			2.7	25	8		30		
			3.0 to 3.6	20	6[2]		24		
t_w	$\overline{MR}$ pulse width LOW	Figure 4	2.0	34	10		41		ns
			2.7	25	8		30		
			3.0 to 3.6	20	6[2]		24		
t_{su}	Set-up time D, A_n to $\overline{LE}$	Figure 5 and 6	1.2		35				ns
			2.0	24	12		29		
			2.7	18	9		21		
			3.0 to 3.6	14	7[2]		17		
t_h	Hold time D to $\overline{LE}$	Figure 5	1.2		–30				ns
			2.0	5	–10		5		
			2.7	5	–8		5		
			3.0 to 3.6	5	–6[2]		5		

AC CHARACTERISTICS (Continued)

GND = 0V; $t_r = t_f \leq 2.5$ns; $C_L = 50$pF; $R_L = 1K\Omega$

SYMBOL	PARAMETER	WAVEFORM	CONDITION	–40 to +85 °C			–40 to +125 °C		UNIT
			V_{CC}(V)	MIN	TYP[1]	MAX	MIN	MAX	
t_h	Hold time A_n to $\overline{LE}$	Figure 6	1.2		–20				ns
			2.0	5	–7		5		
			2.7	5	–5		5		
			3.0 to 3.6	5	–4[2]		5		

NOTES:
1. Unless otherwise stated, all typical values are measured at $T_{amb} = 25°C$
2. Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

$V_M = 1.5$ V at $V_{CC} \geq 2.7$ V and ≤ 3.6V;
$V_M = 0.5 \times V_{CC}$ at $V_{CC} < 2.7$ V and ≥ 4.5 V.
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

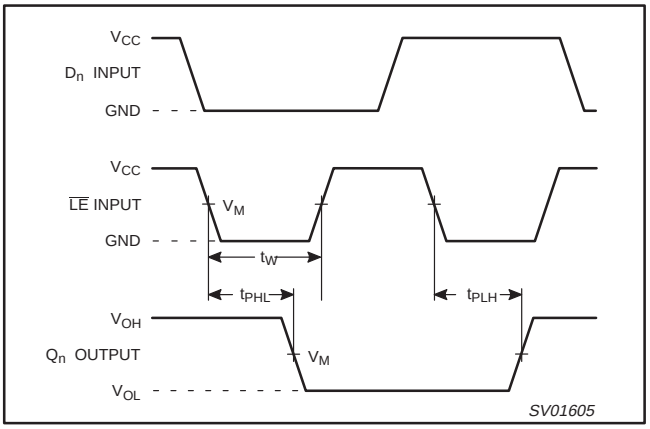


Figure 1. Enable input ($\overline{LE}$) to output (Q_n) propagation delays and the enable input pulse width.

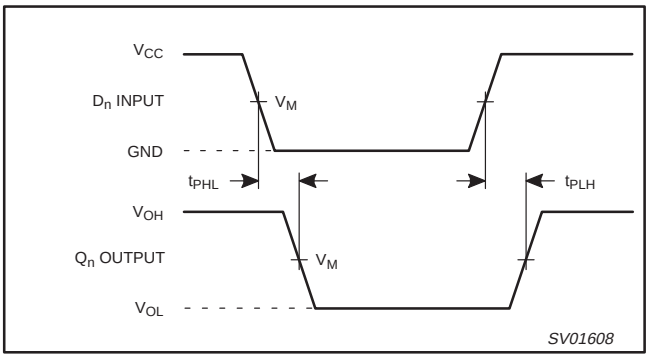


Figure 2. Data input (D) to output (Q_n) propagation delays.

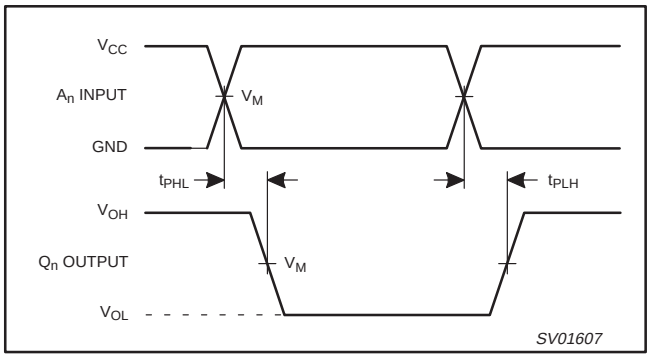


Figure 3. Address inputs (A_n) to output (Q_n) propagation delays.

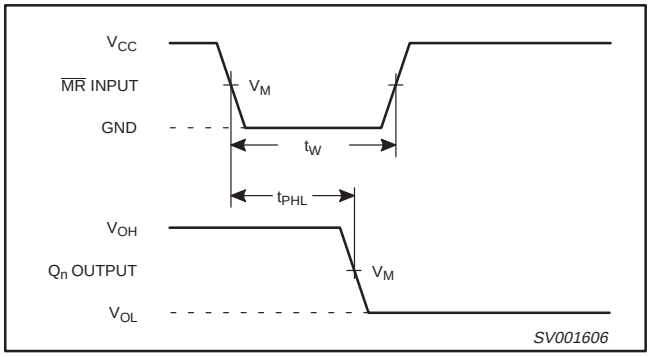


Figure 4. Conditional reset input ($\overline{MR}$) to output (Q_n) propagation delays.

AC WAVEFORMS (Continued)

V_M = 1.5 V at $V_{CC} \geq$ 2.7 V and $\leq$ 3.6V;
$V_M = 0.5 \times V_{CC}$ at $V_{CC} <$ 2.7 V and $\geq$ 4.5 V.
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

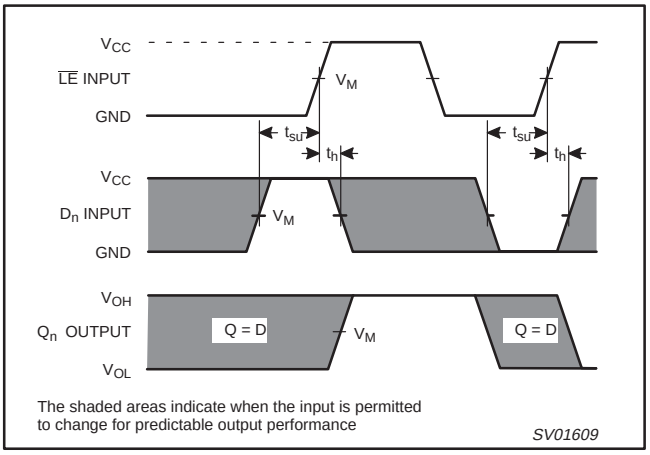


Figure 5. Data set-up and hold times for D input to $\overline{LE}$ input.

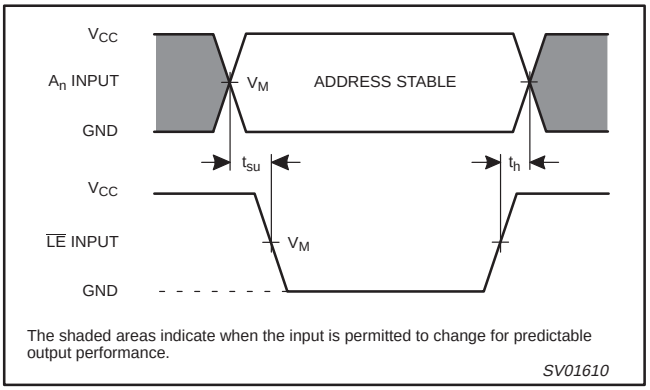


Figure 6. Address set-up and hold times for A_n inputs to $\overline{LE}$ input.

TEST CIRCUIT

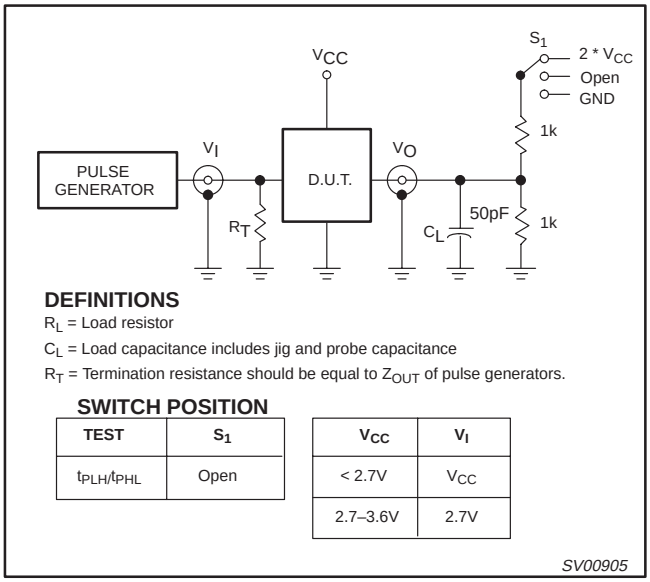
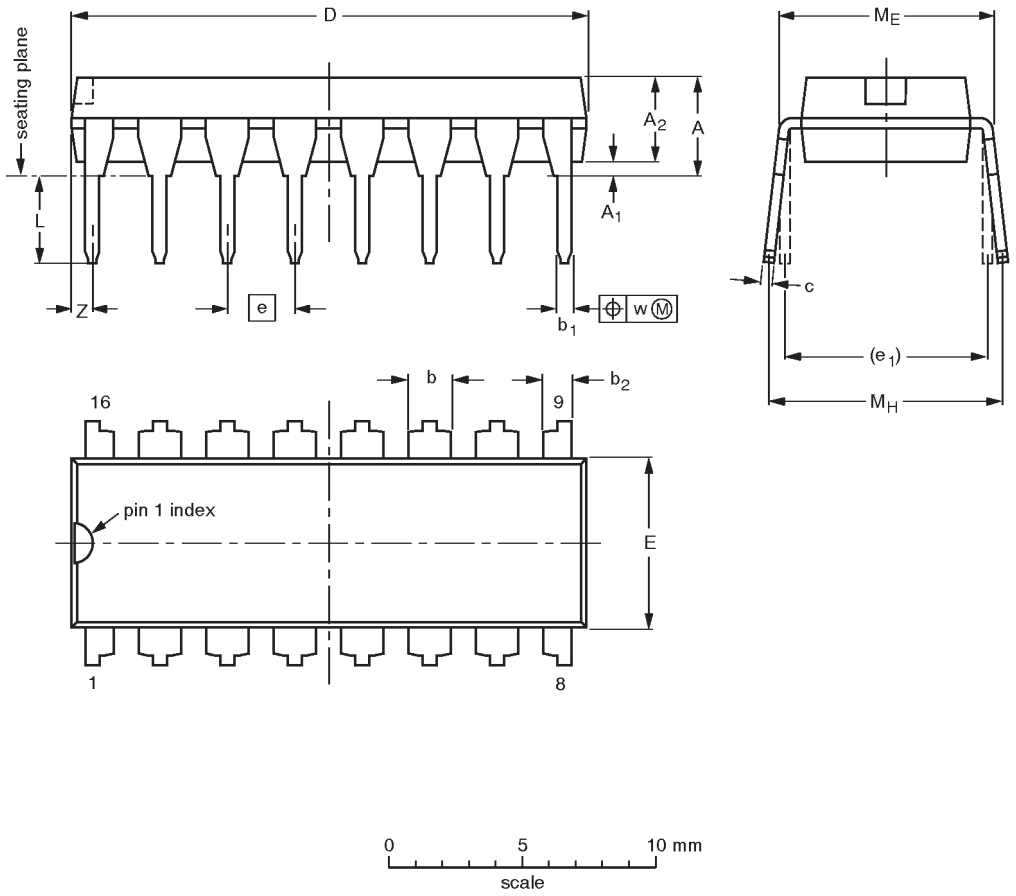


Figure 7. Load circuitry for switching times.

DIP16: plastic dual in-line package; 16 leads (300 mil) SOT38-4



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

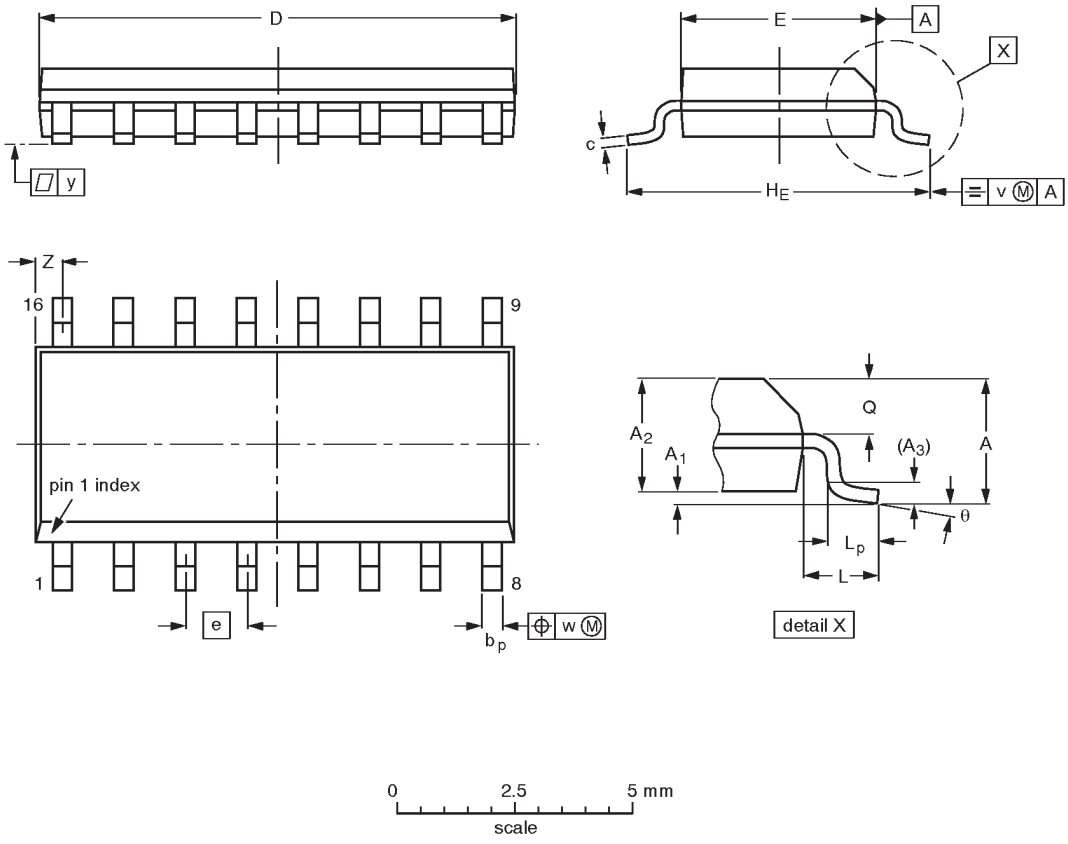
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-4						~~92-11-17~~ 95-01-14

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

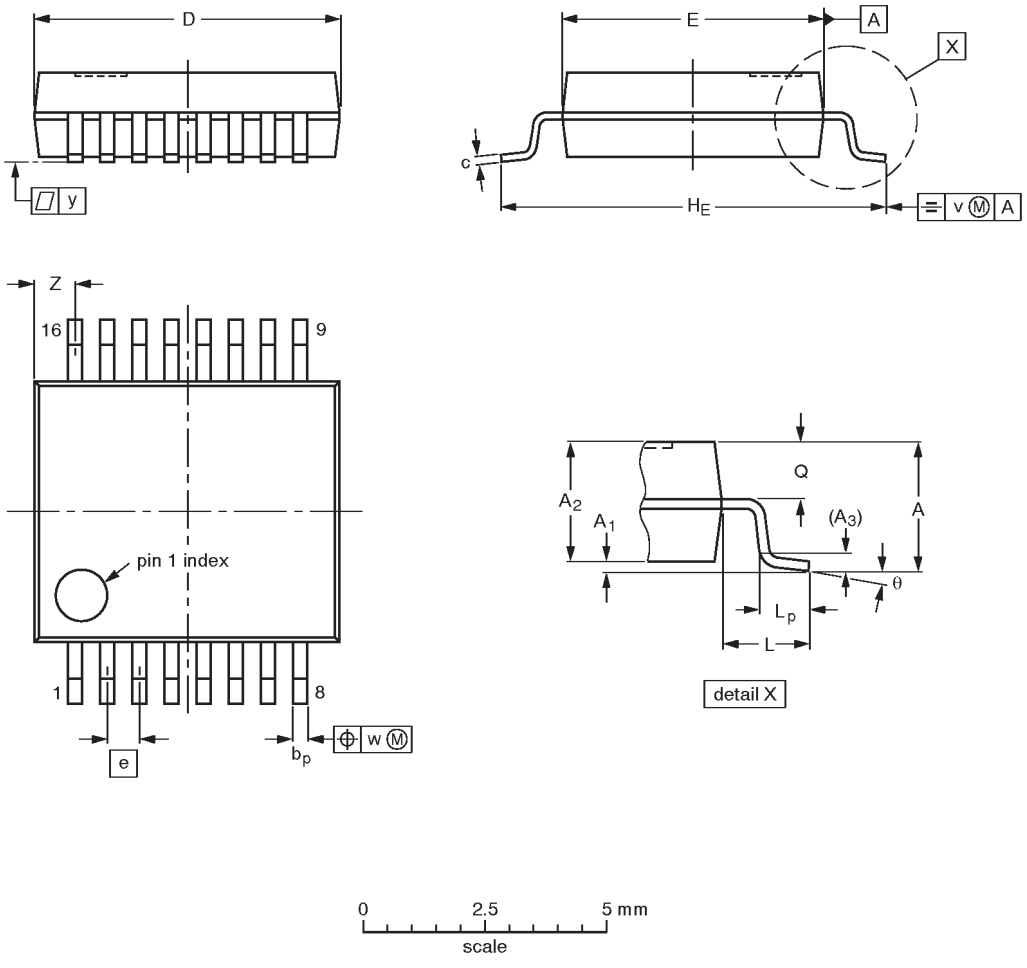
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.0098 0.0039	0.057 0.049	0.01	0.019 0.014	0.0098 0.0075	0.39 0.38	0.16 0.15	0.050	0.24 0.23	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07S	MS-012AC				~~91-08-13~~ 95-01-23

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm **SOT338-1**



DIMENSIONS (mm are the original dimensions)

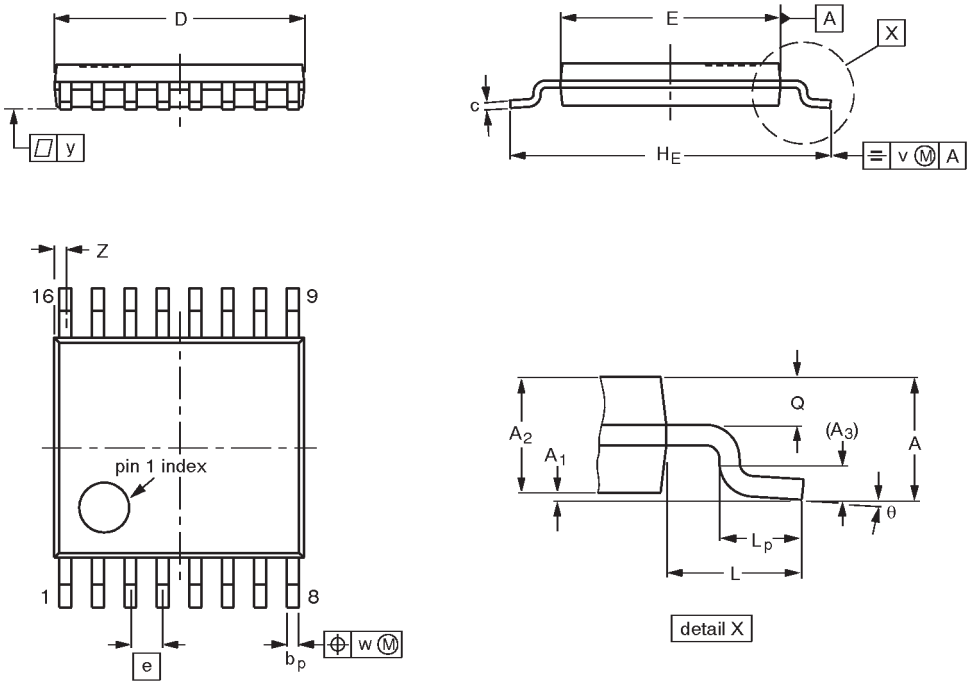
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8° 0°

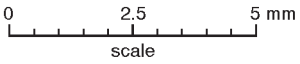
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT338-1		MO-150AC				~~94-01-14~~ 95-02-04

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT403-1		MO-153				~~94-07-12~~ 95-04-04

NOTES

DEFINITIONS

Data Sheet Identification	Product Status	Definition
Objective Specification	Formative or in Design	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	Preproduction Product	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	Full Production	This data sheet contains Final Specifications. Philips Semiconductors reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product.

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