

- **8-Bit Parallel-Out Storage Register Performs Serial-to-Parallel Conversion With Storage**
- **Asynchronous Parallel Clear**
- **Active-High Decoder**
- **Enable Input Simplifies Expansion**
- **Expandable for n-Bit Applications**
- **Four Distinct Functional Modes**
- **Package Options Include Plastic Small-Outline (D), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

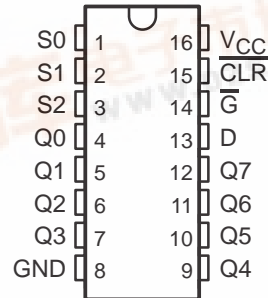
**description**

These 8-bit addressable latches are designed for general-purpose storage applications in digital systems. Specific uses include working registers, serial-holding registers, and active-high decoders or demultiplexers. They are multifunctional devices capable of storing single-line data in eight addressable latches, and being a 1-of-8 decoder or demultiplexer with active-high outputs.

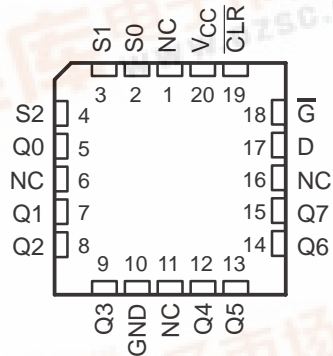
Four distinct modes of operation are selectable by controlling the clear ( $\overline{\text{CLR}}$ ) and enable ( $\overline{\text{G}}$ ) inputs. In the addressable-latch mode, data at the data-in terminal is written into the addressed latch. The addressed latch follows the data input with all unaddressed latches remaining in their previous states. In the memory mode, all latches remain in their previous states and are unaffected by the data or address inputs. To eliminate the possibility of entering erroneous data in the latches,  $\overline{\text{G}}$  should be held high (inactive) while the address lines are changing. In the 1-of-8 decoding or demultiplexing mode, the addressed output follows the level of the D input with all other outputs low. In the clear mode, all outputs are low and unaffected by the address and data inputs.

The SN54HC259 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74HC259 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

SN54HC259 . . . J OR W PACKAGE  
 SN74HC259 . . . D, N, OR PW PACKAGE  
 (TOP VIEW)



SN54HC259 . . . FK PACKAGE  
 (TOP VIEW)



NC – No internal connection

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



# SN54HC259, SN74HC259

## 8-BIT ADDRESSABLE LATCHES

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### Function Tables

#### FUNCTION

INPUTS		OUTPUT OF ADDRESSED LATCH	EACH OTHER OUTPUT	FUNCTION
$\overline{\text{CLR}}$	$\overline{\text{G}}$			
H	L	D	$Q_iO$	Addressable latch
H	H	$Q_iO$	$Q_iO$	Memory
L	L	D	L	8-line demultiplexer
L	H	L	L	Clear

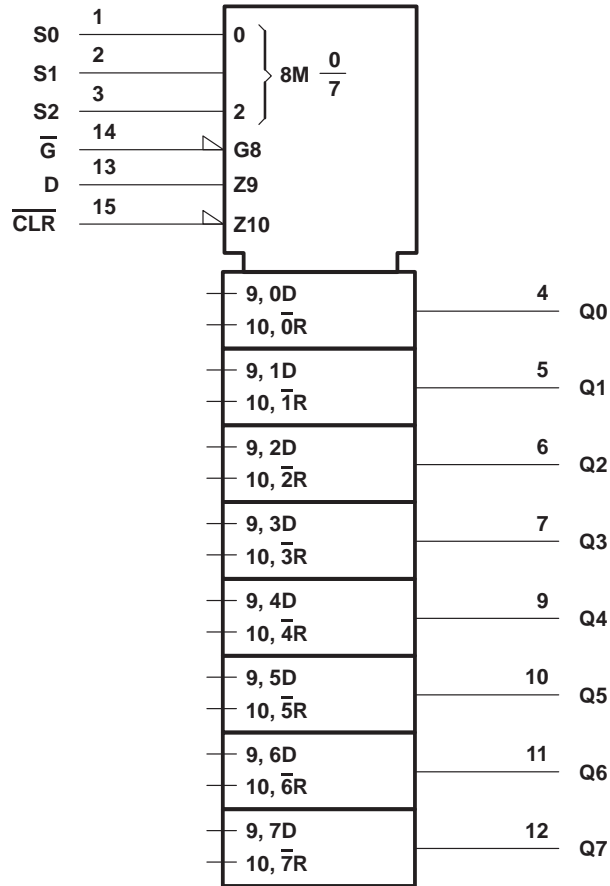
#### LATCH SELECTION

SELECT INPUTS			LATCH ADDRESSED
S2	S1	S0	
L	L	L	0
L	L	H	1
L	H	L	2
L	H	H	3
H	L	L	4
H	L	H	5
H	H	L	6
H	H	H	7

# SN54HC259, SN74HC259 8-BIT ADDRESSABLE LATCHES

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## logic symbol†

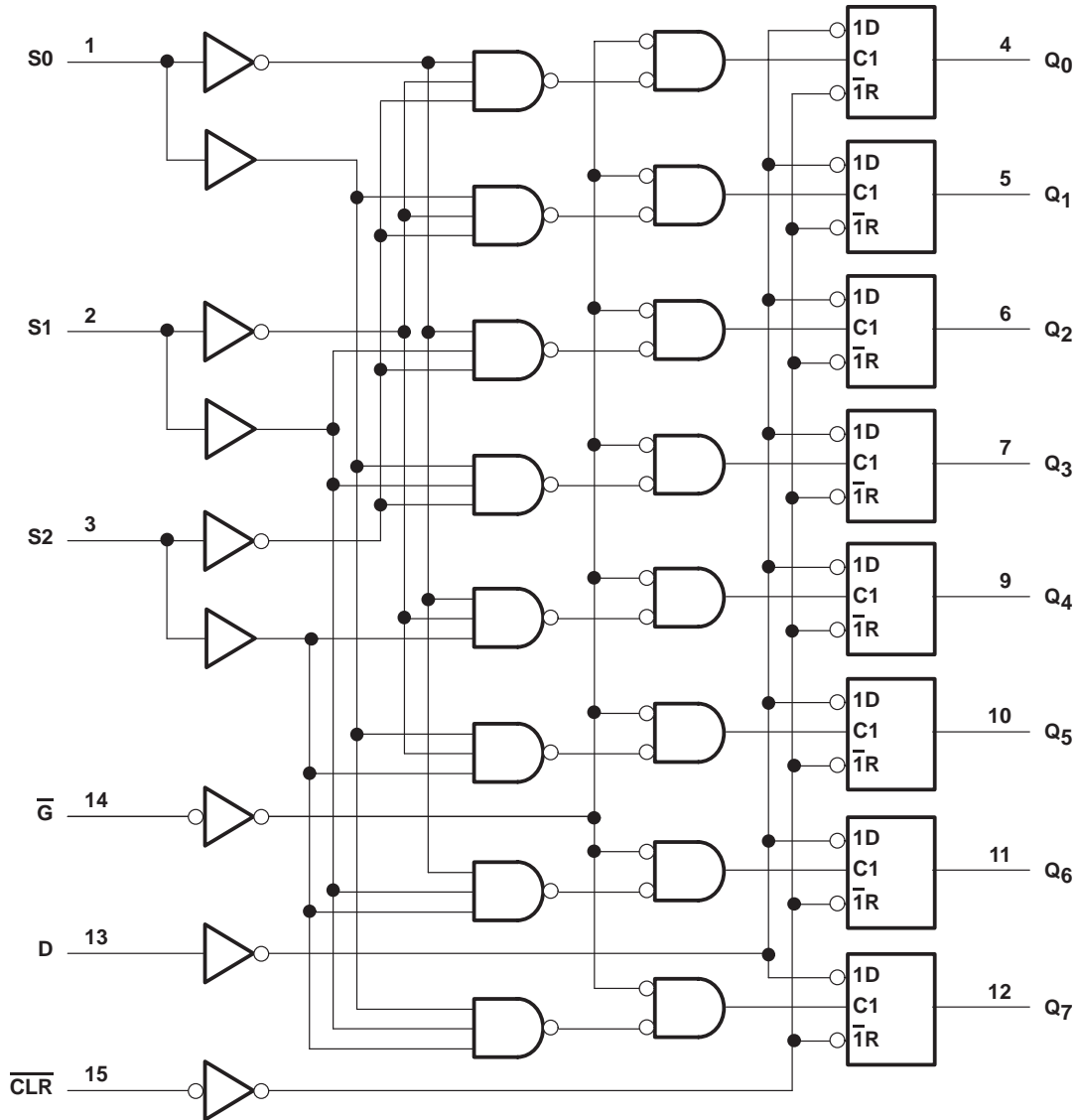


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.  
Pin numbers shown are for the D, J, N, PW, and W packages.

# SN54HC259, SN74HC259 8-BIT ADDRESSABLE LATCHES

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## logic diagram (positive logic)



Pin numbers shown are for the D, J, N, PW, and W packages.

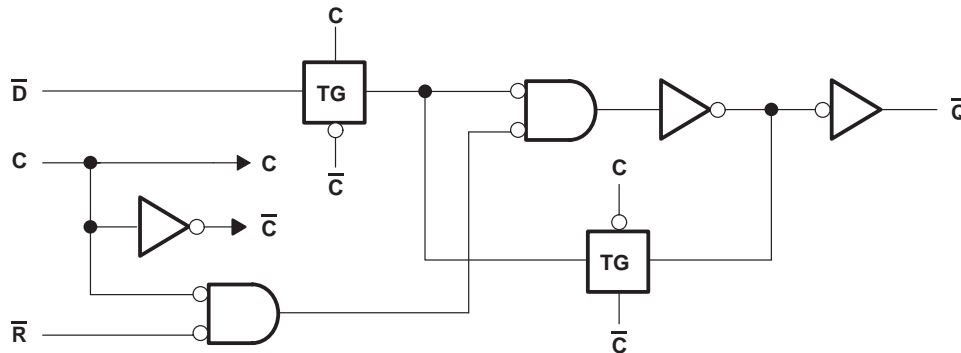
# SN54HC259, SN74HC259 8-BIT ADDRESSABLE LATCHES

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## logic symbol, each internal latch



## logic diagram, each internal latch (positive logic)



## absolute maximum ratings over operating free-air temperature range†

Supply voltage range, $V_{CC}$ .....	-0.5 V to 7 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) (see Note 1) .....	$\pm 20$ mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) (see Note 1) .....	$\pm 20$ mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....	$\pm 25$ mA
Continuous current through $V_{CC}$ or GND .....	$\pm 50$ mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package .....	113°C/W
N package .....	78°C/W
PW package .....	149°C/W
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

# SN54HC259, SN74HC259

## 8-BIT ADDRESSABLE LATCHES

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### recommended operating conditions

		SN54HC259			SN74HC259			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	2	5	6	2	5	6	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 2 V	1.5		1.5		V	
		V <sub>CC</sub> = 4.5 V	3.15		3.15			
		V <sub>CC</sub> = 6 V	4.2		4.2			
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 2 V	0	0.5	0	0.5	V	
		V <sub>CC</sub> = 4.5 V	0	1.35	0	1.35		
		V <sub>CC</sub> = 6 V	0	1.8	0	1.8		
V <sub>I</sub>	Input voltage	0	V <sub>CC</sub>		0	V <sub>CC</sub>		V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>		0	V <sub>CC</sub>		V
t <sub>t</sub>	Input transition (rise and fall) time	V <sub>CC</sub> = 2 V	0	1000	0	1000	ns	
		V <sub>CC</sub> = 4.5 V	0	500	0	500		
		V <sub>CC</sub> = 6 V	0	400	0	400		
T <sub>A</sub>	Operating free-air temperature	-55	125		-40	85		°C

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HC259		SN74HC259		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -20 μA	2 V	1.9	1.998	1.9	1.9	V		
			4.5 V	4.4	4.499	4.4	4.4			
			6 V	5.9	5.999	5.9	5.9			
		I <sub>OH</sub> = -4 mA	4.5 V	3.98	4.3	3.7	3.84			
			6 V	5.48	5.8	5.2	5.34			
V <sub>OL</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 20 μA	2 V	0.002	0.1	0.1	0.1	V		
			4.5 V	0.001	0.1	0.1	0.1			
			6 V	0.001	0.1	0.1	0.1			
		I <sub>OL</sub> = 4 mA	4.5 V	0.17	0.26	0.4	0.33			
			6 V	0.15	0.26	0.4	0.33			
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0	6 V	±0.1	±100	±1000	±1000	nA			
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0, I <sub>O</sub> = 0	6 V	8		160	80	μA			
C <sub>i</sub>		2 V to 6 V	3	10	10	10	pF			

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**timing requirements over recommended operating free-air temperature range (unless otherwise noted)**

		V <sub>CC</sub>	T <sub>A</sub> = 25°C		SN54HC259		SN74HC259		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>w</sub>	Pulse duration	CLR low	2 V	80	120	100	ns		
			4.5 V	16	24	20			
			6 V	14	20	17			
	Ḡ low	2 V	80	120	100				
		4.5 V	16	24	20				
		6 V	14	20	17				
t <sub>su</sub>	Setup time, data or address before Ḡ↑	2 V	75	115	95	ns			
		4.5 V	15	23	19				
		6 V	13	20	16				
t <sub>h</sub>	Hold time, data or address after Ḡ↑	2 V	5	5	5	ns			
		4.5 V	5	5	5				
		6 V	5	5	5				

**switching characteristics over recommended operating free-air temperature range, C<sub>L</sub> = 50 pF (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HC259		SN74HC259		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>PHL</sub>	CLR	Any Q	2 V	60	150	225	190	ns			
			4.5 V	18	30	45	38				
			6 V	14	26	38	32				
t <sub>pd</sub>	Data	Any Q	2 V	56	130	195	165	ns			
			4.5 V	17	26	39	33				
			6 V	13	22	33	28				
	Address	Any Q	2 V	74	200	300	250				
			4.5 V	21	40	60	50				
			6 V	17	34	51	43				
	Ḡ	Any Q	2 V	66	170	255	215				
			4.5 V	20	34	51	43				
			6 V	16	29	43	37				
t <sub>t</sub>		Any	2 V	28	75	110	95	ns			
			4.5 V	8	15	22	19				
			6 V	6	13	19	16				

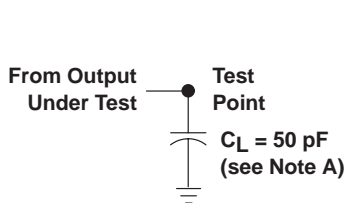
**operating characteristics, T<sub>A</sub> = 25°C**

PARAMETER	TEST CONDITIONS	TYP	UNIT
C <sub>pd</sub> Power dissipation capacitance per latch	No load	33	pF

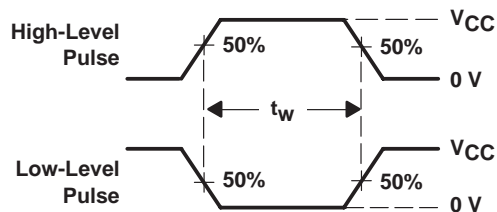
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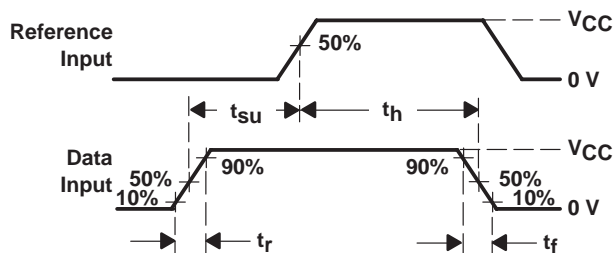
## PARAMETER MEASUREMENT INFORMATION



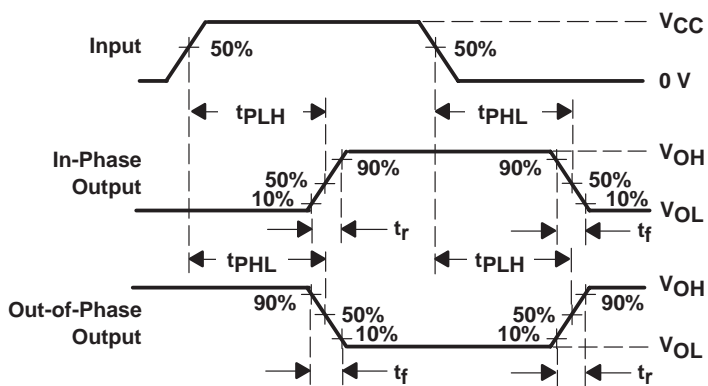
LOAD CIRCUIT



VOLTAGE WAVEFORMS  
PULSE DURATIONS



VOLTAGE WAVEFORMS  
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

- NOTES:
- A.  $C_L$  includes probe and test-fixture capacitance.
  - B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r = 6 \text{ ns}$ ,  $t_f = 6 \text{ ns}$ .
  - C. The outputs are measured one at a time with one input transition per measurement.
  - D.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms



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