ANALOG DEVICES

Low Cost, General Purpose High Speed JFET Amplifier

AD825

FEATURES
High Speed
  41 MHz, –3 dB Bandwidth
  125 V/μs Slew Rate
  80 ns Settling Time
**Input Bias Current of 20 pA and Noise Current of
  10 fA/√Hz**
Input Voltage Noise of 12 nV/√Hz
Fully Specified Power Supplies: ±5 V to ±15 V
Low Distortion: –76 dB at 1 MHz
High Output Drive Capability
  Drives Unlimited Capacitance Load
  50 mA Min Output Current
No Phase Reversal When Input Is at Rail
Available in 8-Lead SOIC

APPLICATIONS
CCD
Low Distortion Filters
Mixed Gain Stages
Audio Amplifier
Photo Detector Interface
ADC Input Buffer
DAC Output Buffer

CONNECTION DIAGRAM
8-Lead Plastic SOIC (R) Package

NC	1	8 NC
–IN	2	7 +V_S
+IN	3	6 OUTPUT
–V_S	4	5 NC

AD825
TOP VIEW
(Not to Scale)

NC = NO CONNECT

PRODUCT DESCRIPTION
The AD825 is a superbly optimized operational amplifier for
high speed, low cost and dc parameters, making it ideally suited
for a broad range of signal conditioning and data acquisition
applications. The ac performance, gain, bandwidth, slew rate
and drive capability are all very stable over temperature. The
AD825 also maintains stable gain under varying load conditions.

The unique input stage has ultralow input bias current and
ultralow input current noise. Signals that go to either rail on this
high performance input do not cause phase reversals at the output.
These features make the AD825 a good choice as a buffer for
MUX outputs, creating minimal offset and gain errors.

The AD825 is fully specified for operation with dual ±5 V and
±15 V supplies. This power supply flexibility, and the low sup-
ply current of 6.5 mA with excellent ac characteristics under all
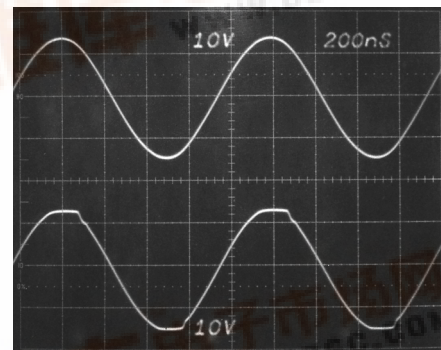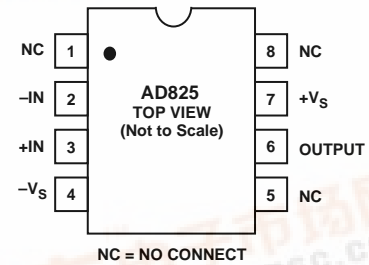supply conditions, makes the AD825 well suited for many
demanding applications.

Figure 1. Performance with Rail-to-Rail Input Signals

REV. C

AD825–SPECIFICATIONS (@ T_A = +25°C, V_S = ±15 V unless otherwise noted)

Parameter	Conditions	V_S	AD825A Min	Typ	Max	Units
DYNAMIC PERFORMANCE						
Unity Gain Bandwidth		±15 V	23	26		MHz
Bandwidth for 0.1 dB Flatness	Gain = +1	±15 V	18	21		MHz
−3 dB Bandwidth	Gain = +1	±15 V	44	46		MHz
Slew Rate	R_{LOAD} = 1 kΩ, G = 1	±15 V	125	140		V/μs
Settling Time to 0.1%	0 V–10 V Step, A_V = −1	±15 V		150	180	ns
to 0.01%	0 V–10 V Step, A_V = −1	±15 V		180	220	ns
Total Harmonic Distortion	F_C = 1 MHz, G = −1	±15 V		−77		dB
Differential Gain Error	NTSC	±15 V		1.3		%
(R_{LOAD} = 150 Ω)	Gain = +2					
Differential Phase Error	NTSC	±15 V		2.1		Degrees
(R_{LOAD} = 150 Ω)	Gain = +2					
INPUT OFFSET VOLTAGE		±15 V		1	2	mV
	T_{MIN} to T_{MAX}				5	mV
Offset Drift				10		μV/°C
INPUT BIAS CURRENT		±15 V		15	40	pA
	T_{MIN}		5			pA
	T_{MAX}				700	pA
INPUT OFFSET CURRENT		±15 V		20	30	pA
	T_{MIN}		5			pA
	T_{MAX}				440	pA
OPEN LOOP GAIN	V_{OUT} = ±10 V	±15 V				
	R_{LOAD} = 1 kΩ		70	76		dB
	V_{OUT} = ±7.5 V	±15 V				
	R_{LOAD} = 1 kΩ		70	76		dB
	V_{OUT} = ±7.5 V	±15 V				
	R_{LOAD} = 150 Ω		72	74		dB
	(50 mA Output)					
COMMON-MODE REJECTION	V_{CM} = ±10 V	±15 V	71	80		dB
INPUT VOLTAGE NOISE	f = 10 kHz	±15 V		12		nV/√Hz
INPUT CURRENT NOISE	f = 10 kHz	±15 V		10		fA/√Hz
INPUT COMMON-MODE VOLTAGE RANGE		±15 V		±13.5		V
OUTPUT VOLTAGE SWING	R_{LOAD} = 1 kΩ	±15 V	13	±13.3		V
	R_{LOAD} = 500 Ω	±15 V	12.9	±13.2		V
Output Current		±15 V	50			mA
Short-Circuit Current		±15 V		100		mA
INPUT RESISTANCE				5×10^{11}		Ω
INPUT CAPACITANCE				6		pF
OUTPUT RESISTANCE	Open Loop			8		Ω
POWER SUPPLY						
Quiescent Current		±15 V		6.5	7.2	mA
	T_{MIN} to T_{MAX}	±15 V			7.5	mA

NOTES
All limits are determined to be at least four standard deviations away from mean value.
Specifications subject to change without notice.

SPECIFICATIONS (@ T_A = +25°C, V_S = ±5 V unless otherwise noted) <div style="text-align:right">**AD825**</div>

Parameter	Conditions	V_S	AD825A Min	AD825A Typ	AD825A Max	Units
DYNAMIC PERFORMANCE						
Unity Gain Bandwidth		±5 V	18	21		MHz
Bandwidth for 0.1 dB Flatness	Gain = +1	±5 V	8	10		MHz
–3 dB Bandwidth	Gain = +1	±5 V	34	37		MHz
Slew Rate	R_{LOAD} = 1 kΩ, G = –1	±5 V	115	130		V/μs
Settling Time to 0.1%	–2.5 V to +2.5 V	±5 V		75	90	ns
to 0.01%	–2.5 V to +2.5 V	±5 V		90	110	ns
Total Harmonic Distortion	F_C = 1 MHz, G = –1	±5 V		–76		dB
Differential Gain Error	NTSC	±5 V		1.2		%
(R_{LOAD} = 150 Ω)	Gain = +2					
Differential Phase Error	NTSC	±5 V		1.4		Degrees
(R_{LOAD} = 150 Ω)	Gain = +2					
INPUT OFFSET VOLTAGE		±5 V		1	2	mV
	T_{MIN} to T_{MAX}				5	mV
Offset Drift				10		μV/°C
INPUT BIAS CURRENT		±5 V		10	30	pA
	T_{MIN}		5			pA
	T_{MAX}				600	pA
INPUT OFFSET CURRENT		±5 V		15	25	pA
	T_{MIN}		5			pA
Offset Current Drift	T_{MAX}				280	pA
OPEN LOOP GAIN	V_{OUT} = ±2.5 V	±5 V				
	R_{LOAD} = 500 Ω		64	66		dB
	R_{LOAD} = 150 Ω		64	66		dB
COMMON-MODE REJECTION	V_{CM} = ±2 V	±5 V	69	80		dB
INPUT VOLTAGE NOISE	f = 10 kHz	±5 V		12		nV/√Hz
INPUT CURRENT NOISE	f = 10 kHz	±5 V		10		fA/√Hz
INPUT COMMON-MODE VOLTAGE RANGE		±5 V		±3.5		V
OUTPUT VOLTAGE SWING	R_{LOAD} = 500 Ω		3.2	±3.4		V
	R_{LOAD} = 150 Ω	±5 V	3.1	±3.2		V
Output Current		±5 V	50			mA
Short-Circuit Current		±5 V		80		mA
INPUT RESISTANCE				5×10^{11}		Ω
INPUT CAPACITANCE				6		pF
OUTPUT RESISTANCE	Open Loop			8		Ω
POWER SUPPLY						
Quiescent Current		±5 V		6.2	6.8	mA
	T_{MIN} to T_{MAX}	±5 V			7.5	mA
POWER SUPPLY REJECTION	V_S = ±5 V to ±15 V		76	88		dB

NOTES
All limits are determined to be at least four standard deviations away from mean value.

Specifications subject to change without notice.

AD825

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . ±18 V
Internal Power Dissipation[2]
  Small Outline (R) . . . . See Derating Curves
Input Voltage (Common Mode) . . . . ±V_S
Differential Input Voltage . . . . ±V_S
Output Short Circuit Duration . . . . See Derating Curves
Storage Temperature Range R . . . . –65°C to +125°C
Operating Temperature Range . . . . –40°C to +85°C
Lead Temperature Range (Soldering 10 sec) . . . . +300°C

NOTES
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Specification is for device in free air: 8-lead SOIC package: θ_{JA} = 155°C/W.

PIN CONFIGURATION

NC = NO CONNECT
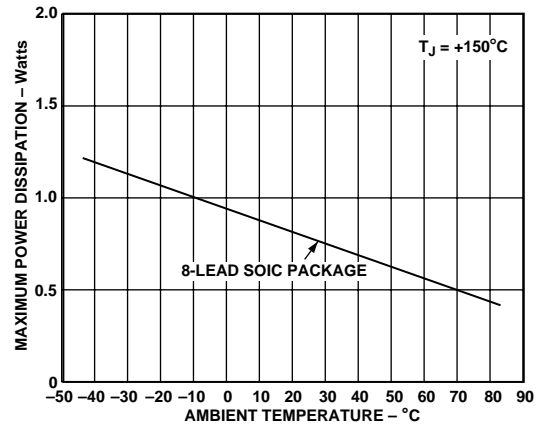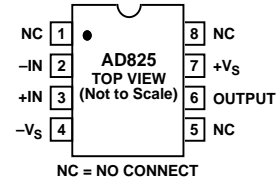
Figure 2. Maximum Power Dissipation vs. Temperature

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD825AR	–40°C to +85°C	8-Lead Plastic SOIC	SO-8
AD825ACHIPS	–40°C to +85°C	Die	
AD825AR-REEL	–40°C to +85°C	13" Tape and Reel	SO-8
AD825AR-REEL7	–40°C to +85°C	7" Tape and Reel	SO-8
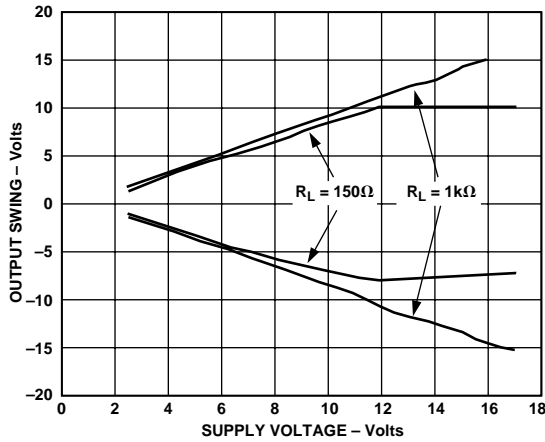
Figure 3. Output Voltage Swing vs. Supply

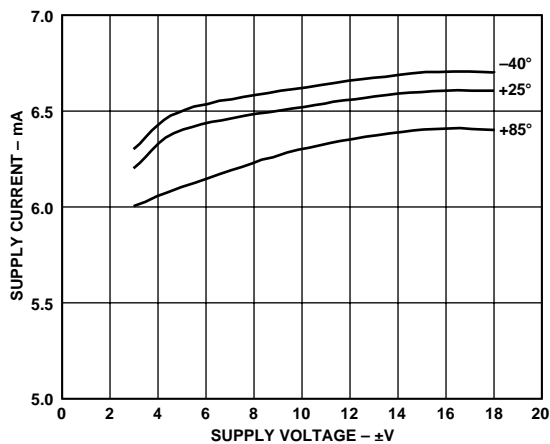Figure 4. Output Voltage Swing vs. Load Resistance

Figure 5. Quiescent Supply Current vs. Supply Voltage for Various Temperatures

Figure 6. Closed-Loop Output Impedance vs. Frequency

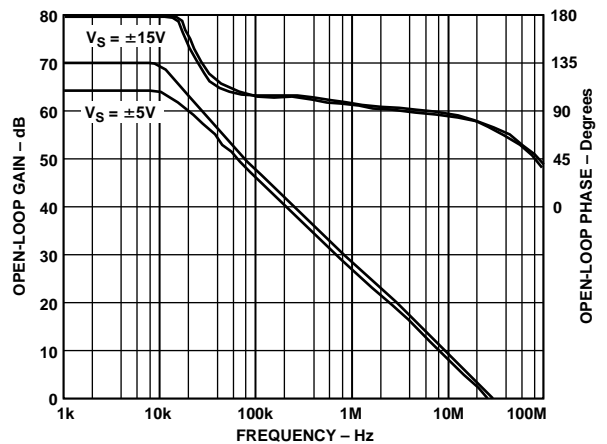Figure 7. Unity Gain Bandwidth and Phase Margin vs. Temperature

Figure 8. Open-Loop Gain and Phase Margin vs. Frequency
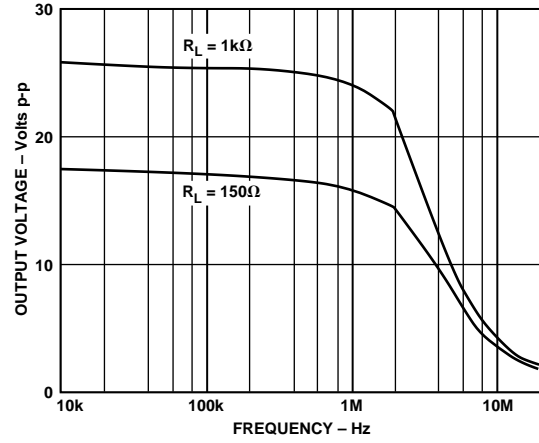
AD825
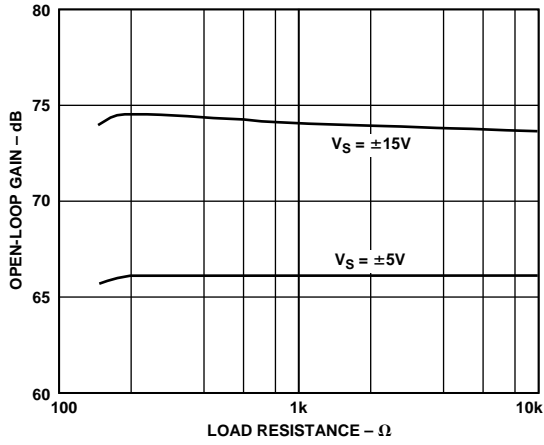
Figure 9. Open-Loop Gain vs. Load Resistance
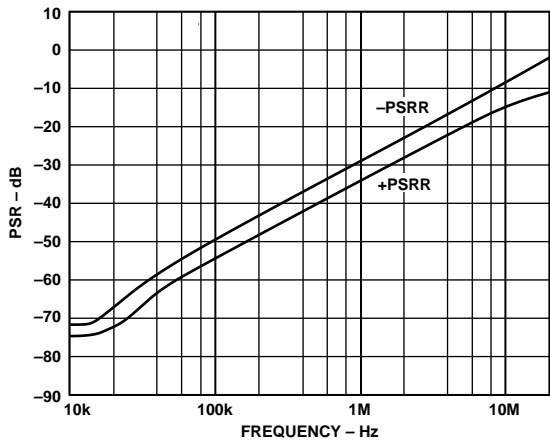

Figure 12. Large Signal Frequency Response; G = +2

Figure 10. Power Supply Rejection vs. Frequency
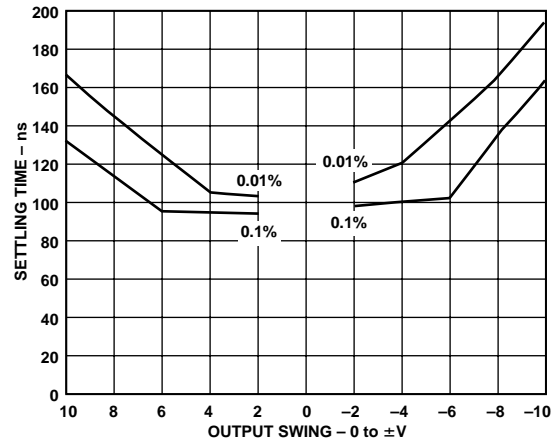
Figure 13. Output Swing and Error vs. Settling Time
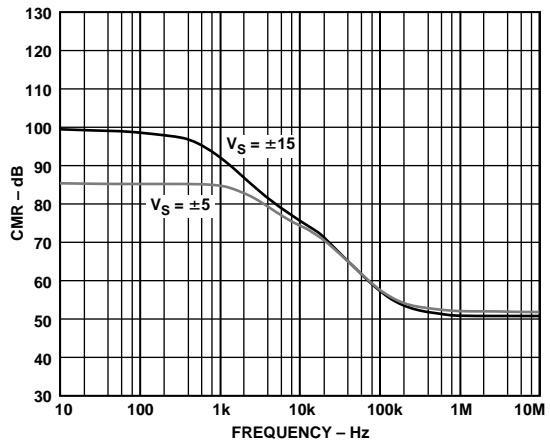
Figure 11. Common-Mode Rejection vs. Frequency
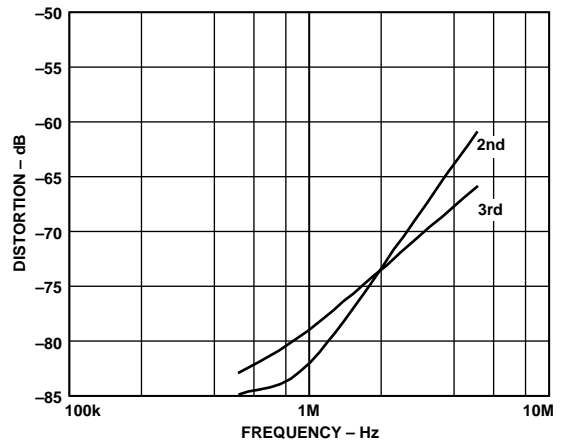
Figure 14. Harmonic Distortion vs. Frequency
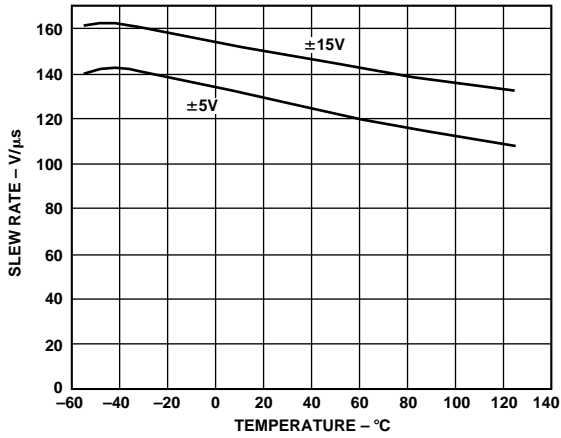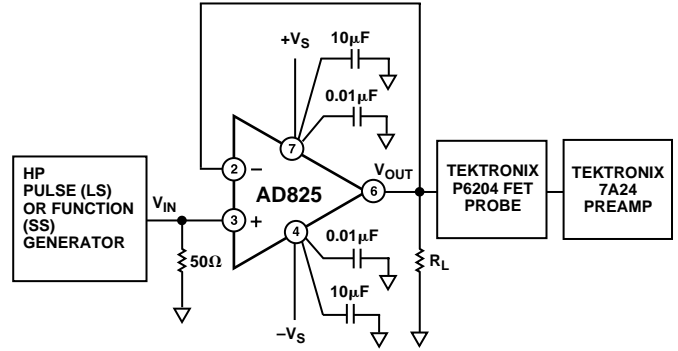
Figure 15. Slew Rate vs. Temperature
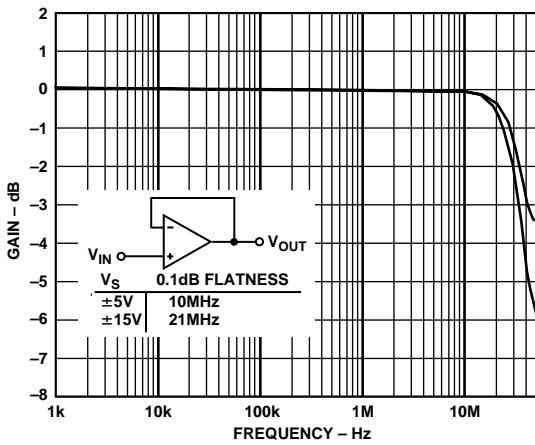

Figure 18. Noninverting Amplifier Connection

Figure 16. Closed-Loop Gain vs. Frequency, Gain = +1

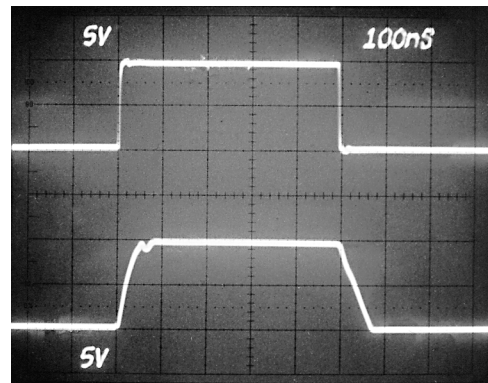Figure 19. Noninverting Large Signal Pulse Response, R_L = 1 kΩ

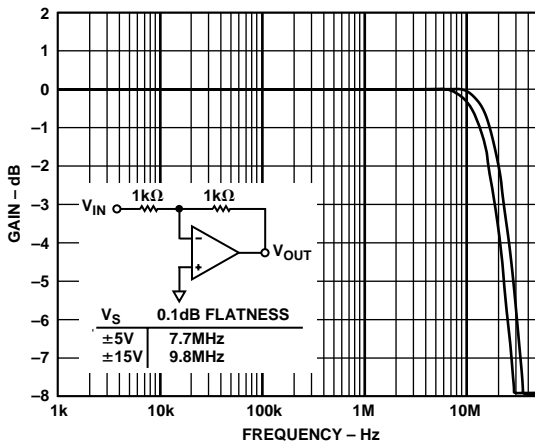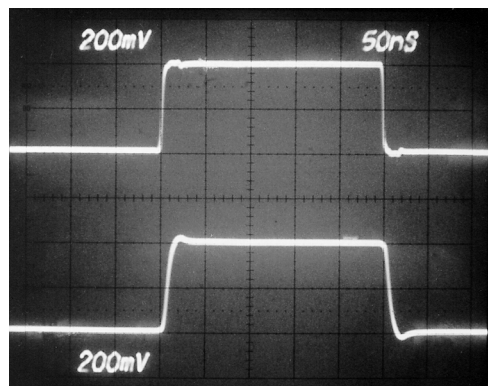Figure 17. Closed-Loop Gain vs. Frequency, Gain = –1

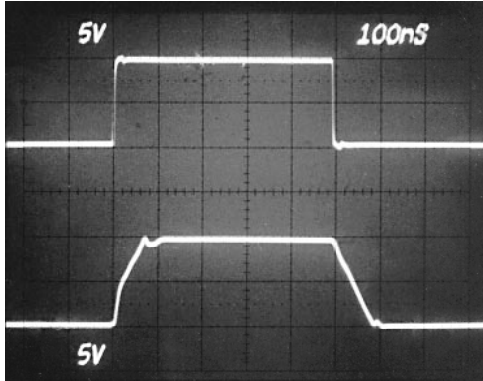Figure 20. Noninverting Small Signal Pulse Response, R_L = 1 kΩ

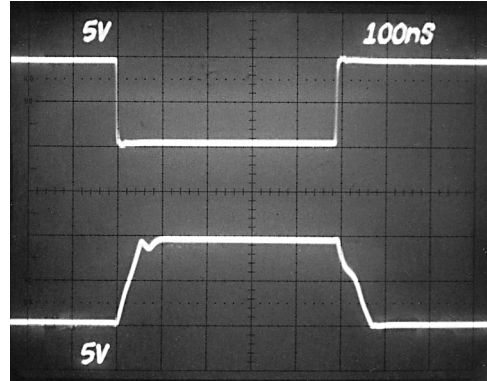Figure 21. Noninverting Large Signal Pulse
Response, $R_L = 150 \ \Omega$

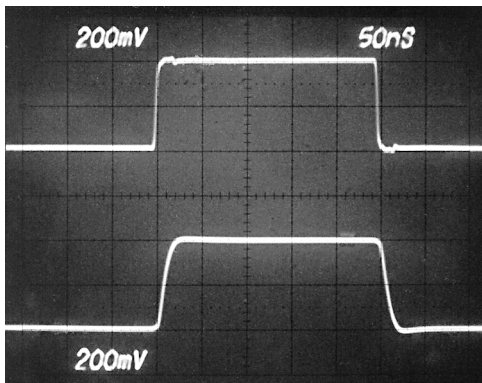Figure 24. Inverting Large Signal Pulse
Response, $R_L = 1 \ k\Omega$

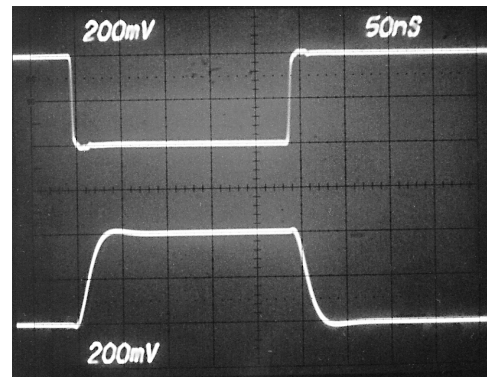Figure 22. Noninverting Small Signal Pulse
Response, $R_L = 150 \ \Omega$

Figure 25. Inverting Small Signal Pulse
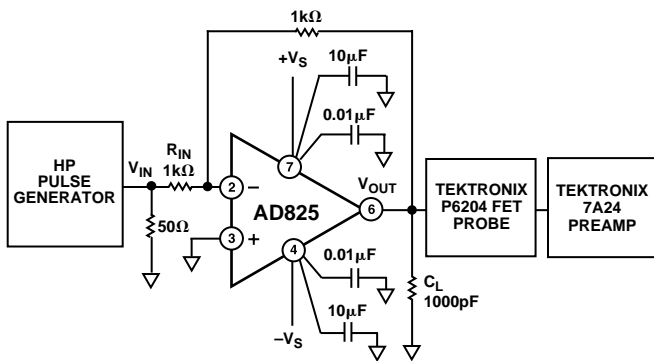Response, $R_L = 1 \ k\Omega$

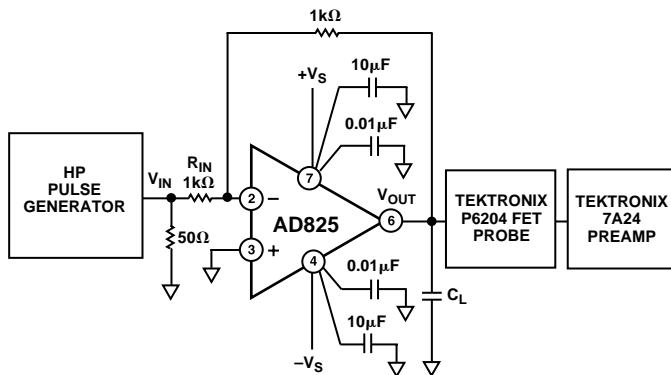Figure 23. Inverting Amplifier Connection
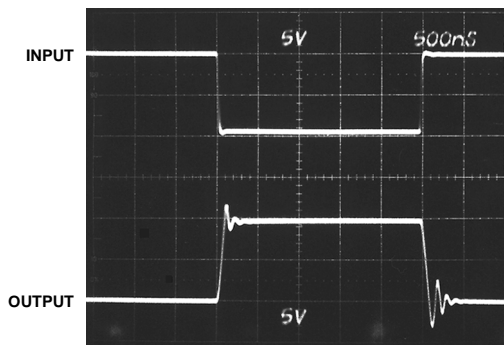
Figure 26a. Inverting Amplifier Driving a Capacitive Load

Figure 26b. Inverting Amplifier Pulse Response
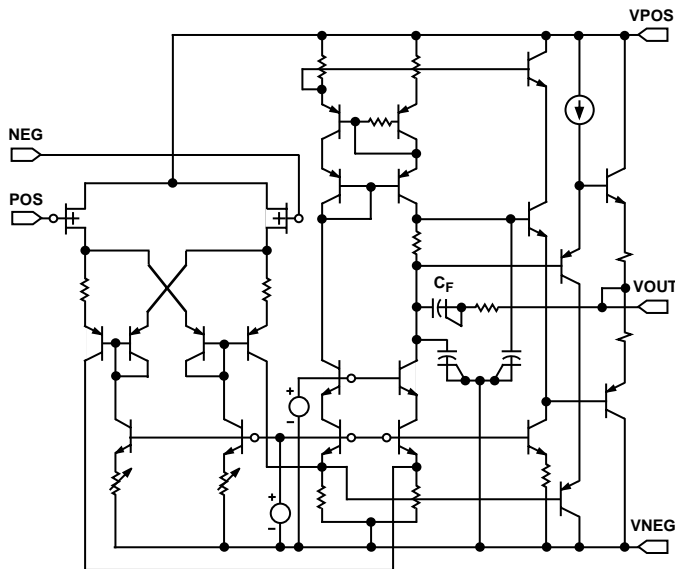While Driving a 400 pF Capacitive Loads

Figure 27. Simplified Schematic

DRIVING CAPACITIVE LOADS
The internal compensation of the AD825, together with its high output current drive, permits excellent large signal performance while driving extremely high capacitive loads.

THEORY OF OPERATION
The AD825 is a low cost, wide band, high performance FET input operational amplifier. With its unique input stage design, the AD825 assures no phase reversal even for inputs that exceed the power supply voltages, and its output stage is designed to drive heavy capacitive or resistive load with small changes relative to no load condition.

The AD825 (Figure 27) consists of common-drain common-base FET input stage driving a cascoded, common base matched NPN gain stage. The output buffer stage uses emitter followers in a class AB amplifier that can deliver large current to the load while maintaining low levels of distortion.

The capacitor, C_F, in the output stage, enables the AD825 to drive heavy capacitive load. For light load, the gain of the output buffer is close to unity, C_F is bootstrapped and not much happens. As the capacitive load is increased, the gain of the output buffer is decreased and the bandwidth of the amplifier is reduced through a portion of C_F adding to the dominant pole. As the capacitive load is further increased, the amplifier's bandwidth continues to drop, maintaining the stability of the AD825.

Input Consideration
The AD825 with its unique input stage assures no phase reversal for signals as large or even larger than the supply voltages. Also, layout considerations of the input transistors assure functionality even with a large differential signal.

The need for a low noise input stage calls for a larger FET transistor. One should consider the additional capacitance that is added to assure stability. When filters are designed with the AD825, one needs to consider the input capacitance (5 pF–6 pF) of the AD825 as part of the passive network.

Grounding and Bypassing
The AD825 is a low input bias current FET amplifier. Its high frequency response makes it useful in applications such as photo diode interfaces, filters and audio circuits. When designing high frequency circuits, some special precautions are in order. Circuits must be built with short interconnects, and resistances should have low inductive paths to ground. Power supply leads should be bypassed to common as close as possible to the amplifier pins. Ceramic capacitors of 0.1 µF are recommended.

AD825

Second Order Low-Pass Filter

A second order Butterworth low-pass filter can be implemented using the AD825 as shown in Figure 28. The extremely low bias currents of the AD825 allow the use of large resistor values, and consequently small capacitor values, without concern for developing large offset errors. Low current noise is another factor in permitting the use of large resistors without having to worry about the resultant voltage noise.

With the values shown, the corner frequency will be 1 MHz. The equations for component selection are shown below. Note that the noninverting input (and the inverting input) has an input capacitance of 6 pF. As a result, the calculated value of C1 (12 pF) is reduced to 6 pF.

$$C1 = \frac{1.414}{2\pi\, f_{CUTOFF} R1}$$

$$C2\,(farads) = \frac{0.707}{2\pi\, f_{CUTOFF} R1}$$

$$R1 = R2 = user\ selected\ \left(typically\ 10\,k\Omega\ to\ 100\,k\Omega\right)$$

A plot of the filter frequency response is shown in Figure 29; better than 40 dB of high frequency rejection is provided.
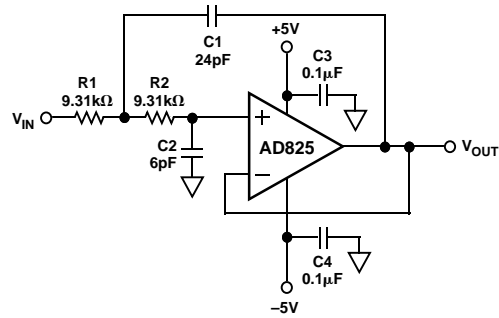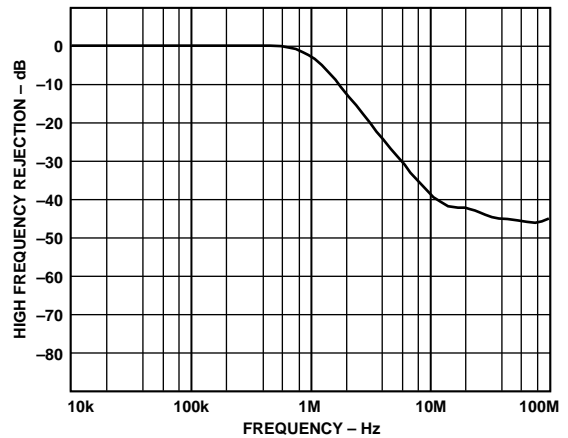

Figure 28. Second Order Butterworth Low-Pass Filter

Figure 29. Frequency Response of Second Order Butterworth Filter

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

8-Lead Plastic SOIC
(SO-8)