

**INTEGRATED CIRCUITS**

# DATA SHEET

## **74LVC16245A; 74LVCH16245A** 16-bit bus transceiver with direction pin; 5 V tolerant; 3-state

Product specification  
Supersedes data of 2003 Jan 30

2003 Nov 25

Philips  
Semiconductors



**PHILIPS**



## 16-bit bus transceiver with direction pin; 5 V tolerant; 3-state

### 74LVC16245A; 74LVCH16245A

#### FEATURES

- 5 V tolerant inputs/outputs for interfacing with 5 V logic
- Wide supply voltage range from 1.2 to 3.6 V
- CMOS low power consumption
- MULTIBYTE™ flow-through standard pin-out architecture
- Low inductance multiple power and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels
- High-impedance when  $V_{CC} = 0$  V
- All data inputs have bushold (74LVCH16245A only)
- Complies with JEDEC standard no. 8-1A
- ESD protection:  
HBM EIA/JESD22-A114-A exceeds 2000 V  
MM EIA/JESD22-A115-A exceeds 200 V.

#### DESCRIPTION

The 74LVC(H)16245A is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families. Inputs can be driven from either 3.3 or 5 V devices. In 3-state operation, outputs can handle 5 Volt. These features allow the use of these devices as a mixed 3.3 and 5 V environment.

The 74LVC(H)16245A is a 16-bit transceiver featuring non-inverting 3-state bus compatible outputs in both send and receive directions. The device features two output enable ( $\overline{nOE}$ ) inputs for easy cascading and two send/receive ( $\overline{nDIR}$ ) inputs for direction control.  $\overline{nOE}$  controls the outputs so that the buses are effectively isolated. This device can be used as two 8-bit transceivers or one 16-bit transceiver.

The 74LVCH16245A bushold data inputs eliminates the need for external pull-up resistors to hold unused inputs.

#### QUICK REFERENCE DATA

GND = 0 V;  $T_{amb} = 25$  °C;  $t_r = t_f \leq 2.5$  ns.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
$t_{PHL}/t_{PLH}$	propagation delay nAn to nBn; nBn to nAn	$C_L = 50$ pF; $V_{CC} = 3.3$ V	2.2	ns
$C_I$	input capacitance		5.0	pF
$C_{I/O}$	input/output capacitance		10	pF
$C_{PD}$	power dissipation capacitance per gate	$V_{CC} = 3.3$ V; notes 1 and 2	30	pF

#### Notes

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu$ W).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz;

$f_o$  = output frequency in MHz;

$C_L$  = output load capacitance in pF;

$V_{CC}$  = supply voltage in Volts;

$N$  = total load switching outputs;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.

2. The condition is  $V_I = \text{GND to } V_{CC}$ .

16-bit bus transceiver with direction pin; 5 V tolerant;  
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#### ORDERING INFORMATION

TYPE NUMBER	PACKAGE				
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE
74LVC16245ADL	-40 to +125 °C	48	SSOP48	plastic	SOT370-1
74LVCH16245ADL	-40 to +125 °C	48	SSOP48	plastic	SOT370-1
74LVC16245ADGG	-40 to +125 °C	48	TSSOP48	plastic	SOT362-1
74LVCH16245ADGG	-40 to +125 °C	48	TSSOP48	plastic	SOT362-1
74LVC16245AEV	-40 to +125 °C	56	VFBGA56	plastic	SOT702-1
74LVCH16245AEV	-40 to +125 °C	56	VFBGA56	plastic	SOT702-1

#### FUNCTION TABLE

See note 1.

INPUT		OUTPUT	
nOE	nDIR	nAn	nBn
L	L	A = B	inputs
L	H	inputs	B = A
H	X	Z	Z

#### Note

1. H = HIGH voltage level;  
L = LOW voltage level;  
X = don't care;  
Z = high-impedance OFF-state.

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#### PINNING

SYMBOL	PIN	BALL	DESCRIPTION
1DIR	1	A1	direction control input
1B0	2	B2	data input/output
1B1	3	B1	data input/output
GND	4, 10, 15, 21, 28, 34, 39, 45	B3, B4, D3, D4, G3, G4, J3, J4	ground (0 V)
1B2	5	C2	data input/output
1B3	6	C1	data input/output
V <sub>CC</sub>	7, 18, 31, 42	C3, C4, H3, H4	supply voltage
1B4	8	D2	data input/output
1B5	9	D1	data input/output
1B6	11	E2	data input/output
1B7	12	E1	data input/output
2B0	13	F1	data input/output
2B1	14	F2	data input/output
2B2	16	G1	data input/output
2B3	17	G2	data input/output
2B4	19	H1	data input/output
2B5	20	H2	data input/output
2B6	22	J1	data input/output
2B7	23	J2	data input/output
2DIR	24	K1	direction control input
2O <sub>E</sub>	25	K6	output enable input (active LOW)
2A7	26	J5	data input/output
2A6	27	J6	data input/output
2A5	29	H5	data input/output
2A4	30	H6	data input/output
2A3	32	G5	data input/output
2A2	33	G6	data input/output
2A1	35	F5	data input/output
2A0	36	F6	data input/output
1A7	37	E6	data input/output
1A6	38	E5	data input/output
1A5	40	D6	data input/output
1A4	41	D5	data input/output
1A3	43	C6	data input/output
1A2	44	C5	data input/output
1A1	46	B6	data input/output
1A0	47	B5	data input/output
1O <sub>E</sub>	48	A6	output enable input (active LOW)
n.c.	–	A2, A3, A4, A5, K2, K3, K4, K5	not connected

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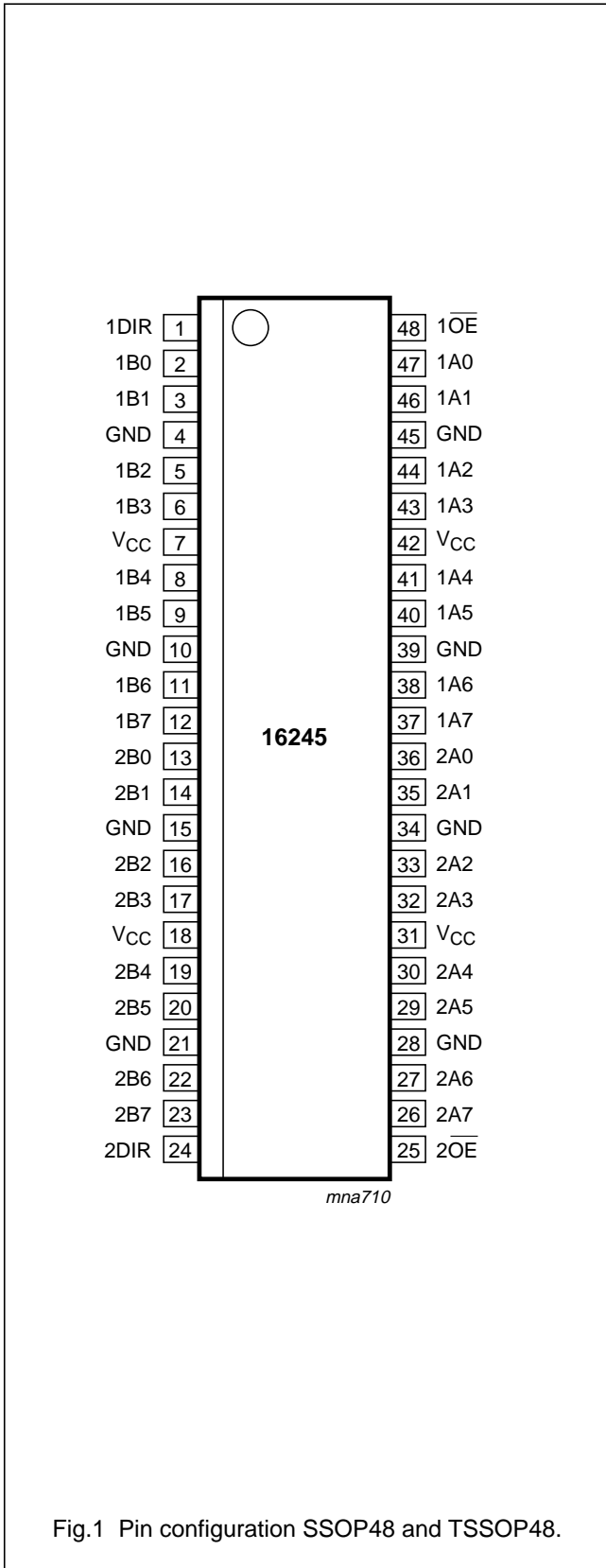


Fig.1 Pin configuration SSOP48 and TSSOP48.

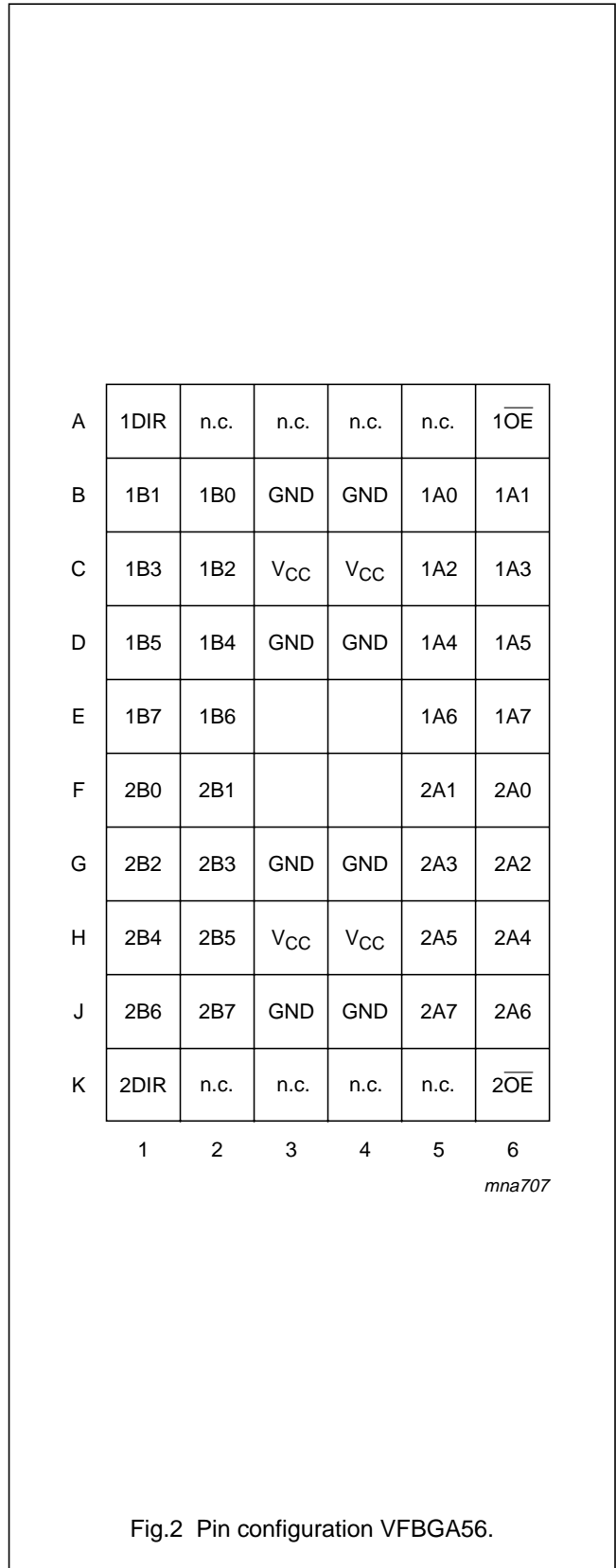


Fig.2 Pin configuration VFBGA56.

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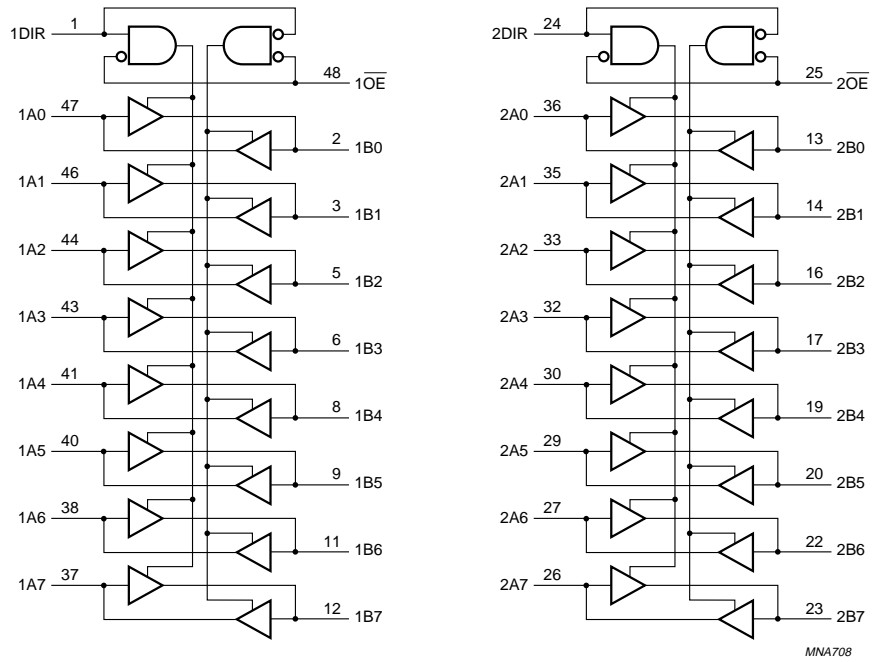
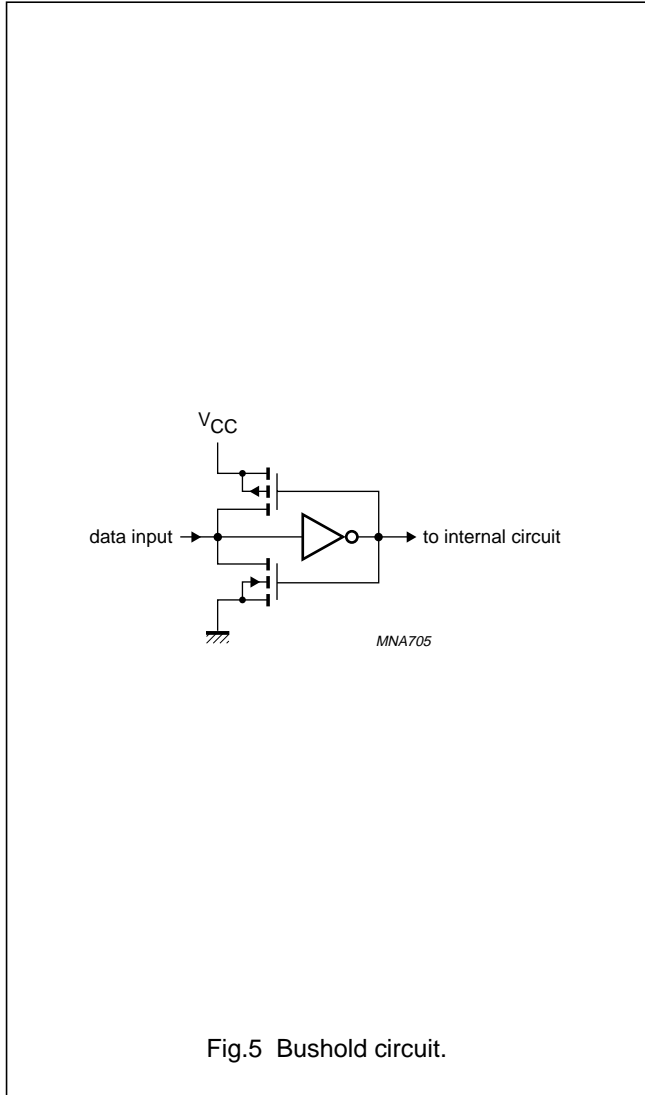
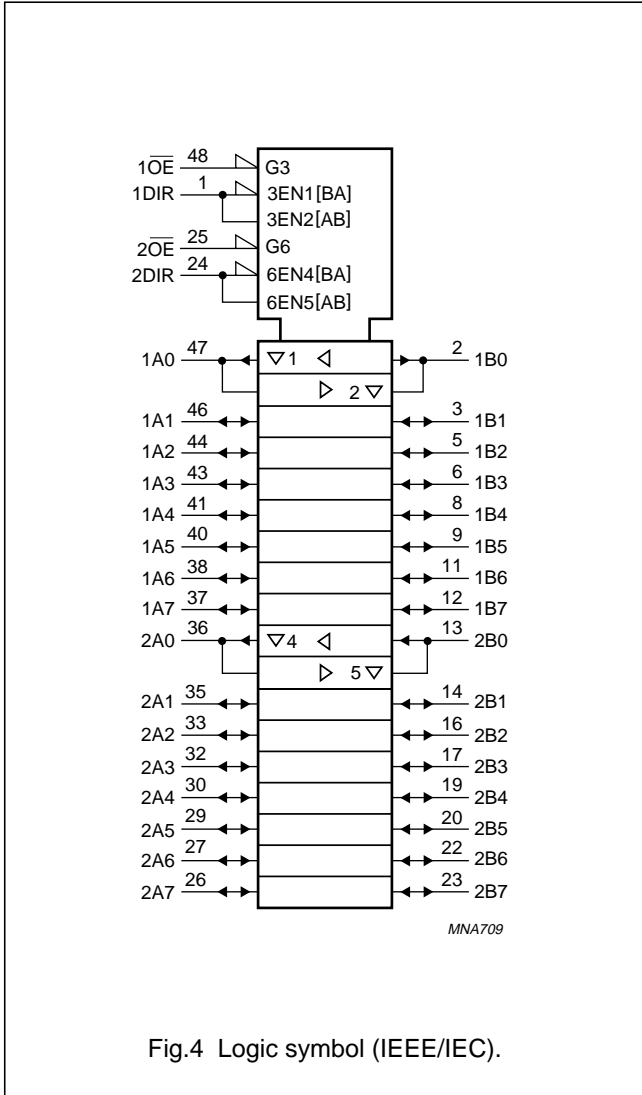


Fig.3 Logic symbol.

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### RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V <sub>CC</sub>	supply voltage	for maximum speed performance	2.7	3.6	V
		for low voltage applications	1.2	3.6	V
V <sub>I</sub>	input voltage		0	5.5	V
V <sub>O</sub>	output voltage	output HIGH or LOW state	0	V <sub>CC</sub>	V
		output 3-state	0	5.5	V
T <sub>amb</sub>	operating ambient temperature	in free air	-40	+125	°C
t <sub>r</sub> , t <sub>f</sub>	input rise and fall times	V <sub>CC</sub> = 1.2 to 2.7 V	0	20	ns/V
		V <sub>CC</sub> = 2.7 to 3.6 V	0	10	ns/V

### LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V <sub>CC</sub>	supply voltage		-0.5	+6.5	V
I <sub>IK</sub>	input diode current	V <sub>I</sub> < 0	-	-50	mA
V <sub>I</sub>	input voltage	note 1	-0.5	+6.5	V
I <sub>OK</sub>	output diode current	V <sub>O</sub> > V <sub>CC</sub> or V <sub>O</sub> < 0	-	±50	mA
V <sub>O</sub>	output voltage	output HIGH or LOW state; note 1	-0.5	V <sub>CC</sub> + 0.5	V
		output 3-state; note 1	-0.5	+6.5	V
I <sub>O</sub>	output source or sink current	V <sub>O</sub> = 0 to V <sub>CC</sub>	-	±50	mA
I <sub>CC</sub> , I <sub>GND</sub>	V <sub>CC</sub> or GND current		-	±100	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
P <sub>tot</sub>	power dissipation SSOP and TSSOP package VFPGA package	T <sub>amb</sub> = -40 to +125 °C; note 2	-	500	mW
		T <sub>amb</sub> = -40 to +125 °C; note 3	-	1000	mW

### Notes

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. Above 60 °C the value of P<sub>D</sub> derates linearly with 5.5 mW/K.
3. Above 70 °C the value of P<sub>D</sub> derates linearly with 1.8 mW/K.



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**DC CHARACTERISTICS**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP. <sup>(1)</sup>	MAX.	UNIT
		OTHER	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 to +85 °C</b>							
V <sub>IH</sub>	HIGH-level input voltage		1.2	V <sub>CC</sub>	–	–	V
			2.7 to 3.6	2.0	–	–	V
V <sub>IL</sub>	LOW-level input voltage		1.2	–	–	0	V
			2.7 to 3.6	–	–	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = -100 µA	2.7 to 3.6	V <sub>CC</sub> - 0.2	V <sub>CC</sub>	–	V
		I <sub>O</sub> = -12 mA	2.7	V <sub>CC</sub> - 0.5	–	–	V
		I <sub>O</sub> = -18 mA	3.0	V <sub>CC</sub> - 0.6	–	–	V
		I <sub>O</sub> = -24 mA	3.0	V <sub>CC</sub> - 0.8	–	–	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = 100 µA	2.7 to 3.6	–	0	0.20	V
		I <sub>O</sub> = 12 mA	2.7	–	–	0.40	V
		I <sub>O</sub> = 24 mA	3.0	–	–	0.55	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND ; notes 2 and 3	3.6	–	±0.1	±5	µA
I <sub>OZ</sub>	3-state output OFF-state current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = 5.5 V or GND	3.6	–	0.1	±5	µA
I <sub>off</sub>	power off leakage supply	V <sub>I</sub> or V <sub>O</sub> = 5.5 V	0.0	–	0.1	±10	µA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0	3.6	–	0.1	10	µA
ΔI <sub>CC</sub>	additional quiescent supply current per pin	V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; I <sub>O</sub> = 0	2.7 to 3.6	–	5	500	µA
I <sub>BHL</sub>	bushold LOW sustaining current	V <sub>I</sub> = 0.8 V; notes 4, 5 and 6	3.0	75	–	–	µA
I <sub>BHH</sub>	bushold HIGH sustaining current	V <sub>I</sub> = 2.0 V; notes 4, 5 and 6	3.0	-75	–	–	µA
I <sub>BHLO</sub>	bushold LOW overdrive current	notes 4, 5 and 7	3.6	500	–	–	µA
I <sub>BHNO</sub>	bushold HIGH overdrive current	notes 4, 5 and 7	3.6	-500	–	–	µA

**16-bit bus transceiver with direction pin; 5 V tolerant;  
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SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP. <sup>(1)</sup>	MAX.	UNIT
		OTHER	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 to +125 °C</b>							
V <sub>IH</sub>	HIGH-level input voltage		1.2	V <sub>CC</sub>	-	-	V
			2.7 to 3.6	2.0	-	-	V
V <sub>IL</sub>	LOW-level input voltage		1.2	-	-	GND	V
			2.7 to 3.6	-	-	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = -100 μA	2.7 to 3.6	V <sub>CC</sub> - 0.3	-	-	V
		I <sub>O</sub> = -12 mA	2.7	V <sub>CC</sub> - 0.65	-	-	V
		I <sub>O</sub> = -18 mA	3.0	V <sub>CC</sub> - 0.75	-	-	V
		I <sub>O</sub> = -24 mA	3.0	V <sub>CC</sub> - 1	-	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = 100 μA	2.7 to 3.6	-	0	0.3	V
		I <sub>O</sub> = 12 mA	2.7	-	-	0.6	V
		I <sub>O</sub> = 24 mA	3.0	-	-	0.8	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND ; note 2	3.6	-	-	±20	μA
I <sub>OZ</sub>	3-state output OFF-state current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = 5.5 V or GND; D; notes 2 and 3	3.6	-	-	±20	μA
I <sub>off</sub>	power off leakage supply	V <sub>I</sub> or V <sub>O</sub> = 5.5 V	0.0	-	-	±20	μA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0	3.6	-	-	40	μA
ΔI <sub>CC</sub>	additional quiescent supply current per pin	V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; I <sub>O</sub> = 0	2.7 to 3.6	-	-	5000	μA
I <sub>BHL</sub>	bushold LOW sustaining current	V <sub>I</sub> = 0.8 V; notes 4, 5 and 6	3.0	60	-	-	μA
I <sub>BHH</sub>	bushold HIGH sustaining current	V <sub>I</sub> = 2.0 V; notes 4, 5 and 6	3.0	-60	-	-	μA
I <sub>BHLO</sub>	bushold LOW overdrive current	notes 4, 5 and 7	3.6	500	-	-	μA
I <sub>BHHO</sub>	bushold HIGH overdrive current	notes 4, 5 and 7	3.6	-500	-	-	μA

**Notes**

1. All typical values are measured at V<sub>CC</sub> = 3.3 V and T<sub>amb</sub> = 25 °C.
2. For bushold parts, the bushold circuit is switched off when V<sub>I</sub> > V<sub>CC</sub> allowing 5.5 V on the input terminal.
3. For I/O ports the parameter I<sub>OZ</sub> includes the input leakage current.
4. Valid for data inputs of bushold parts (74LVCH16245A) only.
5. For data inputs only, control inputs do not have a bushold circuit.
6. The specified sustaining current at the data input holds the input below the specified V<sub>I</sub> level.
7. The specified overdrive current at the data input forces the data input to the opposite input state.

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### AC CHARACTERISTICS

GND = 0 V;  $t_r = t_f \leq 2.5$  ns.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP. <sup>(1)</sup>	MAX.	UNIT
		WAVEFORMS	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 to +85 °C</b>							
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay nAn to nBn; nBn to nAn	see Figs 6 and 8	1.2	–	13.0	–	ns
			2.7	1.0	2.7	4.7	ns
			3.0 to 3.6	1.0	2.2 <sup>(2)</sup>	4.5	ns
t <sub>PZH</sub> /t <sub>PZL</sub>	3-state output enable time $\overline{nOE}$ to nAn; $\overline{nOE}$ to nBn	see Figs 7 and 8	1.2	–	15.0	–	ns
			2.7	1.5	3.6	6.7	ns
			3.0 to 3.6	1.0	2.8 <sup>(2)</sup>	5.5	ns
t <sub>PHZ</sub> /t <sub>PLZ</sub>	3-state output disable time $\overline{nOE}$ to nAn; $\overline{nOE}$ to nBn	see Figs 7 and 8	1.2	–	11.0	–	ns
			2.7	1.5	3.4	6.6	ns
			3.0 to 3.6	1.5	3.2 <sup>(2)</sup>	5.6	ns
<b>T<sub>amb</sub> = -40 to +125 °C</b>							
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay nAn to nBn; nBn to nAn	see Figs 6 and 8	1.2	–	–	–	ns
			2.7	1.0	–	6.0	ns
			3.0 to 3.6	1.0	–	6.0	ns
t <sub>PZH</sub> /t <sub>PZL</sub>	3-state output enable time $\overline{nOE}$ to nAn; $\overline{nOE}$ to nBn	see Figs 7 and 8	1.2	–	–	–	ns
			2.7	1.5	–	8.5	ns
			3.0 to 3.6	1.0	–	7.0	ns
t <sub>PHZ</sub> /t <sub>PLZ</sub>	3-state output disable time $\overline{nOE}$ to nAn; $\overline{nOE}$ to nBn	see Figs 7 and 8	1.2	–	–	–	ns
			2.7	1.5	–	8.5	ns
			3.0 to 3.6	1.5	–	7.0	ns

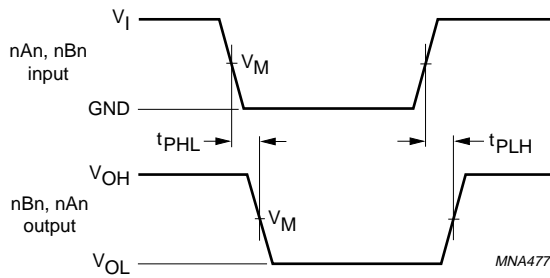
### Notes

1. All typical values are measured at T<sub>amb</sub> = 25 °C.
2. Typical values are measured at V<sub>CC</sub> = 3.3 V and T<sub>amb</sub> = 25 °C.

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AC WAVEFORMS



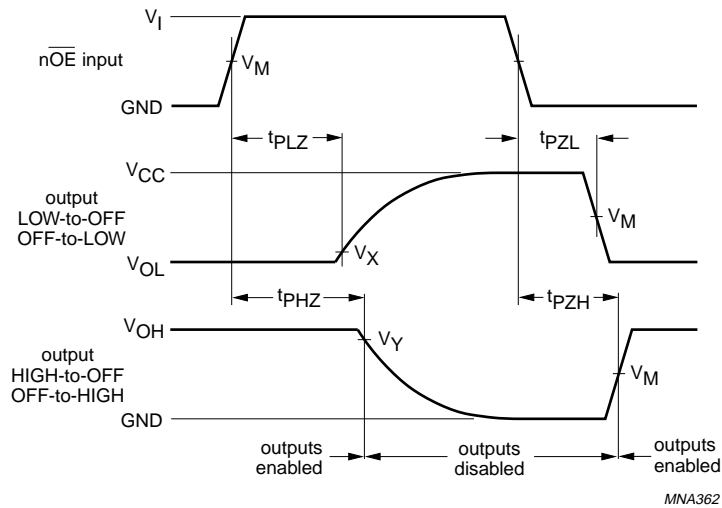
V <sub>CC</sub>	V <sub>M</sub>	INPUT	
		V <sub>I</sub>	t <sub>r</sub> = t <sub>f</sub>
1.2 V	0.5 × V <sub>CC</sub>	V <sub>CC</sub>	≤ 2.5 ns
2.7 V	1.5 V	2.7 V	≤ 2.5 ns
3.0 to 3.6 V	1.5 V	2.7 V	≤ 2.5 ns

V<sub>OL</sub> and V<sub>OH</sub> are typical output voltage drop that occur with the output load.

Fig.6 The input (nAn, nBn) to output (nBn, nAn) propagation delays.

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V <sub>CC</sub>	V <sub>M</sub>	INPUT	
		V <sub>I</sub>	t <sub>r</sub> = t <sub>f</sub>
1.2 V	0.5 × V <sub>CC</sub>	V <sub>CC</sub>	≤ 2.5 ns
2.7 V	1.5 V	2.7 V	≤ 2.5 ns
3.0 to 3.6 V	1.5 V	2.7 V	≤ 2.5 ns

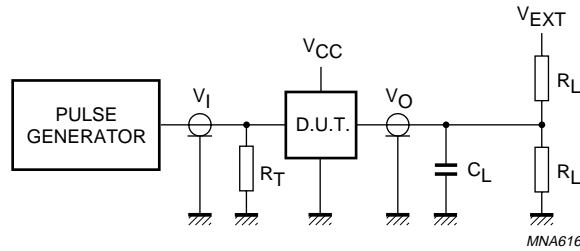
V<sub>X</sub> = V<sub>OL</sub> + 0.3 V at V<sub>CC</sub> ≥ 2.7 V;  
 V<sub>X</sub> = V<sub>OL</sub> + 0.1 V at V<sub>CC</sub> < 2.7 V.  
 V<sub>Y</sub> = V<sub>OH</sub> - 0.3 V at V<sub>CC</sub> ≥ 2.7 V;  
 V<sub>Y</sub> = V<sub>OH</sub> - 0.1 V at V<sub>CC</sub> < 2.7 V.

V<sub>OL</sub> and V<sub>OH</sub> are typical output voltage drop that occur with the output load.

Fig.7 3-state enable and disable times.

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V <sub>CC</sub>	V <sub>I</sub>	C <sub>L</sub>	R <sub>L</sub> <sup>(1)</sup>	V <sub>EXT</sub>		
				t <sub>PLH</sub> /t <sub>PHL</sub>	t <sub>PZH</sub> /t <sub>PHZ</sub>	t <sub>PZL</sub> /t <sub>PLZ</sub>
1.2 V	V <sub>CC</sub>	50 pF	500 Ω	open	GND	2 × V <sub>CC</sub>
2.7 V	2.7 V	50 pF	500 Ω	open	GND	2 × V <sub>CC</sub>
3.0 to 3.6 V	2.7 V	50 pF	500 Ω	open	GND	2 × V <sub>CC</sub>

**Note**

1. The circuit performs better when R<sub>L</sub> = 1 000 Ω.

Definitions for test circuit:

R<sub>L</sub> = Load resistor.

C<sub>L</sub> = Load capacitance including jig and probe capacitance.

R<sub>T</sub> = Termination resistance should be equal to the output impedance Z<sub>o</sub> of the pulse generator.

Fig.8 Load circuitry for switching times.

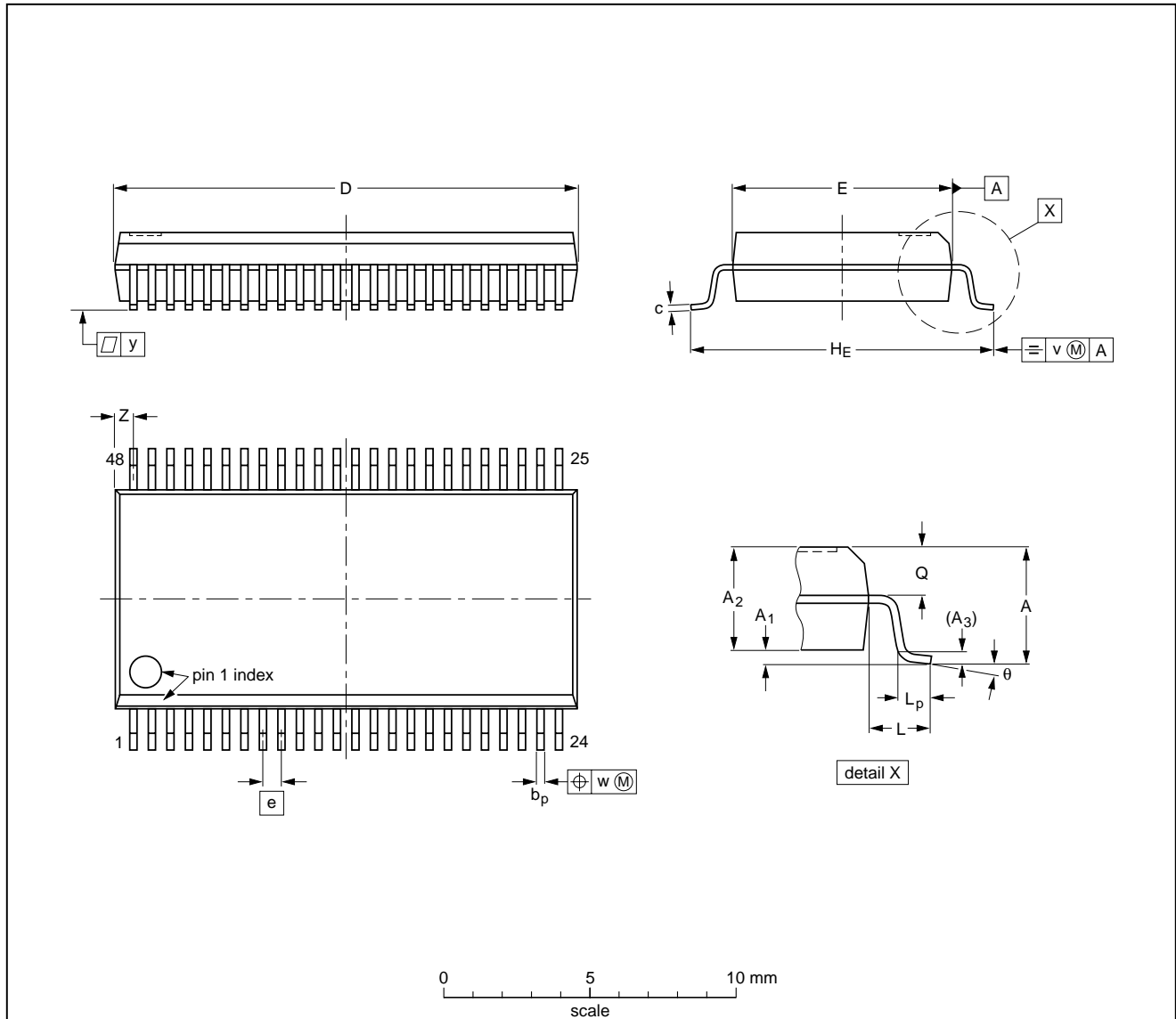
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PACKAGE OUTLINES

SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm

SOT370-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	z <sup>(1)</sup>	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	16.00 15.75	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

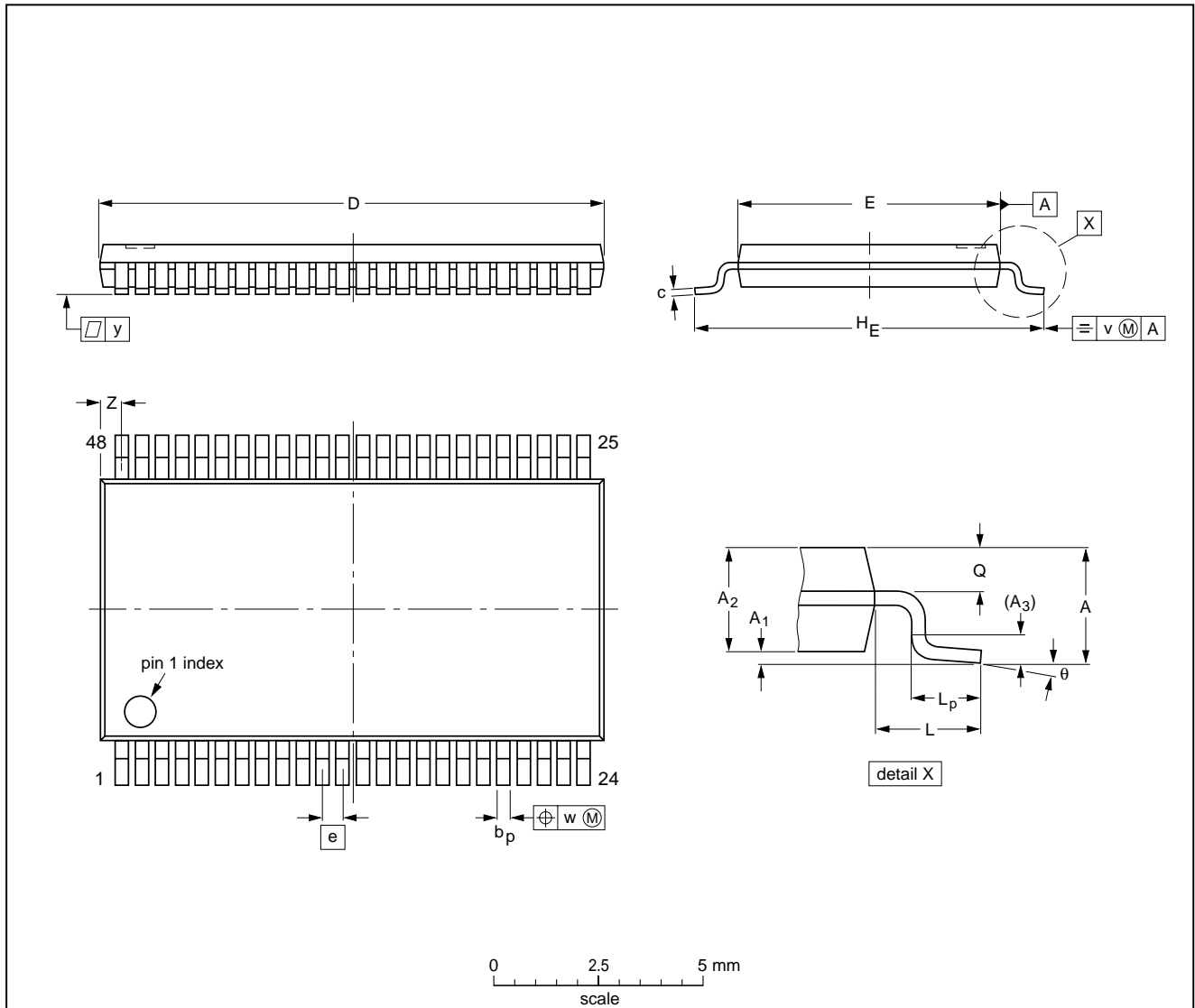
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT370-1		MO-118			99-12-27 03-02-19

16-bit bus transceiver with direction pin; 5 V tolerant;  
3-state

74LVC16245A;  
74LVCH16245A

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm

SOT362-1



**DIMENSIONS (mm are the original dimensions).**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	12.6 12.4	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.8 0.4	8° 0°

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT362-1		MO-153			99-12-27 03-02-19

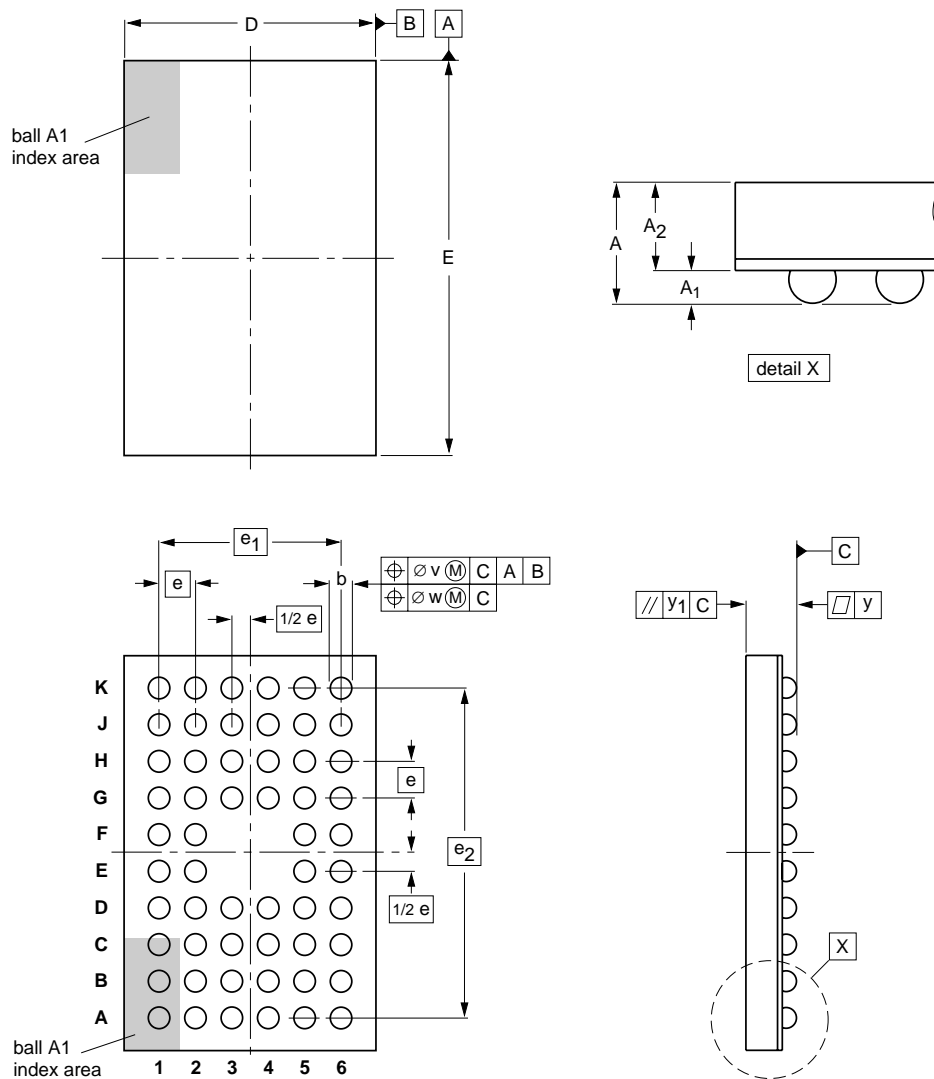


16-bit bus transceiver with direction pin; 5 V tolerant;  
3-state

74LVC16245A;  
74LVCH16245A

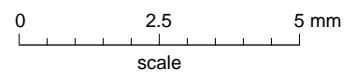
VFBGA56: plastic very thin fine-pitch ball grid array package; 56 balls; body 4.5 x 7 x 0.65 mm

SOT702-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	b	D	E	e	e <sub>1</sub>	e <sub>2</sub>	v	w	y	y <sub>1</sub>
mm	1	0.3 0.2	0.7 0.6	0.45 0.35	4.6 4.4	7.1 6.9	0.65	3.25	5.85	0.15	0.08	0.08	0.1



OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT702-1		MO-225			02-08-08 03-07-01

16-bit bus transceiver with direction pin; 5 V tolerant;  
3-state

74LVC16245A;  
74LVCH16245A

#### DATA SHEET STATUS

LEVEL	DATA SHEET STATUS <sup>(1)</sup>	PRODUCT STATUS <sup>(2)(3)</sup>	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

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3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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