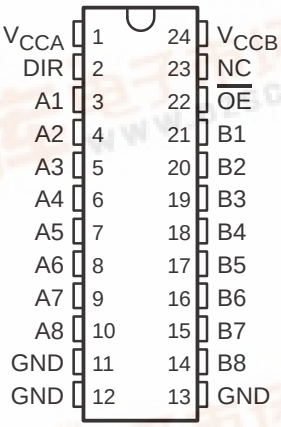
OCTAL BUS TRANSCEIVER WITH ADJUSTABLE OUTPUT VOLTAGE AND 3-STATE OUTPUTS

SCAS585F – NOVEMBER 1996 – REVISED AUGUST 1998

- ***EPIC***™ **(Enhanced-Performance Implanted CMOS) Submicron Process**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages**

DB, DW, OR PW PACKAGE
(TOP VIEW)



NC – No internal connection

description

This 8-bit (octal) noninverting bus transceiver contains two separate supply rails. The B port is designed to track V_{CCB}, which accepts voltages from 3 V to 5.5 V, and the A port is designed to track V_{CCA}, which operates at 2.3 V to 3.6 V. This allows for translation from a 3.3-V to a 5-V system environment and vice versa, or from a 2.5-V to a 3.3-V system environment and vice versa.

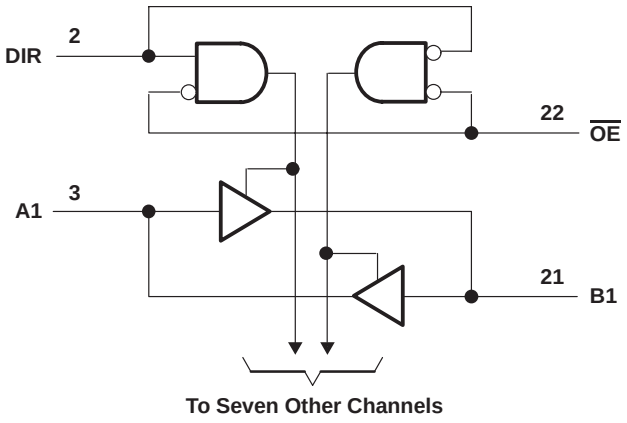
The SN74LVCC3245A is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so the buses are effectively isolated.

The SN74LVCC3245A is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CCA} and V_{CCB} . . . . . –0.5 V to 6 V
Input voltage range, V_I: All A port (see Note 2) . . . . . –0.5 V to V_{CCA} + 0.5 V
All B port (see Note 1) . . . . . –0.5 V to V_{CCB} + 0.5 V
Except I/O ports (see Note 2) . . . . . –0.5 V to V_{CCA} + 0.5 V
Output voltage range, V_O (see Note 1): All A port . . . . . –0.5 V to V_{CCA} + 0.5 V
All B port . . . . . –0.5 V to V_{CCB} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) . . . . . –50 mA
Output clamp current, I_{OK} (V_O < 0) . . . . . –50 mA
Continuous output current, I_O . . . . . ±50 mA
Continuous current through V_{CCA}, V_{CCB}, or GND . . . . . ±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DB package . . . . . 104°C/W
DW package . . . . . 81°C/W
PW package . . . . . 120°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. This value is limited to 6 V maximum.
2. This value is limited to 4.6 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			V_{CCA}	V_{CCB}	MIN	NOM	MAX	UNIT
V_{CCA}	Supply voltage				2.3	3.3	3.6	V
V_{CCB}	Supply voltage				3	5	5.5	V
V_{IHA}	High-level input voltage	$V_{OB} \le 0.1$ V, $V_{OB} \ge V_{CCB} - 0.1$ V	2.3 V	3 V	1.7			V
			2.7 V	3 V	2			
			3 V	3.6 V	2			
			3.6 V	5.5 V	2			
V_{IHB}	High-level input voltage	$V_{OA} \le 0.1$ V, $V_{OA} \ge V_{CCA} - 0.1$ V	2.3 V	3 V	2			V
			2.7 V	3 V	2			
			3 V	3.6 V	2			
			3.6 V	5.5 V	3.85			
V_{ILA}	Low-level input voltage	$V_{OB} \le 0.1$ V, $V_{OB} \ge V_{CCB} - 0.1$ V	2.3 V	3 V			0.7	V
			2.7 V	3 V			0.8	
			3 V	3.6 V			0.8	
			3.6 V	5.5 V			0.8	
V_{ILB}	Low-level input voltage	$V_{OA} \le 0.1$ V, $V_{OA} \ge V_{CCA} - 0.1$ V	2.3 V	3 V			0.8	V
			2.7 V	3 V			0.8	
			3 V	3.6 V			0.8	
			3.6 V	5.5 V			1.65	
V_{IA}	Input voltage				0		V_{CCA}	V
V_{IB}	Input voltage				0		V_{CCB}	V
V_{OA}	Output voltage				0		V_{CCA}	V
V_{OB}	Output voltage				0		V_{CCB}	V
I_{OHA}	High-level output current		2.3 V	3 V			–8	mA
			2.7 V	3 V			–12	
			3.3 V	3 V			–24	
I_{OHB}	High-level output current		2.3 V	3.3 V			–12	mA
			2.7 V	3.3 V			–12	
			3.3 V	3 V			–24	
I_{OLA}	Low-level output current		2.3 V	3 V			8	mA
			2.7 V	3 V			12	
			3.3 V	3 V			24	
I_{OLB}	Low-level output current		2.3 V	3.3 V			12	mA
			2.7 V	3.3 V			12	
			3.3 V	3 V			24	
$\Delta t/\Delta v$	Input transition rise or fall rate				0		10	ns/V
T_A	Operating free-air temperature				–40		85	°C

NOTE 4: All unused inputs of the device must be held at the associated V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

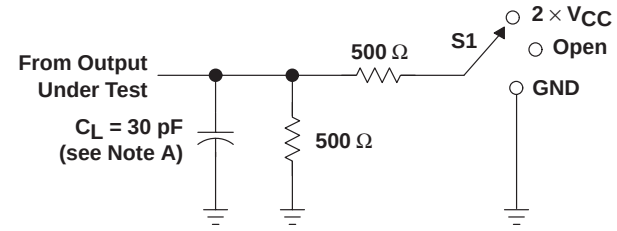
PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}	MIN	TYP	MAX	UNIT
V_{OHA}		I_{OH} = –100 μA	3 V	3 V	2.9	3		V
		I_{OH} = –8 mA	2.3 V	3 V	2			
		I_{OH} = –12 mA	2.7 V	3 V	2.2	2.5		
			3 V	3 V	2.4	2.8		
		I_{OH} = –24 mA	3 V	3 V	2.2	2.6		
			2.7 V	4.5 V	2	2.3		
V_{OHB}		I_{OH} = –100 μA	3 V	3 V	2.9	3		V
		I_{OH} = –12 mA	2.3 V	3 V	2.4			
			2.7 V	3 V	2.4	2.8		
		I_{OH} = –24 mA	3 V	3 V	2.2	2.6		
			2.7 V	4.5 V	3.2	4.2		
V_{OLA}		I_{OL} = 100 μA	3 V	3 V			0.1	V
		I_{OL} = 8 mA	2.3 V	3 V			0.6	
		I_{OL} = 12 mA	2.7 V	3 V		0.1	0.5	
		I_{OL} = 24 mA	3 V	3 V		0.2	0.5	
			2.7 V	4.5 V		0.2	0.5	
V_{OLB}		I_{OL} = 100 μA	3 V	3 V			0.1	V
		I_{OL} = 12 mA	2.3 V	3 V			0.4	
		I_{OL} = 24 mA	3 V	3 V		0.2	0.5	
				4.5 V		0.2	0.5	
I_I	Control inputs	V_I = V_{CCA} or GND	3.6 V	3.6 V		±0.1	±1	μA
				5.5 V		±0.1	±1	
I_{OZ}†	A or B ports	V_O = $V_{CCA/B}$ or GND, V_I = V_{IL} or V_{IH}	3.6 V	3.6 V		±0.5	±5	μA
I_{CCA}	B to A	A port = V_{CCA} or GND, I_O = 0	3.6 V	Open		5	50	μA
		B port = V_{CCB} or GND, I_O = 0		3.6 V		5	50	
				5.5 V		5	50	
I_{CCB}	A to B	A port = V_{CCA} or GND, I_O = 0	3.6 V	3.6 V		5	50	μA
				5.5 V		8	80	
ΔI_{CCA}‡	A port	V_I = V_{CCA} – 0.6 V, Other inputs at V_{CCA} or GND, $\overline{OE}$ at GND and DIR at V_{CCA}	3.6 V	3.6 V		0.35	0.5	mA
	$\overline{OE}$	V_I = V_{CCA} – 0.6 V, Other inputs at V_{CCA} or GND, DIR at V_{CCA}	3.6 V	3.6 V		0.35	0.5	
	DIR	V_I = V_{CCA} – 0.6 V, Other inputs at V_{CCA} or GND, $\overline{OE}$ at GND	3.6 V	3.6 V		0.35	0.5	
ΔI_{CCB}‡	B port	V_I = V_{CCB} – 2.1 V, Other inputs at V_{CCB} or GND, $\overline{OE}$ at GND and DIR at GND	3.6 V	5.5 V		1	1.5	mA
C_i	Control inputs	V_I = V_{CCA} or GND	Open	Open		4		pF
C_{io}	A or B ports	V_O = $V_{CCA/B}$ or GND	3.3 V	5 V		18.5		pF
C_{pd}	A to B	Outputs enabled	3.3 V	5 V		38		pF
	B to A	Outputs enabled	3.3 V	5 V		36.5		

† For I/O ports, the parameter I_{OZ} includes the input leakage current.
‡ This is the increase in supply current for each input that is at one of the specified voltage levels rather than 0 V or the associated V_{CC}.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 4)

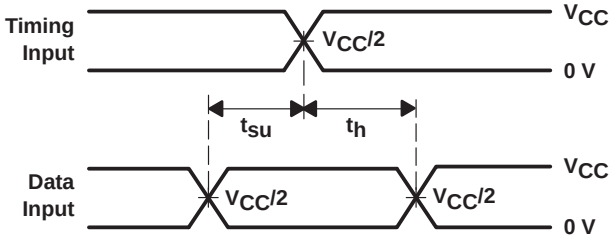
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCA} = 2.5 V ± 0.2 V, V_{CCB} = 3.3 V ± 0.3 V		V_{CCA} = 2.7 V TO 3.6 V, V_{CCB} = 5 V ± 0.5 V		V_{CCA} = 2.7 V TO 3.6 V, V_{CCB} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{PHL}	A	B	1	9.4	1	6	1	7.1	ns
t_{PLH}			1	9.1	1	5.3	1	7.2	
t_{PHL}	B	A	1	11.2	1	5.8	1	6.4	ns
t_{PLH}			1	9.9	1	7	1	7.6	
t_{PZL}	$\overline{OE}$	A	1	14.5	1	9.2	1	9.7	ns
t_{PZH}			1	12.9	1	9.5	1	9.5	
t_{PZL}	$\overline{OE}$	B	1	13	1	8.1	1	9.2	ns
t_{PZH}			1	12.8	1	8.4	1	9.9	
t_{PLZ}	$\overline{OE}$	A	1	7.1	1	5.5	1	6.6	ns
t_{PHZ}			1	6.9	1	7.8	1	6.9	
t_{PLZ}	$\overline{OE}$	B	1	8.8	1	7.3	1	7.5	ns
t_{PHZ}			1	8.9	1	7	1	7.9	

PARAMETER MEASUREMENT INFORMATION FOR A PORT
V_{CCA} = 2.5 V ± 0.2 V AND V_{CCB} = 3.3 V ± 0.3 V

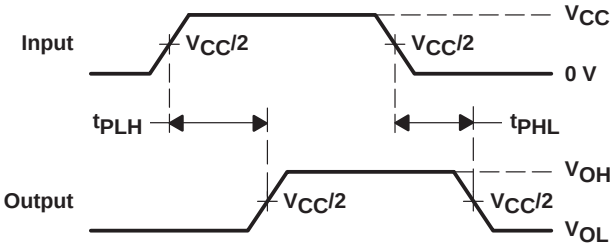


TEST	S1
t_{pd} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open 2 × V_{CC} GND

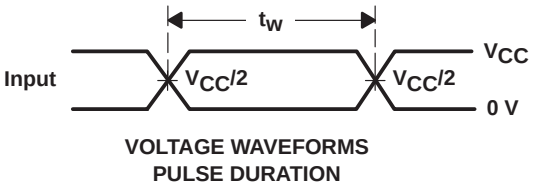
LOAD CIRCUIT



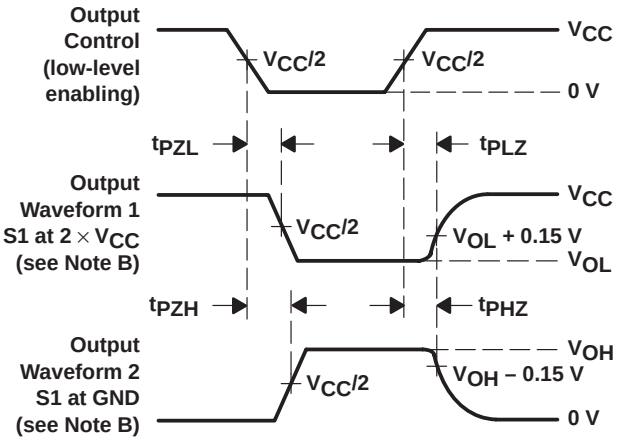
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION

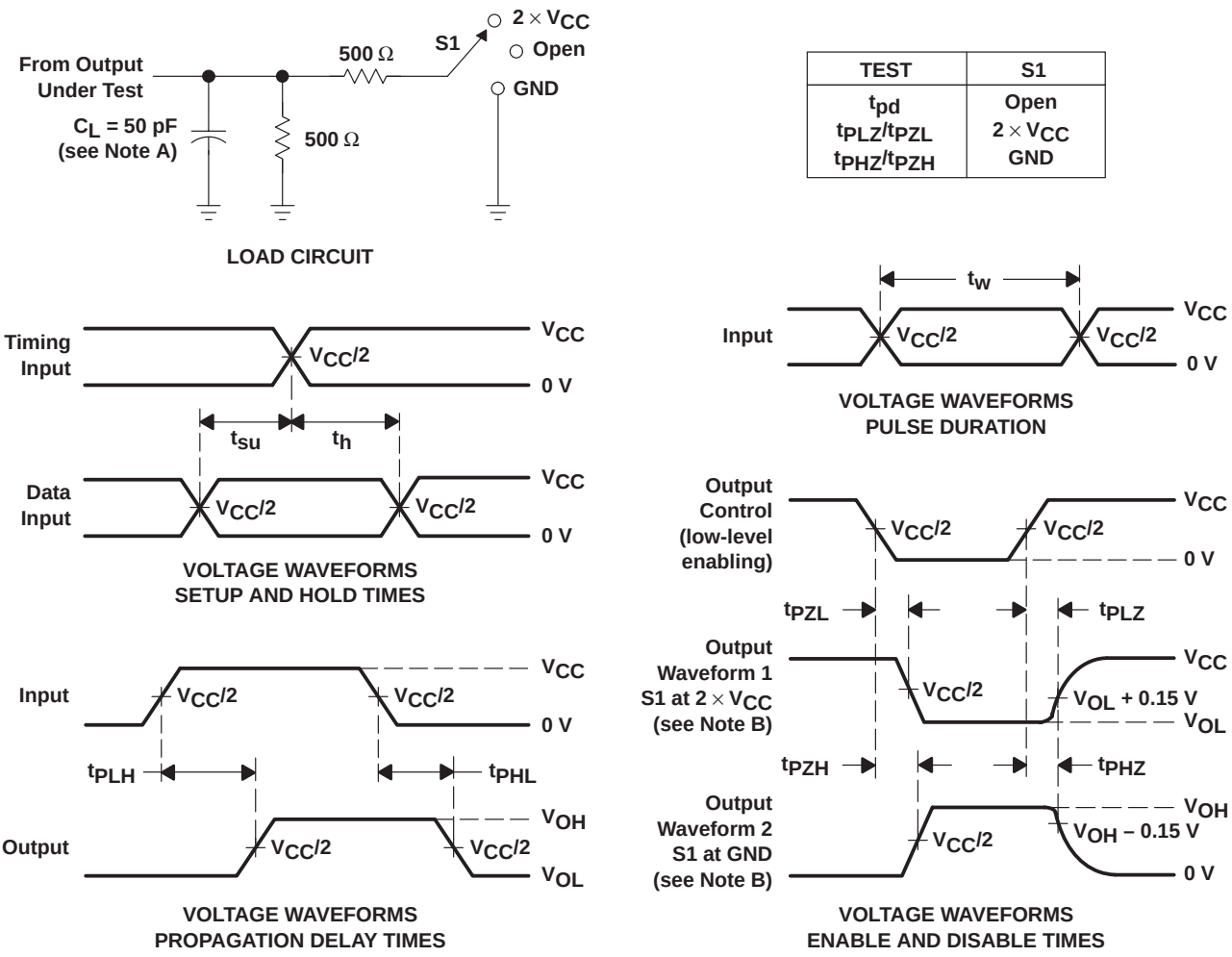


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

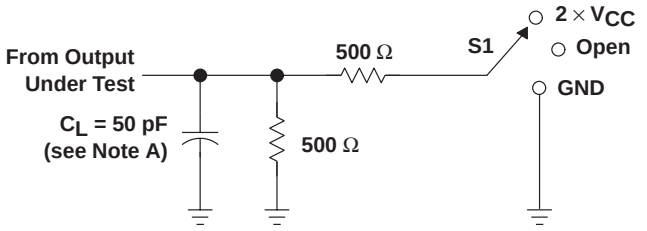
PARAMETER MEASUREMENT INFORMATION FOR B PORT
V_{CCA} = 2.5 V ± 0.2 V AND V_{CCB} = 3.3 V ± 0.3 V



NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

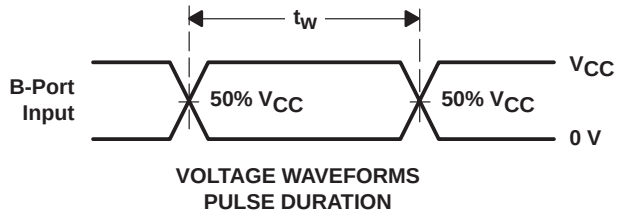
Figure 2. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION FOR B PORT
V_{CCA} = 3.6 V AND V_{CCB} = 5.5 V

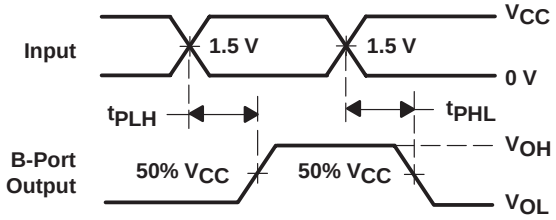


LOAD CIRCUIT

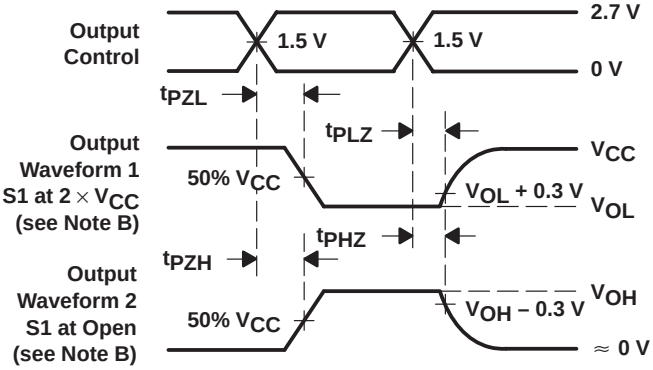
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	Open



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
NONINVERTING OUTPUTS

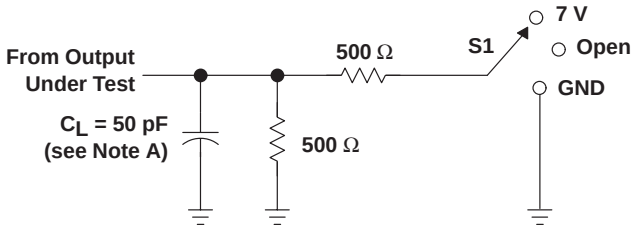


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

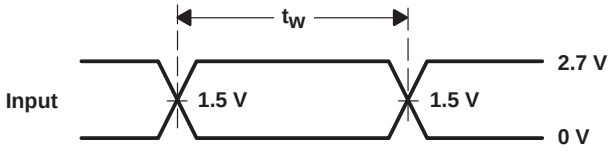
Figure 3. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION FOR A AND B PORT
V_{CCA} AND V_{CCB} = 3.6 V

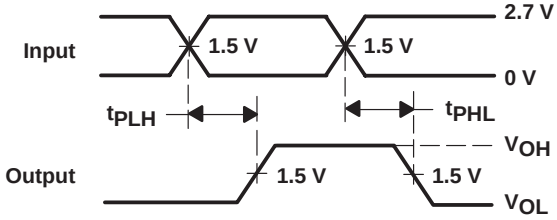


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

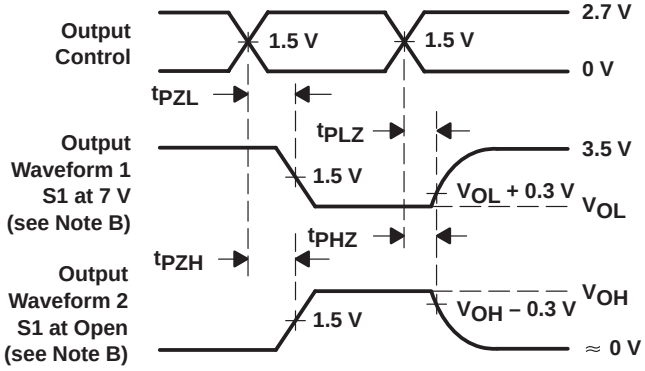
LOAD CIRCUIT



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 4. Load Circuit and Voltage Waveforms

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.