19-2966; Rev 0; 10/03

EVALUATION KIT AVAILABLE

MAXIM

Dual 180° Out-of-Phase Buck Controllers with Sequencing/Prebias Startup and POR

General Description

The MAX1858A/MAX1875A/MAX1876A dual, synchronized, step-down controllers generate two outputs from input supplies ranging from 4.5V to 23V. Each output is adjustable from sub-1V to 18V and supports loads of 10A or higher. Input voltage ripple and total RMS input ripple current are reduced by synchronized 180° out-of-phase operation.

The switching frequency is adjustable from 100kHz to 600kHz with an external resistor. Alternatively, the controller can be synchronized to an external clock generated by another MAX1858A/MAX1875A/MAX1876A or a system clock. One MAX1858A/MAX1875A/MAX1876A can be set to generate an in-phase, or 90° out-of-phase, clock signal for synchronization with additional controllers. This allows two controllers to operate either as an interleaved two- or four-phase system with each output shifted by 90°. The MAX1858A/MAX1875A/MAX1876A feature soft-start. The MAX1858A also features first-on/last-off power sequencing and soft-stop.

The MAX1858A/MAX1875A/MAX1876A eliminate the need for current-sense resistors by utilizing the low-side MOSFET's on-resistance as a current-sense element. This protects the DC-DC components from damage during output-overload conditions or output short-circuit faults without requiring a current-sense resistor. Adjustable foldback current limit reduces power dissipation during short-circuit conditions. The MAX1858A/MAX1876A include a power-on reset (POR) output to signal the system when both outputs reach regulation.

The MAX1858A/MAX1875A/MAX1876A ensure that the output voltage does not swing negative when the input power is removed or when EN is driven low. The MAX1875A/MAX1876A also allow prebias startup without discharging the output.

The MAX1858A/MAX1875A/MAX1876A are available in a 24-pin QSOP package. Use the MAX1875 evaluation kit or the MAX1858 evaluation kit to evaluate the MAX1858A/MAX1875A/MAX1876A.

Applications

Network Power Supplies

Telecom Power Supplies

DSP, ASIC, and FPGA Power Supplies

Set-Top Boxes

Broadband Routers

Servers

Desknote Computers

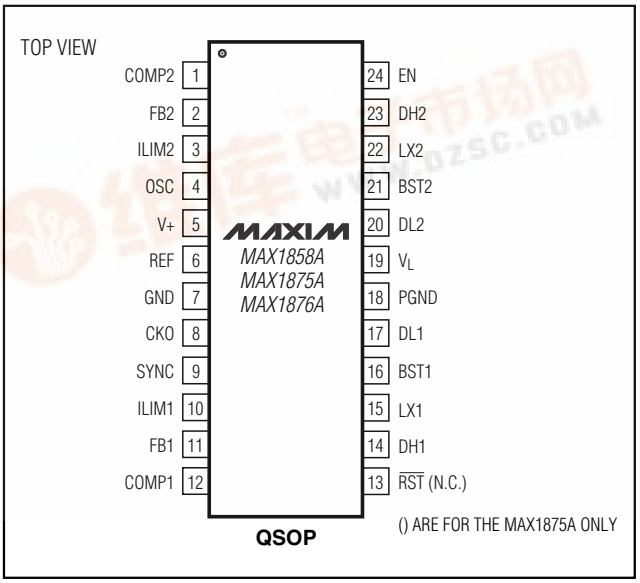
Features

- ♦ 4.5V to 23V Input Supply Range
- ♦ 0 to 18V Output Voltage Range (Up to 10A)
- ♦ Adjustable Lossless Foldback Current Limit
- ♦ Adjustable 100kHz to 600kHz Switching Frequency
- ♦ Optional Synchronization
- ♦ Clock Output for Master/Slave Synchronization
- ♦ 4 x 90° Out-of-Phase Step-Down Converters (Using Two Controllers, Figure 7)
- ♦ Prebias Startup (MAX1875A/MAX1876A)
- ♦ Power Sequencing (MAX1858A)
- ♦ $\overline{RST}$ Output with 140ms Minimum Delay (MAX1858A/MAX1876A)
- ♦ Fixed-Frequency Pulse-Width Modulation (PWM) Operation

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX1858AEEG	-40°C to +85°C	24 QSOP
MAX1875AEEG	-40°C to +85°C	24 QSOP
MAX1876AEEG	-40°C to +85°C	24 QSOP

Pin Configuration



Dual 180° Out-of-Phase Buck Controllers with Sequencing/Prebias Startup and POR

ABSOLUTE MAXIMUM RATINGS

V+ to GND .....-0.3V to +25V
PGND to GND .....-0.3V to +0.3V
V_L to GND .....-0.3V to the lower of +6V and (V+ + 0.3V)
BST1, BST2 to GND .....-0.3V to +30V
LX1 to BST1 .....-6V to +0.3V
LX2 to BST2 .....-6V to +0.3V
DH1 to LX1 .....-0.3V to (V_{BST1} + 0.3V)
DH2 to LX2 .....-0.3V to (V_{BST2} + 0.3V)
DL1, DL2 to PGND .....-0.3V to (V_L + 0.3V)
CKO, REF, OSC, ILIM1, ILIM2, COMP1, COMP2 to GND .....-0.3V to (V_L + 0.3V)
FB1, FB2, $\overline{RST}$, SYNC, EN to GND .....-0.3V to +6V
VL to GND Short Circuit .....Continuous
REF to GND Short Circuit .....Continuous
Continuous Power Dissipation (T_A = +70°C)
24-Pin QSOP (derate 9.4mW/°C above +70°C) 762mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = 12V, EN = ILIM_ = V_L, SYNC = GND, I_{VL} = 0mA, PGND = GND, C_{REF} = 0.22µF, C_{VL} = 4.7µF (ceramic), R_{OSC} = 60kΩ, compensation components for COMP_ are from Figure 1, **T_A = -40°C to +85°C** (Note 1), unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
GENERAL						
V+ Operating Range	(Note 2)		4.5		23.0	V
	V_L = V+ (Note 2)		4.5		5.5	
V+ Operating Supply Current	V_L unloaded, no MOSFETs connected			3.5	6	mA
V+ Standby Supply Current	EN = LX_ = FB_ = 0V			0.3	0.6	mA
Thermal Shutdown	Rising temperature, typical hysteresis = 10°C			+160		°C
Current-Limit Threshold	PGND - LX_	ILIM_ = V_L	75	100	125	mV
		$R_{ILIM\_}$ = 100kΩ	32	50	62	
		$R_{ILIM\_}$ = 600kΩ	225	300	375	
V_L REGULATOR						
Output Voltage	5.5V < V+ < 23V, 1mA < I_{LOAD} < 50mA		4.75	5	5.25	V
V_L Undervoltage Lockout Rising Trip Level			4.1	4.2	4.3	V
V_L Undervoltage Lockout Hysteresis	(Note 3)			100		mV
REFERENCE						
Output Voltage	I_{REF} = 0µA		1.98	2.00	2.02	V
Reference Load Regulation	0µA < I_{REF} < 50µA		0	4	10	mV
SOFT-START						
Digital Ramp Period	Internal 6-bit DAC for one converter to ramp from 0V to full scale (Note 4)			1024		DC-DC clocks
Soft-Start Steps				64		Steps
FREQUENCY						
Low End of Range	R_{OSC} = 60kΩ	0°C to +85°C	84	100	115	kHz
		-40°C to +85°C	80	100	120	
High End of Range	R_{OSC} = 10kΩ		540	600	660	kHz
DH_ Minimum Off-Time	R_{OSC} = 10kΩ			250	303	ns

ELECTRICAL CHARACTERISTICS (continued)

(V+ = 12V, EN = ILIM_ = V_L, SYNC = GND, I_{VL} = 0mA, PGND = GND, C_{REF} = 0.22µF, C_{VL} = 4.7µF (ceramic), R_{OSC} = 60kΩ, compensation components for COMP_ are from Figure 1, **T_A = -40°C to +85°C** (Note 1), unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SYNC Range	Switching frequency must be set to half of the SYNC frequency		200		1200	kHz
SYNC Input Pulse Width	(Note 4)	High	100			ns
		Low	100			
SYNC Rise/Fall Time	(Note 4)				100	ns
ERROR AMPLIFIER						
FB_ Input Bias Current					250	nA
FB_ Input Voltage Set Point	0°C to +85°C		0.985	1.00	1.015	V
	-40°C to +85°C		0.98	1.00	1.02	
FB_ to COMP_ Transconductance	0°C to +85°C		1.25	1.8	2.70	mS
	-40°C to +85°C		1.2	1.8	2.9	
DRIVERS						
DL_, DH_ Break-Before-Make Time	C_{LOAD} = 5nF			30		ns
DH_ On-Resistance	Low			1.5	2.5	Ω
	High			3	5	
DL_ On-Resistance	Low			0.6	1.5	Ω
	High			3	5	
LOGIC INPUTS (EN, SYNC)						
Input Low Level	Typical 15% hysteresis, V_L = 4.5V				0.8	V
Input High Level	V_L = 5.5V		2.4			V
Input High/Low Bias Current	V_{EN} = 0 or 5.5V		-1	+0.1	+1	µA
LOGIC OUTPUTS (CKO)						
Output Low Level	V_L = 5V, sinking 5mA				0.4	V
Output High Level	V_L = 5V, sourcing 5mA		4.0			V
COMP_						
Pulldown Resistance During Shutdown and Current Limit				17		Ω
$\overline{RST}$ OUTPUT (MAX1858A/MAX1876A ONLY)						
Output-Voltage Trip Level	Both FBs must be over this to allow the reset timer to start; there is no hysteresis		0.87	0.9	0.93	V
Output Low Level	V_L = 5V, sinking 3.2mA				0.4	V
	V_L = 1V, sinking 0.4mA				0.3	
Output Leakage	V+ = V_L = 5V, $V_{\overline{RST}}$ = 5.5V, V_{FB} = 1V				1	µA
Reset Timeout Period	$V_{FB\_}$ = 1V		140	315	560	ms
FB_ to Reset Delay	FB_ overdrive from 1V to 0.85V			4		µs

Note 1: Specifications to -40°C are guaranteed by design and not production tested.

Note 2: Operating supply range is guaranteed by V_L line regulation test. Connect V+ to V_L for 5V operation.

Note 3: When V_L falls and UVLO is tripped, the device is latched and V_L must be discharged below 2.5V before normal operation can resume.

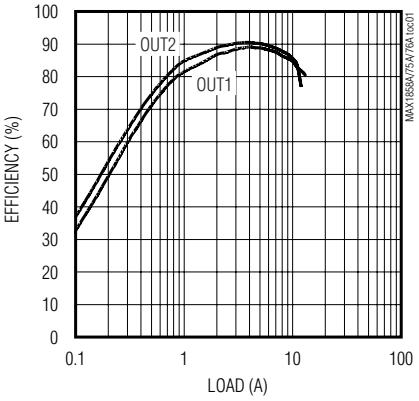
Note 4: Guaranteed by design and not production tested.

Dual 180° Out-of-Phase Buck Controllers with Sequencing/Prebias Startup and POR

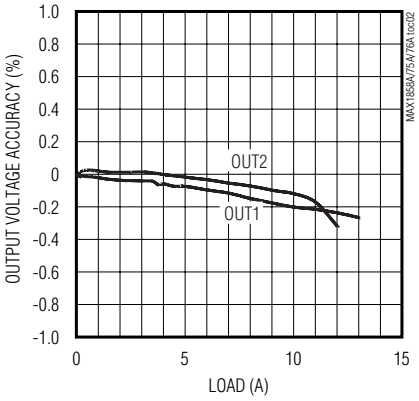
Typical Operating Characteristics

(Circuit of Figure 1, V_{IN} = 12V, T_A = +25°C, unless otherwise noted.)

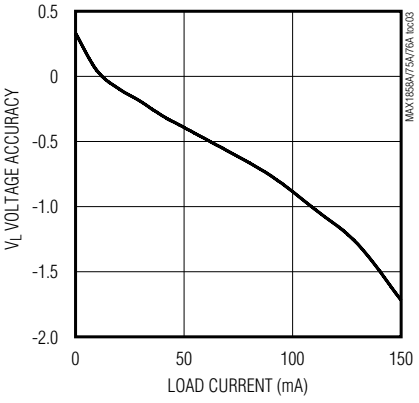
EFFICIENCY vs. LOAD



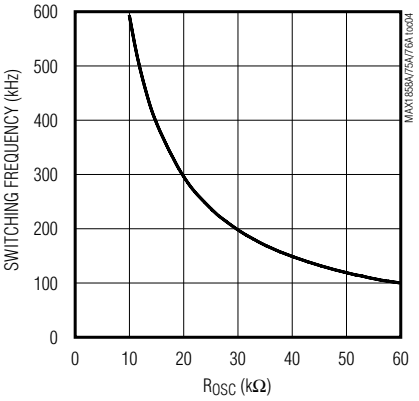
OUTPUT VOLTAGE ACCURACY vs. LOAD



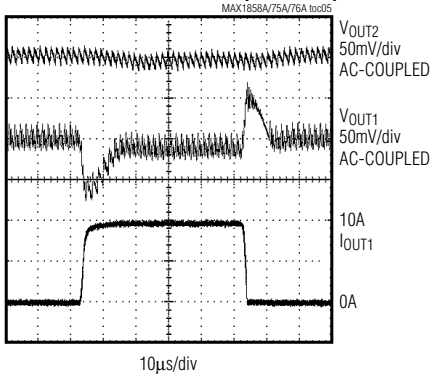
V_L VOLTAGE ACCURACY vs. LOAD CURRENT



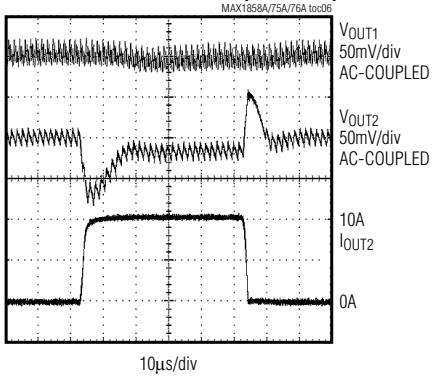
SWITCHING FREQUENCY vs. R_{OSC}



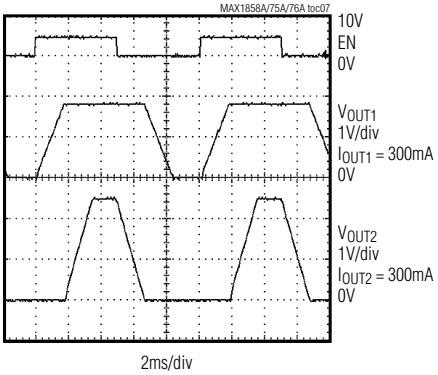
LOAD TRANSIENT RESPONSE (OUTPUT 1)



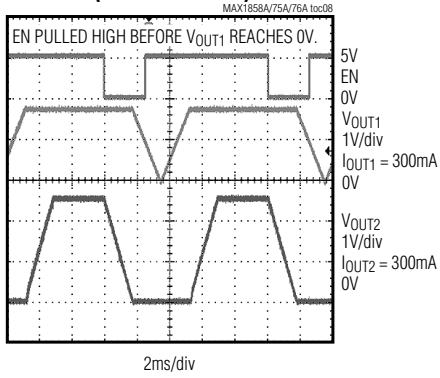
LOAD TRANSIENT RESPONSE (OUTPUT 2)



SOFT-START AND SOFT-STOP WAVEFORM (MAX1858A ONLY)



SOFT-START AND SOFT-STOP WAVEFORM (MAX1858A ONLY)

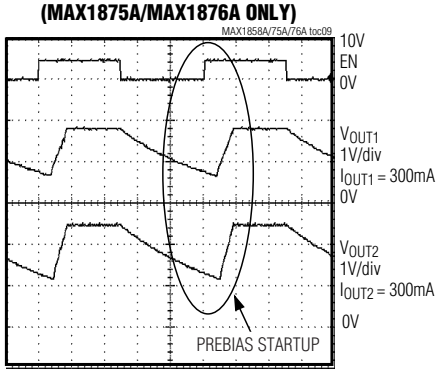


Dual 180° Out-of-Phase Buck Controllers with Sequencing/Prebias Startup and POR

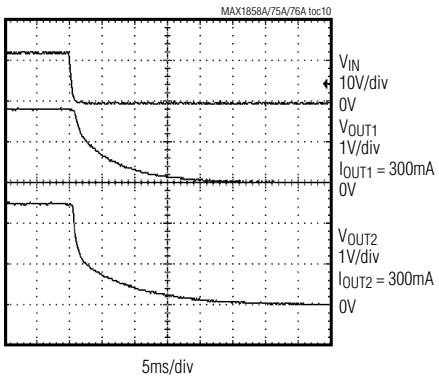
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{IN} = 12V, T_A = +25°C, unless otherwise noted.)

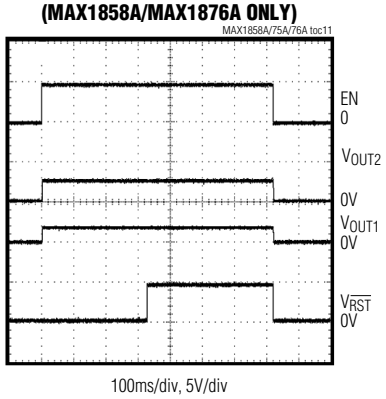
START AND STOP WAVEFORM (MAX1875A/MAX1876A ONLY)



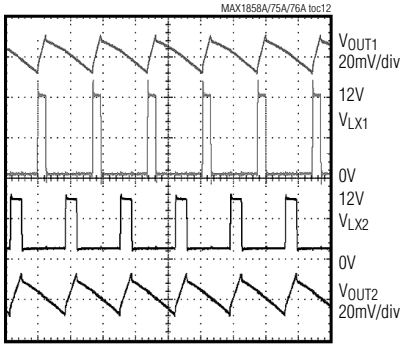
INPUT POWER REMOVAL



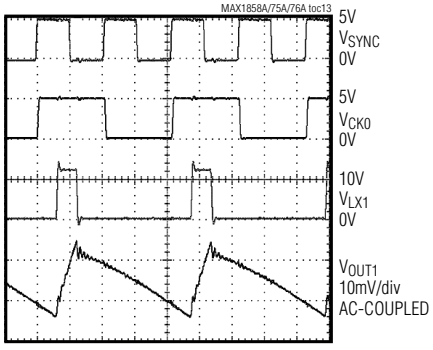
RESET TIMEOUT (MAX1858A/MAX1876A ONLY)



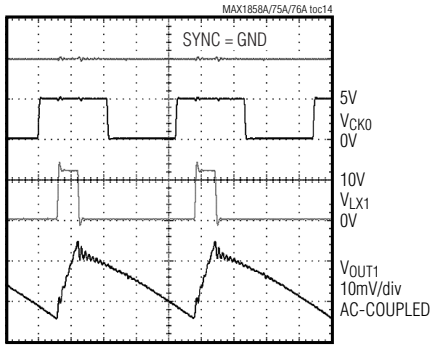
OUT-OF-PHASE WAVEFORM



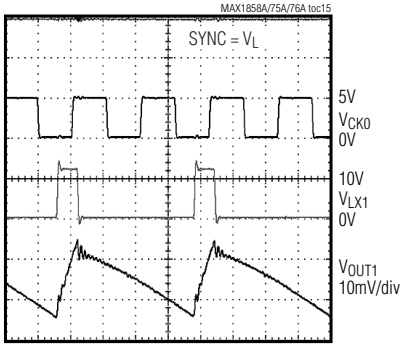
EXTERNALLY SYNCHRONIZED SWITCHING WAVEFORM



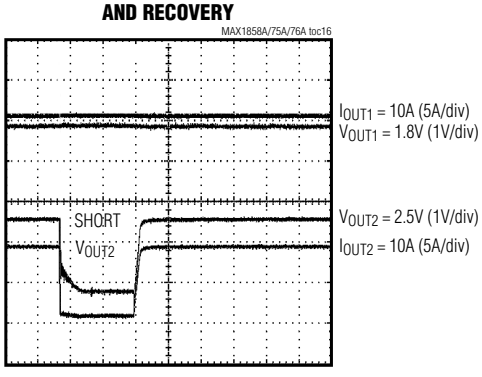
CKO OUTPUT WAVEFORM



CKO OUTPUT WAVEFORM



SHORT-CIRCUIT CURRENT FOLDBACK AND RECOVERY



Dual 180° Out-of-Phase Buck Controllers with Sequencing/Prebias Startup and POR

Pin Description

PIN	NAME	FUNCTION
1	COMP2	Compensation Pin for Regulator 2 (REG2). Compensate REG2's control loop by connecting a series resistor (R_{COMP2}) and capacitor (C_{COMP2A}) to GND in parallel with a second compensation capacitor (C_{COMP2B}) as shown in Figure 1.
2	FB2	Feedback Input for Regulator 2 (REG2). Connect FB2 to a resistive divider between REG2's output and GND to adjust the output voltage between 1V and 18V. To set the output voltage below 1V, connect FB2 to a resistive voltage-divider from REF to REG2's output. See the *Setting the Output Voltage* section.
3	ILIM2	Current-Limit Adjustment for Regulator 2 (REG2). The PGND–LX2 current-limit threshold defaults to 100mV if ILIM2 is connected to V_L. Connect a resistor (R_{ILIM2}) from ILIM2 to GND to adjust the REG2's current-limit threshold (V_{ITH2}) from 50mV (R_{ILIM2} = 100kΩ) to 300mV (R_{ILIM2} = 600kΩ). See the *Setting the Valley Current Limit* section.
4	OSC	Oscillator Frequency Set Input. Connect a resistor from OSC to GND (R_{OSC}) to set the switching frequency from 100kHz (R_{OSC} = 60kΩ) to 600kHz (R_{OSC} = 10kΩ). The controller still requires R_{OSC} when an external clock is connected to SYNC. When using an external clock, select R_{OSC} as described above, and set the external clock frequency to twice the desired switching frequency.
5	V+	Input Supply Voltage. 4.5V to 23V.
6	REF	2V Reference Output. Bypass to GND with a 0.22µF or greater ceramic capacitor.
7	GND	Analog Ground
8	CKO	Clock Output. Clock output for external 2- or 4-phase synchronization (see the *Clock Synchronization (SYNC, CKO)* section).
9	SYNC	Synchronization Input or Clock Output Selection Input. SYNC has three operating modes. Connect SYNC to a 200kHz to 1200kHz clock for external synchronization. Connect SYNC to GND for 2-phase operation as a master controller. Connect SYNC to V_L for 4-phase operation as a master controller (see the *Clock Synchronization (SYNC, CKO)* section).
10	ILIM1	Current-Limit Adjustment for Regulator 1 (REG1). The PGND–LX1 current-limit threshold defaults to 100mV if ILIM1 is connected to V_L. Connect a resistor (R_{ILIM1}) from ILIM1 to GND to adjust REG1's current-limit threshold (V_{ITH1}) from 50mV (R_{ILIM1} = 100kΩ) to 300mV (R_{ILIM1} = 600kΩ). See the *Setting the Valley Current Limit* section.
11	FB1	Feedback Input for Regulator 1 (REG1). Connect FB1 to a resistive divider between REG1's output and GND to adjust the output voltage between 1V and 18V. To set the output voltage below 1V, connect FB1 to a resistive voltage-divider from REF and REG1's output. See the *Setting the Output Voltage* section.
12	COMP1	Compensation Pin for Regulator 1 (REG1). Compensate REG1's control loop by connecting a series resistor (R_{COMP1}) and capacitor (C_{COMP1A}) to GND in parallel with a second compensation capacitor (C_{COMP1B}) as shown in Figure 1.
13	$\overline{RST}$	Open-Drain Reset Output (MAX1858A/MAX1876A Only). $\overline{RST}$ is low when either output voltage is more than 10% below its regulation point. After soft-start is completed and both outputs exceed 90% of their nominal output voltage ($V_{FB\_}$ > 0.9V), $\overline{RST}$ becomes high impedance after a 140ms delay and remains high impedance as long as both outputs maintain regulation. Connect a resistor between $\overline{RST}$ and the logic supply for logic-level voltages.
	N.C.	Connect to GND or leave unconnected for the MAX1875A.

Pin Description (continued)

PIN	NAME	FUNCTION
14	DH1	High-Side Gate-Driver Output for Regulator 1 (REG1). DH1 swings from LX1 to BST1. DH1 is low during UVLO.
15	LX1	External Inductor Connection for Regulator 1 (REG1). Connect LX1 to the switched side of the inductor. LX1 serves as the lower supply rail for the DH1 high-side gate driver.
16	BST1	Boost Flying-Capacitor Connection for Regulator 1 (REG1). Connect BST1 to an external ceramic capacitor and diode according to Figure 1.
17	DL1	Low-Side Gate-Driver Output for Regulator 1 (REG1). DL1 swings from PGND to V_L. DL1 is low during UVLO.
18	PGND	Power Ground
19	V_L	Internal 5V Linear-Regulator Output. Supplies the regulators and powers the low-side gate drivers and external boost circuitry for the high-side gate drivers.
20	DL2	Low-Side Gate-Driver Output for Regulator 2 (REG2). DL2 swings from PGND to V_L. DL2 is low during UVLO.
21	BST2	Boost Flying-Capacitor Connection for Regulator 2 (REG2). Connect BST2 to an external ceramic capacitor and diode according to Figure 1.
22	LX2	External Inductor Connection for Regulator 2 (REG2). Connect LX2 to the switched side of the inductor. LX2 serves as the lower supply rail for the DH2 high-side gate driver.
23	DH2	High-Side Gate-Driver Output for Regulator 2 (REG2). DH2 swings from LX2 to BST2. DH2 is low during UVLO.
24	EN	Active-High Enable Input. A logic low shuts down both controllers. Connect to V_L for always-on operation.

Detailed Description

DC-DC PWM Controller

The MAX1858A/MAX1875A/MAX1876A step-down converters use a PWM voltage-mode control scheme (Figure 2) for each out-of-phase controller. The controller generates the clock signal by dividing down the internal oscillator or SYNC input when driven by an external clock, so each controller's switching frequency equals half the oscillator frequency ($f_{SW} = f_{OSC}/2$). An internal transconductance error amplifier produces an integrated error voltage at the COMP pin, providing high DC accuracy. The voltage at COMP sets the duty cycle using a PWM comparator and a ramp generator. At each rising edge of the clock, REG1's high-side N-channel MOSFET turns on and remains on until either the appropriate duty cycle or until the maximum duty cycle is reached. REG2 operates out-of-phase, so the second high-side MOSFET turns on at each falling edge of the clock. During each high-side MOSFET's on-time, the associated inductor current ramps up.

During the second-half of the switching cycle, the high-side MOSFET turns off and the low-side N-channel MOSFET turns on. Now the inductor releases the stored energy as its current ramps down, providing current to the output. Under overload conditions, when the inductor current exceeds the selected valley current limit (see the *Current-Limit Circuit (ILIM_)* section), the high-side MOSFET does not turn on at the appropriate clock edge and the low-side MOSFET remains on to let the inductor current ramp down.

Synchronized Out-of-Phase Operation

The two independent regulators in the MAX1858A/MAX1875A/MAX1876A operate 180° out-of-phase to reduce input filtering requirements, reduce electromagnetic interference (EMI), and improve efficiency. This effectively lowers component cost and saves board space, making the MAX1858A/MAX1875A/MAX1876A ideal for cost-sensitive applications.

Dual-switching regulators typically operate both controllers in-phase, and turn on both high-side MOSFETs at the same time. The input capacitor must then support the instantaneous current requirements of both controllers simultaneously, resulting in increased ripple voltage and current when compared to a single switching regulator. The higher RMS ripple current lowers efficiency due to power loss associated with the input capacitor's effective series resistance (ESR). This typically requires more low-ESR input capacitors in parallel to minimize input voltage ripple and ESR-related losses, or to meet the necessary ripple-current rating.

Dual 180° Out-of-Phase Buck Controllers with Sequencing/Prebias Startup and POR

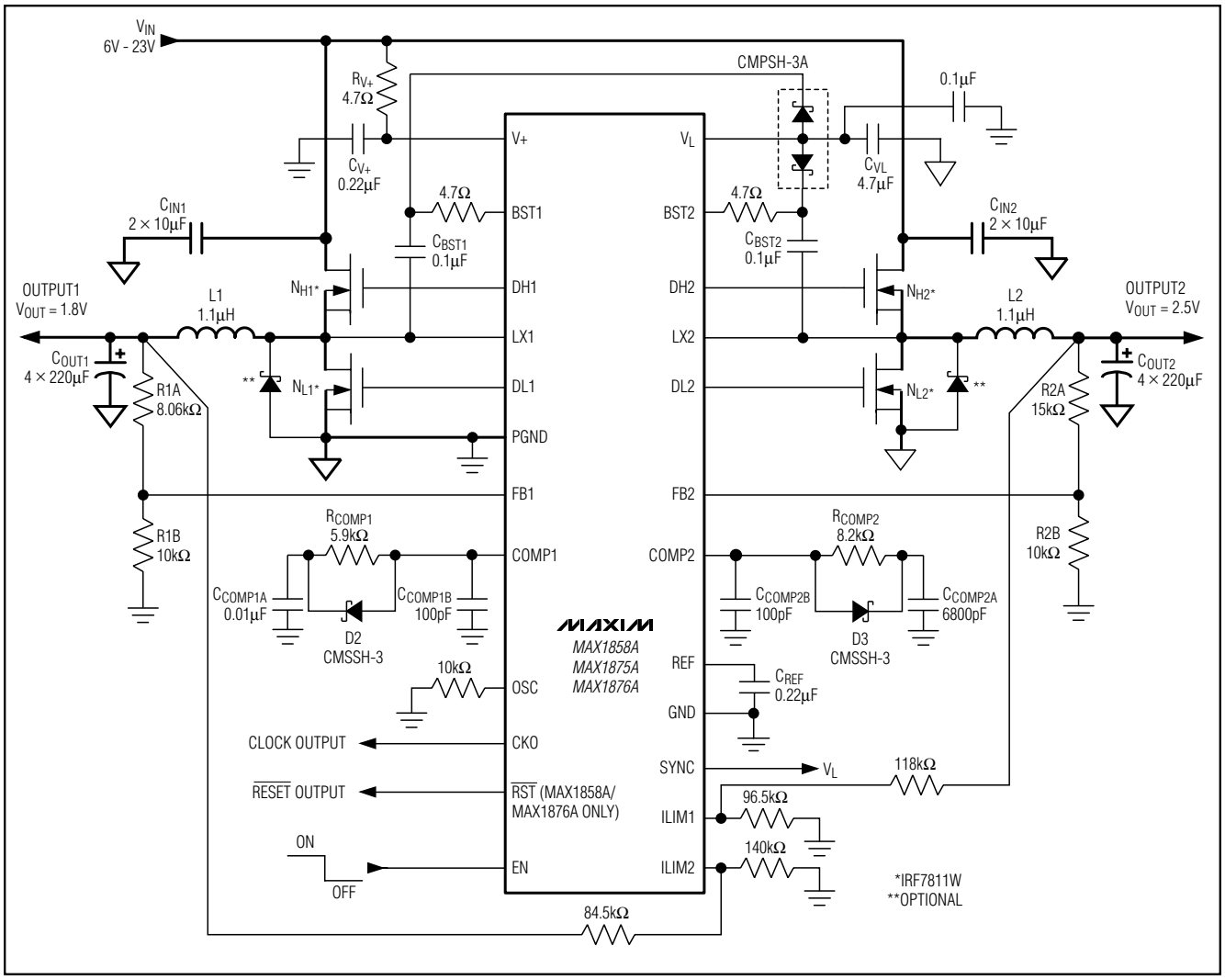


Figure 1. Standard 600kHz Application Circuit

With dual, synchronized, out-of-phase operation, the MAX1858A/MAX1875A/MAX1876As' high-side MOSFETs turn on 180° out-of-phase. The instantaneous input current peaks of both regulators no longer overlap, resulting in reduced RMS ripple current and input voltage ripple. This reduces the required input capacitor ripple-current rating, allowing fewer or less expensive capacitors, and reduces shielding requirements for EMI. The Out-of-Phase Waveforms in the *Typical Operating Characteristics* demonstrate synchronized 180° out-of-phase operation.

Internal 5V Linear Regulator (V_L)

All MAX1858A/MAX1875A/MAX1876A functions are internally powered from an on-chip, low-dropout 5V regulator. The maximum regulator input voltage (V+) is 23V. Bypass the regulator's output (V_L) with a 4.7µF ceramic capacitor to PGND. The V_L dropout voltage is typically 500mV, so when V+ is greater than 5.5V, V_L is typically 5V. The MAX1858A/MAX1875A/MAX1876A also employs an undervoltage lockout circuit that disables both regulators when V_L falls below 4.2V. V_L should also be bypassed to GND with a 0.1µF capacitor. When V_L falls and UVLO is tripped, the device is latched and V_L must be discharged below 2.5V before normal operation can resume.

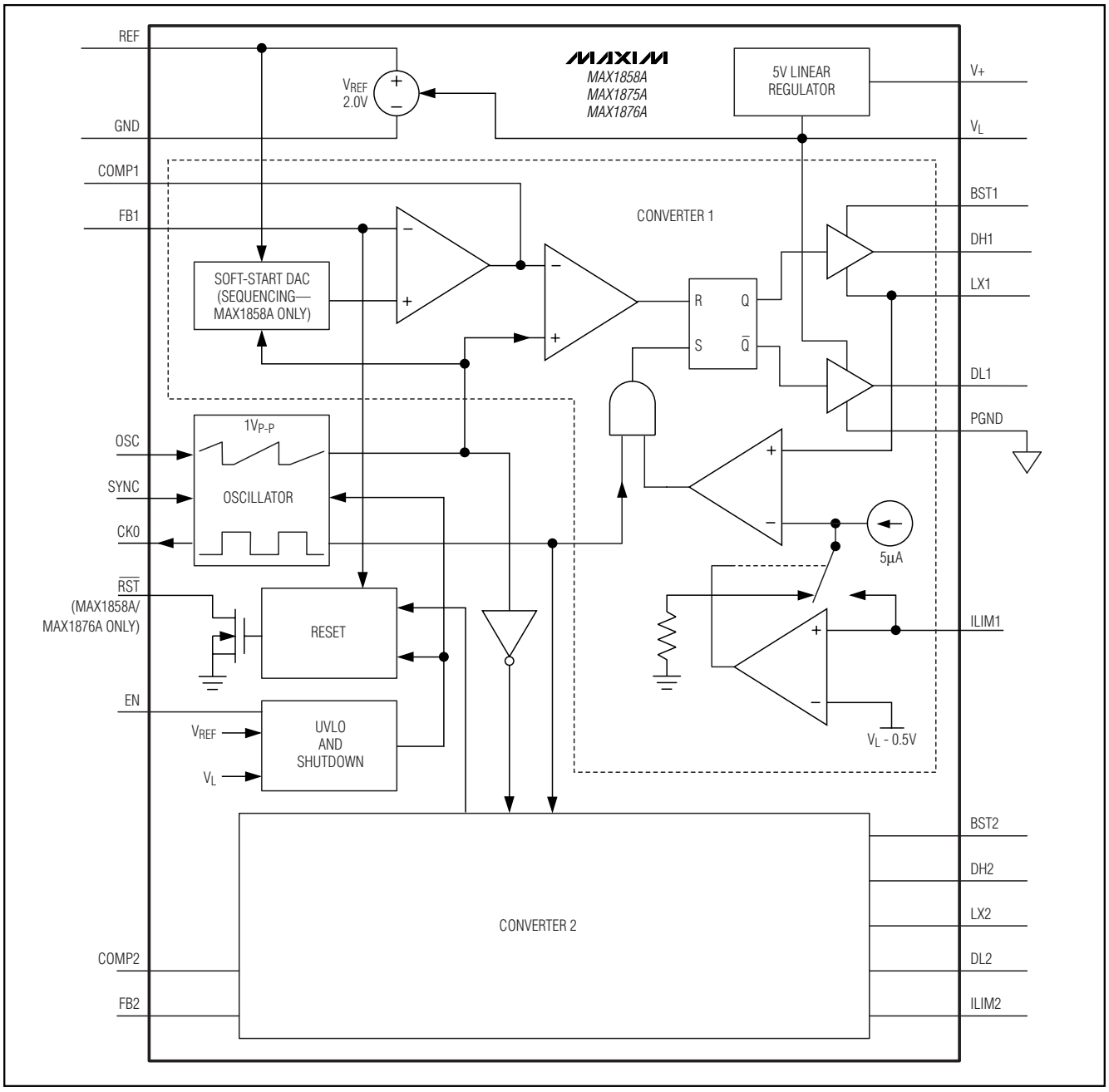
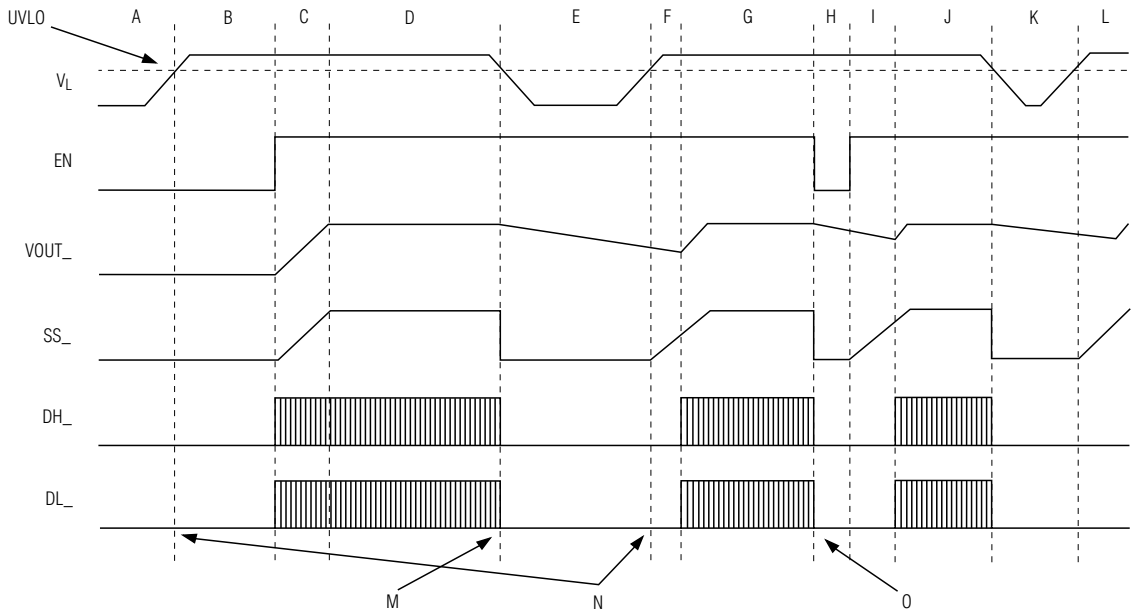


Figure 2. Functional Diagram

The internal V_L linear regulator can source over 50mA to supply the IC, power the low-side gate driver, charge the external boost capacitor, and supply small external loads. When driving large FETs, little or no regulator current may be available for external loads.

For example, when switched at 600kHz, a single large FET with 18nC total gate charge requires 18nC × 600kHz = 11mA. To drive larger MOSFETs, or deliver larger loads, connect V_L to an external power supply from 4.5V to 5.5V.

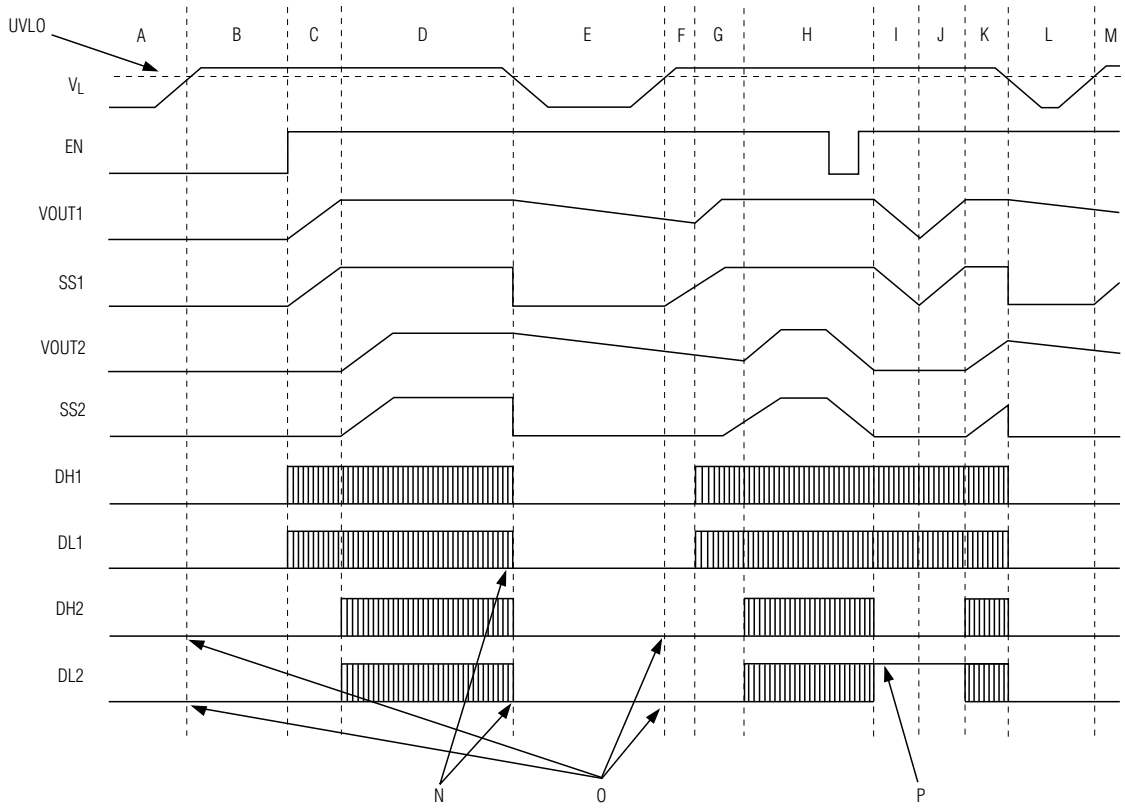
Dual 180° Out-of-Phase Buck Controllers with Sequencing/Prebias Startup and POR



MAX1875A/MAX1876A POWER-ON-OFF SEQUENCING DEFINITIONS

SYMBOL	DEFINITION
UVLO	Undervoltage lockout trip level is provided in the *Electrical Characteristics* table.
VL	Internal 5V Linear-Regulator Output
EN	Active-High Enable Input
VOUT_	Output Voltage
SS_	Internal Soft-Start Input Signal into Error Amplifier
DH_	High-Side Gate-Driver Output
DL_	Low-Side Gate-Driver Output
A	V_L rising while below the UVLO threshold. EN is low.
B	V_L is greater than the UVLO threshold. EN is low.
C	EN is pulled high.
D	Normal operation
E	V_L enters UVLO.
F	V_L exits UVLO.
G	Resumes normal operation
H	EN is pulled low.
I	EN is pulled high.
J	Resumes normal operation
K	V_L drops below UVLO threshold while EN is high.
L	Resumes normal operation
M	UVLO is activated and DL_ is latched low.
N	Exiting UVLO: DL_ remains latched low until the first fall of DH_ is detected.
O	DL_ is low after EN is pulled low.

Figure 3. MAX1875A/MAX1876A Detailed Power-On-Off Sequencing



MAX1858A POWER-ON-OFF SEQUENCING DEFINITIONS

SYMBOL	DEFINITION
UVLO	Undervoltage threshold value is provided in the *Electrical Characteristics* table.
V_L	Internal 5V Linear-Regulator Output
EN	Active-High Enable Input
VOUT1	Regulator 1 Output Voltage
SS1	Regulator 1: Internal Soft-Start Input Signal into Error Amplifier
VOUT2	Regulator 2 Output Voltage
SS2	Regulator 2: Internal Soft-Start Input Signal into Error Amplifier
DH1	Regulator 1: High-Side Gate-Driver Output
DL1	Regulator 1: Low-Side Gate-Driver Output
DH2	Regulator 2: High-Side Gate-Driver Output
DL2	Regulator 2: Low-Side Gate-Driver Output
A	V_L rising while below the UVLO threshold. EN is low.
B	V_L is greater than the UVLO threshold. EN is low.
C	EN is pulled high. DH1 and DL1 start switching. DH2 and DL2 are off.

SYMBOL	DEFINITION
D	Normal operation
E	V_L enters UVLO.
F	V_L exits UVLO.
G	Resumes normal operation. DH1 and DL1 start switching. DH2 and DL2 are off.
H	EN is pulled low and then high.
I	VOUT1 must reach 0V before restarting due to the cycling of the enable in region H (above).
J	VOUT1 recovers.
K	VOUT2 recovers.
L	V_L enters UVLO before VOUT2 fully recovers.
M	V_L exits UVLO.
N	UVLO latches DL_ low.
O	Exiting UVLO: DL_ remains latched low until the first fall of DH_ is detected.
P	DL_ is high after EN is pulled low and soft-stop is complete.

Figure 4. MAX1858A Detailed Power-On-Off Sequencing

Dual 180° Out-of-Phase Buck Controllers with Sequencing/Prebias Startup and POR

High-Side Gate-Drive Supply (BST_)

Gate-drive voltages for the high-side N-channel switches are generated by the flying-capacitor boost circuits (Figure 5). A boost capacitor (connected from BST_ to LX_) provides power to the high-side MOSFET driver.

On startup, the synchronous rectifier (low-side MOSFET) forces LX_ to ground and charges the boost capacitor to 5V. On the second half-cycle, after the low-side MOSFET turns off, the high-side MOSFET is turned on by closing an internal switch between BST_ and DH_. This provides the necessary gate-to-source voltage to turn on the high-side switch, an action that boosts the 5V gate-drive signal above V_{IN}. The current required to drive the high-side MOSFET gates ($f_{SWITCH} \times Q_G$) is ultimately drawn from V_L.

MOSFET Gate Drivers (DH_, DL_)

The DH and DL drivers are optimized for driving moderate-size N-channel high-side and larger low-side power MOSFETs. This is consistent with the low duty factor seen with large V_{IN} - V_{OUT} differential. The DL_ low-side drive waveform is always the complement of the DH_ high-side drive waveform (with controlled dead time to prevent cross-conduction or "shoot-through"). An adaptive dead-time circuit monitors the DL_ output and prevents the high-side FET from turning on until DL_ is fully off. There must be a low-resistance, low-inductance path from the DL_ driver to the MOSFET gate in order for the adaptive dead-time circuit to work properly. Otherwise, the sense circuitry in the MAX1858A/MAX1875A/MAX1876A interprets the MOSFET gate as "off" while there is actually charge still left on the gate. Use very short, wide traces (50mils to 100mils wide if the MOSFET is 1in from the device). The dead time at the DH-off edge is determined by a fixed 30ns internal delay.

Synchronous rectification reduces conduction losses in the rectifier by replacing the normal low-side Schottky catch diode with a low-resistance MOSFET switch. Additionally, the MAX1858A/MAX1875A/MAX1876A use the synchronous rectifier to ensure proper startup of the boost gate-driver circuit and to provide the current-limit signal.

The internal pulldown transistor that drives DL_ low is robust, with a 0.5Ω (typ) on-resistance. This low on-resistance helps prevent DL_ from being pulled up during the fast rise time of the LX_ node, due to capacitive coupling from the drain to the gate of the low-side synchronous-rectifier MOSFET. However, for high-current applications, some combinations of high- and low-side FETs can cause excessive gate-drain coupling, leading to poor efficiency, EMI, and shoot-through currents. This can be remedied by adding a resistor (typically less than 5Ω) in series with BST_, which increases the turn-on time of the high-side FET without degrading the turn-off time (Figure 5).

Current-Limit Circuit (ILIM_)

The current-limit circuit employs a "valley" current-sensing algorithm that uses the on-resistance of the low-side MOSFET as a current-sensing element. If the current-sense signal is above the current-limit threshold, the MAX1858A/MAX1875A/MAX1876A do not initiate a new cycle (Figure 6). Since valley current sensing is employed, the actual peak current is greater than the current-limit threshold by an amount equal to the inductor ripple current. Therefore, the exact current-limit characteristic and maximum load capability are a function of the low-side MOSFET's on-resistance, current-limit threshold, inductor value, and input voltage. The reward for this uncertainty is robust, lossless overcurrent sensing that does not require costly sense resistors.

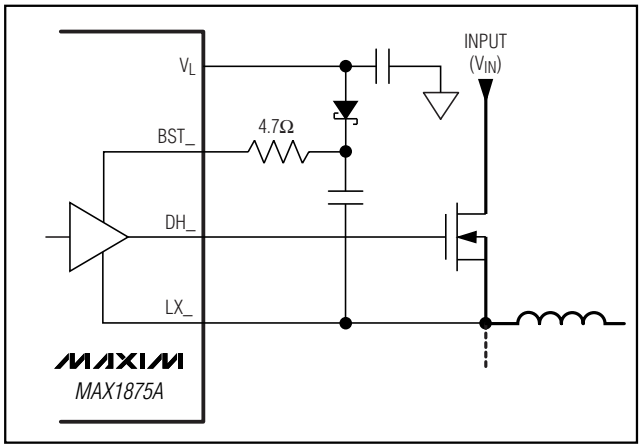


Figure 5. Reducing the Switching-Node Rise Time

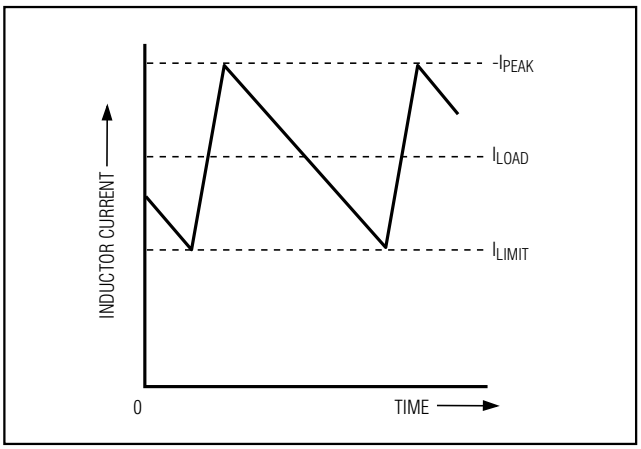


Figure 6. "Valley" Current-Limit Threshold Point

The adjustable current limit accommodates MOSFETs with a wide range of on-resistance characteristics (see the *Design Procedure* section). The current-limit threshold is adjusted with an external resistor at ILIM_ (Figure 1). The adjustment range is from 50mV to 300mV, corresponding to resistor values of 100kΩ to 600kΩ. In adjustable mode, the current-limit threshold across the low-side MOSFET is precisely 1/10th the voltage seen at ILIM_. However, the current-limit threshold defaults to 100mV when ILIM is tied to V_L. The logic threshold for switchover to this 100mV default value is approximately V_L - 0.5V.

Adjustable foldback current limit reduces power dissipation during short-circuit conditions (see the *Design Procedure* section).

Carefully observe the PC board layout guidelines to ensure that noise and DC errors do not corrupt the current-sense signals seen by LX_ and PGND. The IC must be mounted close to the low-side MOSFET with short, direct traces making a Kelvin-sense connection so that trace resistance does not add to the intended sense resistance of the low-side MOSFET.

Undervoltage Lockout and Startup

IF V_L drops below 4.2V, the MAX1858A/MAX1875A/MAX1876A assume that the input supply and reference voltages are too low to make valid decisions and activate the undervoltage lockout (UVLO) circuitry, which latches DL and DH low to inhibit switching. $\overline{RST}$ is also forced low during UVLO. To reset the latch and be ready for the next V_L rise, V_L must be pulled below 2.5V.

In addition, to ensure proper startup, the value of the capacitor at REF to GND must meet the following condition:

$$C_{REF} > ((8.29 \times 10^{-4}) / V_{+\_SLOPE}) - (1.97 \times 10^{-1} / f_{S\_MAX})$$

where V_{+_SLOPE} is the actual input-voltage rise time's slew rate.

For example, if the switching frequency is set at 600kHz nominal, which is 660kHz (max), and the input-voltage rise time's slew rate is 1.6V/mS, then C_{REF} should be greater than 0.22µF. Make sure C_{REF} is chosen large enough to cover for worst-case capacitance tolerances and temperature coefficient.

Enable (EN), Soft-Start, and Soft-Stop

Pull EN high to enable or low to shut down both regulators. See the timing diagrams, Figures 3 and 4, for more detail.

Output-Voltage Sequencing

After the startup circuitry enables the controller, the MAX1858A begins the startup sequence. Regulator 1 (OUT1) powers up with soft-start enabled. Once the first converter's soft-start sequence ends, regulator 2 (OUT2) powers up with soft-start enabled. Finally, when both converters complete soft-start and both output voltages exceed 90% of their nominal values, the reset output ($\overline{RST}$) goes high (see the *Reset Output* section). Soft-stop is initiated by pulling EN low. Soft-stop occurs in reverse order of soft-start, allowing last-on/first-off operation.

Reset Output ($\overline{RST}$) (MAX1858A/MAX1876A Only)

$\overline{RST}$ is an open-drain output. $\overline{RST}$ pulls low when either output falls below 90% of its nominal regulation voltage. Once both outputs exceed 90% of their nominal regulation voltages and both soft-start cycles are completed, $\overline{RST}$ goes high impedance. To obtain a logic-voltage output, connect a pullup resistor from $\overline{RST}$ to the logic supply voltage. A 100kΩ resistor works well for most applications. If unused, leave $\overline{RST}$ grounded or unconnected.

Clock Synchronization (SYNC, CKO)

SYNC serves two functions: SYNC selects the clock output (CKO) type used to synchronize slave controllers, or it serves as a clock input so the MAX1858A/MAX1875A/MAX1876A can be synchronized with an external clock signal. This allows the MAX1858A/MAX1875A/MAX1876A to function as either a master or slave. CKO provides a clock signal synchronized to the MAX1858A/MAX1875A/MAX1876As' switching frequency, allowing either in-phase (SYNC = GND) or 90° out-of-phase (SYNC = V_L) synchronization of additional DC-DC controllers (Figure 7). The MAX1858A/MAX1875A/MAX1876A support the following three operating modes:

- **SYNC = GND:** The CKO output frequency equals REG1's switching frequency ($f_{CKO} = f_{DH1}$) and the CKO signal is in phase with REG1's switching frequency. This provides 2-phase operation when synchronized with a second slave controller.
- **SYNC = V_L:** The CKO output frequency equals two times REG1's switching frequency ($f_{CKO} = 2f_{DH1}$) and the CKO signal is phase shifted by 90° with respect to REG1's switching frequency. This provides 4-phase operation when synchronized with a second MAX1858A/MAX1875A/MAX1876A (slave controller).

Dual 180° Out-of-Phase Buck Controllers with Sequencing/Prebias Startup and POR

- **SYNC Driven by External Oscillator:** The controller generates the clock signal by dividing down the SYNC input signal, so that the switching frequency equals half the synchronization frequency (f_{SW} = f_{SYNC}/2). REG1's conversion cycles initiate on the rising edge of the internal clock signal. The CKO output frequency and phase match REG1's switching frequency (f_{CKO} = f_{DH1}) and the CKO signal is in phase. Note that the MAX1858A/MAX1875A/MAX1876A still require R_{OSC} when SYNC is externally clocked and the internal oscillator frequency should be set to 50% of the synchronization frequency (f_{SW} = 0.5 f_{SYNC}).

Thermal Overload Protection

Thermal overload protection limits total power dissipation in the MAX1858A/MAX1875A/MAX1876A. When the device's die-junction temperature exceeds T_J = +160°C, an on-chip thermal sensor shuts down the device, forcing DL_ and DH_ low, allowing the IC to cool. The thermal sensor turns the part on again after the junction temperature cools by 10°C. During thermal shutdown, the regulators shut down, $\overline{RST}$ goes low, and soft-start is reset. If the V_L linear-regulator output is short circuited, thermal-overload protection is triggered.

Design Procedure

Effective Input Voltage Range

Although the MAX1858A/MAX1875A/MAX1876A controllers can operate from input supplies ranging from 4.5V to 23V, the input voltage range can be effectively limited by the MAX1858A/MAX1875A/MAX1876As' duty-cycle limitations. The maximum input voltage is limited by the minimum on-time ($t_{ON(MIN)}$):

$$V_{IN(MAX)} \le \frac{V_{OUT}}{t_{ON(MIN)} f_{SW}}$$

where $t_{ON(MIN)}$ is 100ns. The minimum input voltage is limited by the switching frequency and minimum off-time, which determine the maximum duty cycle (D_{MAX} = 1 - $f_{SW} t_{OFF(MIN)}$):

$$V_{IN(MIN)} = \left[\frac{V_{OUT} + V_{DROP1}}{1 - f_{SW} t_{OFF(MIN)}}\right] + V_{DROP2} - V_{DROP1}$$

where V_{DROP1} is the sum of the parasitic voltage drops in the inductor discharge path, including synchronous rectifier, inductor, and PC board resistances. V_{DROP2} is the sum of the resistances in the charging path, including high-side switch, inductor, and PC board resistances.

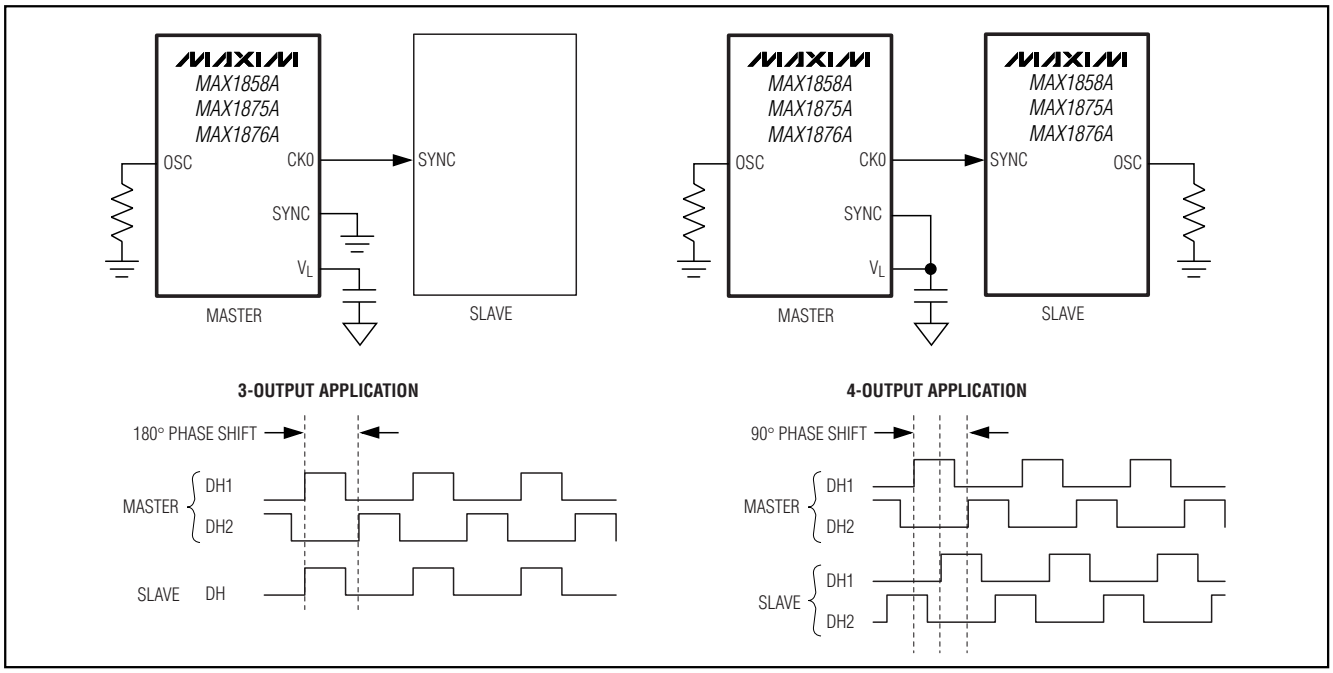


Figure 7. Synchronized Controllers

Dual 180° Out-of-Phase Buck Controllers with Sequencing/Prebias Startup and POR

Setting the Output Voltage

For 1V or greater output voltages, set the MAX1858A/MAX1875A/MAX1876A output voltage by connecting a voltage-divider from the output to FB_ to GND (Figure 8). Select R_B (FB_ to GND resistor) to between 1kΩ and 10kΩ. Calculate R_A (OUT_ to FB_ resistor) with the following equation:

$$R\_A = R\_B\left[\left(\frac{V_{OUT}}{V_{SET}}\right)-1\right]$$

where V_{SET} = 1V (see the *Electrical Characteristics*) and V_{OUT} can range from V_{SET} to 18V.

For output voltages below 1V, set the MAX1858A/MAX1875A/MAX1876A output voltage by connecting a voltage-divider from the output to FB_ to REF (Figure 8). Select R_C (FB to REF resistor) in the 1kΩ to 10kΩ range. Calculate R_A with the following equation:

$$R\_A = R\_C\left(\frac{V_{SET}-V_{OUT}}{V_{REF}-V_{SET}}\right)$$

where V_{SET} = 1V, V_{REF} = 2V (see the *Electrical Characteristics*), and V_{OUT} can range from 0 to V_{SET}.

Setting the Switching Frequency

The controller generates the clock signal by dividing down the internal oscillator or SYNC input signal when driven by an external oscillator, so the switching frequency equals half the oscillator frequency ($f_{SW} = f_{OSC}/2$). The internal oscillator frequency is set by a resistor (R_{OSC}) connected from OSC to GND. The relationship between f_{SW} and R_{OSC} is:

$$R_{OSC} = \frac{6\times10^{9}(\Omega\text{-Hz})}{f_{SW}}$$

where f_{SW} is in Hz and R_{OSC} is in Ω. For example, a 600kHz switching frequency is set with R_{OSC} = 10kΩ. Higher frequencies allow designs with lower inductor values and less output capacitance. Consequently, peak currents and I^2R losses are lower at higher switching frequencies, but core losses, gate-charge currents, and switching losses increase.

A rising clock edge on SYNC is interpreted as a synchronization input. If the SYNC signal is lost, the internal oscillator takes control of the switching rate, returning the switching frequency to that set by R_{OSC}. This maintains output regulation even with intermittent SYNC signals. When an external synchronization signal is used, R_{OSC} should set the switching frequency to one-half SYNC rate (f_{SYNC}).

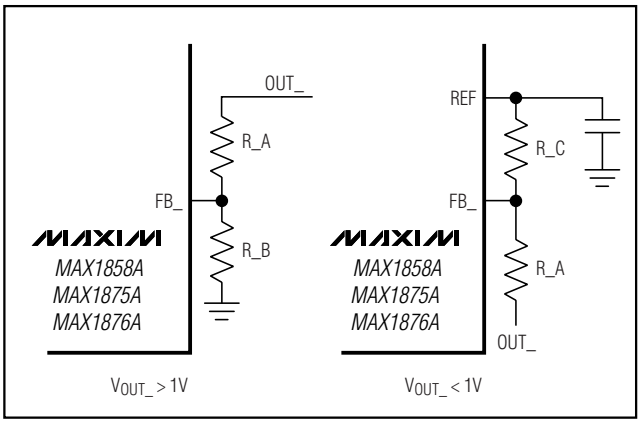


Figure 8. Adjustable Output Voltage

Inductor Selection

Three key inductor parameters must be specified for operation with the MAX1858A/MAX1875A/MAX1876A: inductance value (L), peak-inductor current (I_{PEAK}), and DC resistance (R_{DC}). The following equation assumes a constant ratio of inductor peak-to-peak AC current to DC average current (LIR). For LIR values too high, the RMS currents are high, and therefore I^2R losses are high. Large inductances must be used to achieve very low LIR values. Typically, inductance is proportional to resistance (for a given package type), which again makes I^2R losses high for very low LIR values. A good compromise between size and loss is a 30% peak-to-peak ripple current to average-current ratio (LIR = 0.3). The switching frequency, input voltage, output voltage, and selected LIR determine the inductor value as follows:

$$L = \frac{V_{OUT}(V_{IN}-V_{OUT})}{V_{IN}f_{SW}I_{OUT}LIR}$$

where V_{IN}, V_{OUT}, and I_{OUT} are typical values (so that efficiency is optimum for typical conditions). The switching frequency is set by R_{OSC} (see the *Setting the Switching Frequency* section). The exact inductor value is not critical and can be adjusted in order to make trade-offs among size, cost, and efficiency. Lower inductor values minimize size and cost, but also improve transient response and reduce efficiency due to higher peak currents. On the other hand, higher inductance increases efficiency by reducing the RMS current. However, resistive losses due to extra wire turns can exceed the benefit gained from lower AC current levels, especially when the inductance is increased without also allowing larger inductor dimensions.

Find a low-loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. The

Dual 180° Out-of-Phase Buck Controllers with Sequencing/Prebias Startup and POR

inductor's saturation rating must exceed the peak-inductor current at the maximum defined load current ($I_{LOAD(MAX)}$):

$$I_{PEAK} = I_{LOAD(MAX)} + \left(\frac{LIR}{2}\right) I_{LOAD(MAX)}$$

Setting the Valley Current Limit

The minimum current-limit threshold must be high enough to support the maximum expected load current with the worst-case low-side MOSFET on-resistance value since the low-side MOSFET's on-resistance is used as the current-sense element. The inductor's valley current occurs at $I_{LOAD(MAX)}$ minus half of the ripple current. The current-sense threshold voltage (V_{ITH}) should be greater than voltage on the low-side MOSFET during the ripple-current valley:

$$V_{ITH} > R_{DS(ON,MAX)} \times I_{LOAD(MAX)} \times \left(1 - \frac{LIR}{2}\right)$$

where $R_{DS(ON)}$ is the on-resistance of the low-side MOSFET (N_L). Use the maximum value for $R_{DS(ON)}$ from the low-side MOSFET's data sheet, and additional margin to account for $R_{DS(ON)}$ rise with temperature is also recommended. A good general rule is to allow 0.5% additional resistance for each °C of the MOSFET junction temperature rise.

Connect ILIM_ to VL for the default 100mV (typ) current-limit threshold. For an adjustable threshold, connect a resistor ($R_{ILIM\_}$) from ILIM_ to GND. The relationship between the current-limit threshold ($V_{ITH\_}$) and $R_{ILIM\_}$ is:

$$R_{ILIM\_} = \frac{V_{ITH\_}}{0.5\mu A}$$

where $R_{ILIM\_}$ is in Ω and $V_{ITH\_}$ is in V.

An R_{ILIM} resistance range of 100kΩ to 600kΩ corresponds to a current-limit threshold of 50mV to 300mV. When adjusting the current limit, 1% tolerance resistors minimize error in the current-limit threshold.

For foldback current limit, a resistor (R_{FBI}) is added from ILIM pin to output. The value of R_{ILIM} and R_{FBI} can then be calculated as follows:

First select the percentage of foldback, P_{FB}, from 15% to 30%, then:

$$R_{FBI} = \frac{P_{FB} \times V_{OUT}}{5 \times 10^{-6}(1 - P_{FB})}$$

and

$$R_{ILIM} = \frac{10 \times V_{ITH}(1 - P_{FB}) \times R_{FBI}}{\left[V_{OUT} - 10 \times V_{ITH}(1 - P_{FB})\right]}$$

If $R_{ILIM\_}$ results in a negative number, select a low-side MOSFET with lower $R_{DS(ON)}$ or increase $P_{FB\_}$ or a combination of both for the best compromise of cost, efficiency, and lower power dissipation during short circuit.

Input Capacitor

The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the circuit's switching. The input capacitor must meet the ripple current requirement (I_{RMS}) imposed by the switching currents as defined by the following equation:

$$I_{RMS} = I_{LOAD} \frac{\sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}}$$

I_{RMS} has a maximum value when the input voltage equals twice the output voltage ($V_{IN} = 2V_{OUT}$), so $I_{RMS(MAX)} = I_{LOAD} / 2$. For most applications, nontantalum capacitors (ceramic, aluminum, polymer, or OS-CON) are preferred at the input due to their robustness with high inrush currents typical of systems that can be powered from very low impedance sources. Additionally, two (or more) smaller-value low-ESR capacitors can be connected in parallel for lower cost. Choose an input capacitor that exhibits less than +10°C temperature rise at the RMS input current for optimal long-term reliability.

Output Capacitor

The key selection parameters for the output capacitor are capacitance value, ESR, and voltage rating. These parameters affect the overall stability, output ripple voltage, and transient response. The output ripple has two components: variations in the charge stored in the output capacitor, and the voltage drop across the capacitor's ESR caused by the current flowing into and out of the capacitor:

$$V_{RIPPLE} \cong V_{RIPPLE(ESR)} + V_{RIPPLE(C)}$$

The output voltage ripple as a consequence of the ESR and output capacitance is:

$$V_{RIPPLE(ESR)} = I_{P-P}R_{ESR}$$

$$V_{RIPPLE(C)} = \frac{I_{P-P}}{8C_{OUT}f_{SW}}$$

$$I_{P-P} = \left(\frac{V_{IN} - V_{OUT}}{f_{SW}L}\right)\left(\frac{V_{OUT}}{V_{IN}}\right)$$

where I_{P-P} is the peak-to-peak inductor current (see the *Inductor Selection* section). These equations are suitable for initial capacitor selection, but final values should be verified by testing in a prototype or evaluation circuit.

As a general rule, a smaller inductor ripple current results in less output ripple voltage. Since inductor ripple current depends on the inductor value and input voltage, the output ripple voltage decreases with larger inductance and increases with higher input voltages. However, the inductor ripple current also impacts transient-response performance, especially at low V_{IN} - V_{OUT} differentials. Low inductor values allow the inductor current to slew faster, replenishing charge removed from the output filter capacitors by a sudden load step. The amount of output-voltage sag is also a function of the maximum duty factor, which can be calculated from the minimum off-time and switching frequency:

$$V_{SAG} = \frac{L(I_{LOAD1} - I_{LOAD2})^2\left[\left(\frac{V_{OUT}}{V_{IN}f_{SW}}\right) + t_{OFF(MIN)}\right]}{2C_{OUT}V_{OUT}\left[\left(\frac{V_{IN} - V_{OUT}}{V_{IN}f_{SW}}\right) - t_{OFF(MIN)}\right]}$$

where $t_{OFF(MIN)}$ is the minimum off-time (see the *Electrical Characteristics*), and f_{SW} is set by R_{OSC} (see the *Setting the Switching Frequency* section).

Compensation

Each voltage-mode controller section employs a transconductance error amplifier whose output is the compensation point of the control loop. The control loop is shown in Figure 9. For frequencies much lower than Nyquist, the PWM block can be simplified to a voltage amplifier. Connect $R_{COMP\_}$ and C_{COMP_A} from COMP to GND to compensate the loop (Figure 9). The inductor, output capacitor, compensation resistor, and compensation capacitors determine the loop stability. Since the inductor and output capacitor are chosen based on performance, size, and cost, select the compensation resistor and capacitors to optimize control-loop stability.

To determine the loop gain (A_L), consider the gain from FB to COMP ($A_{COMP/FB}$), from COMP to LX ($A_{LX/COMP}$), and from LX to FB ($A_{FB/LX}$). The total loop gain is:

$$A_L = A_{COMP/FB} \times A_{LX/COMP} \times A_{FB/LX}$$

where:

$$A_{COMP/FB} = \frac{V_{COMP}}{V_{FB}} \cong \frac{g_{M\_COMP}}{sC_{COMP}} \times \frac{1 + sR_{COMP}C_{COMP\_A}}{1 + sR_{COMP}C_{COMP\_B}}$$

assuming an ideal integrator, and assuming that C_{COMP_B} is much less than C_{COMP_A}:

$$A_{LX/COMP} = \frac{V_{LX}}{V_{COMP}} = \frac{V_{IN}}{V_{RAMP}}$$

where $V_{RAMP} = 1V_{P-P}$:

$$A_{FB/LX} = \frac{V_{FB}}{V_{LX}} = \frac{V_{SET}}{V_{OUT}} \frac{1 + sR_{ESR}C_{OUT}}{S^2LC_{OUT} + SR_{ESR}C_{OUT} + 1}$$

$$\cong \frac{V_{SET}}{V_{OUT}} \frac{1 + SR_{ESR}C_{OUT}}{V_{OUT}S^2LC_{OUT} + 1}$$

Therefore:

$$A_L \cong \frac{g_{M\_COMP}}{SC_{COMP\_A}} \times \frac{1 + SR_{COMP}C_{COMP\_A}}{1 + SR_{COMP}C_{COMP\_B}} \times \frac{V_{IN}}{V_{RAMP}} \times \frac{V_{SET}}{V_{OUT}} \times \frac{1 + SR_{ESR}C_{OUT}}{S^2LC_{OUT} + 1}$$

For an ideal integrator, this loop gain approaches infinity at DC. In reality the g_M amplifier has a finite output impedance, which imposes a finite, but large, loop gain. It is this large loop gain that provides DC load accuracy. The dominant pole occurs due to the integrator, and for this analysis, it can be approximated to occur at DC. R_{COMP} creates a zero at:

$$f_{Z\_COMP\_A} = \frac{1}{2\pi \times R_{COMP\_}C_{COMP\_A}}$$

The inductor and capacitor form a double pole at:

$$f_{LC} = \frac{1}{2\pi \times \sqrt{LC_{OUT}}}$$

Dual 180° Out-of-Phase Buck Controllers with Sequencing/Prebias Startup and POR

At some higher frequency, the output capacitor's impedance becomes insignificant compared to its ESR, and the LC system becomes more like an LR system, turning a double pole into a single pole. This zero occurs at:

$$f_{ESR} = \frac{1}{2\pi \times R_{ESR} C_{OUT}}$$

A final pole is added using C_{COMP_B} to reduce the gain and attenuate noise after crossover. This pole (f_{COMP_B}) occurs at:

$$f_{COMP\_B} = \frac{1}{2\pi \times R_{COMP} C_{COMP\_B}}$$

Figure 10 shows a Bode plot of the poles and zeros in their relative locations.

Near crossover, the following approximations can be made to simplify the loop-gain equation:

- R_{COMP} has much higher impedance than C_{COMP}. This is true if, and only if, crossover occurs above $f_{Z\_COMP\_A}$. If this is true, C_{COMP_A} can be ignored (as a short to ground).
- R_{ESR} is much higher impedance than C_{OUT}. This is true if, and only if, crossover occurs well after the output capacitor's ESR zero. If this is true, C_{OUT} becomes an insignificant part of the loop gain and can be ignored (as a short to ground).
- C_{COMP_B} is much higher impedance than R_{COMP} and can be ignored (as an open circuit). This is true if, and only if, crossover occurs far below f_{COMP_B}.

The following loop-gain equation can be found by using these previous approximations with Figure 9:

$$A_L \cong \frac{V_{IN}}{V_{RAMP}} \times \frac{V_{SET}}{V_{OUT}} \times \frac{g_{M\_COMP} \times R_{COMP} \times R_{ESR}}{sL}$$

Setting the loop gain to 1 and solving for the crossover frequency yields:

$$f_{CO} = GBW = \frac{V_{IN}}{V_{RAMP}} \times \frac{V_{SET}}{V_{OUT}} \times \frac{g_{M\_COMP} \times R_{COMP} \times R_{ESR}}{2\pi \times L}$$

To ensure stability, select R_{COMP} to meet the following criteria:

- Unity-gain crossover must occur below 1/5th of the switching frequency.
- For reasonable phase margin using type 1 compensation, f_{CO} must be larger than $5 \times f_{ESR}$.

Choose C_{COMP_A} so that $f_{Z\_COMP\_A}$ equals half f_{LC} using the following equation:

$$C_{COMP\_A} = \frac{2 \times \sqrt{LC_{OUT}}}{R_{COMP}}$$

Choose C_{COMP_B} so that f_{COMP_B} occurs at 3 times f_{CO} using the following equation:

$$C_{COMP\_B} = \frac{1}{2\pi \times \left(3 \times f_{CO}\right) \times R_{COMP}}$$

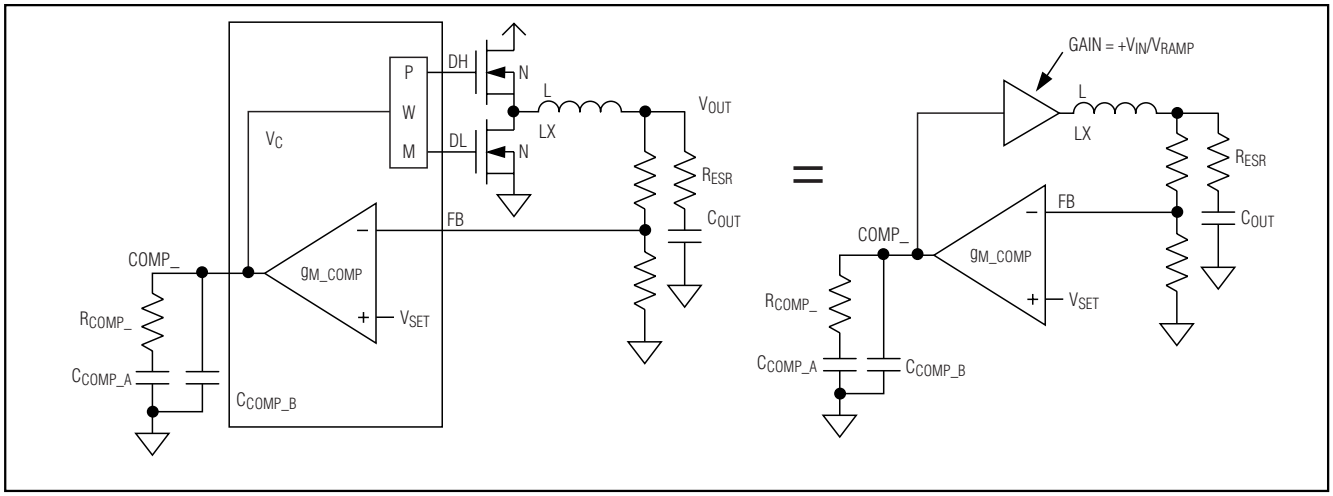


Figure 9. Fixed-Frequency Voltage-Mode Control Loop

MOSFET Selection

The MAX1858A/MAX1875A/MAX1876As' step-down controller drives two external logic-level N-channel MOSFETs as the circuit switch elements. The key selection parameters are:

- On-resistance ($R_{DS(ON)}$)
- Maximum drain-to-source voltage ($V_{DS(MAX)}$)
- Minimum threshold voltage ($V_{TH(MIN)}$)
- Total gate charge (Q_g)
- Reverse transfer capacitance (C_{RSS})
- Power dissipation

All four N-channel MOSFETs must be a logic-level type with guaranteed on-resistance specifications at $V_{GS} \geq 4.5V$. For maximum efficiency, choose a high-side MOSFET ($N_{H\_}$) that has conduction losses equal to the switching losses at the optimum input voltage. Check to ensure that the conduction losses at minimum input voltage do not exceed MOSFET package thermal limits, or violate the overall thermal budget. Also, check to ensure that the conduction losses plus switching losses at the maximum input voltage do not exceed package ratings or violate the overall thermal budget.

Ensure that the MAX1858A/MAX1875A/MAX1876A DL_ gate drivers can drive $N_{L\_}$. In particular, check that the dv/dt caused by $N_{H\_}$ turning on does not pull up the $N_{L\_}$ gate through $N_{L\_}$'s drain-to-gate capacitance. This is the most frequent cause of cross-conduction problems.

Gate-charge losses are dissipated by the driver and do not heat the MOSFET. All MOSFETs must be selected so that their total gate charge is low enough that V_L can power all four drivers without overheating the IC:

$$P_{VL} = V_{IN} \times Q_{G\_TOTAL} \times f_{SW}$$

MOSFET package power dissipation often becomes a dominant design factor. I^2R power losses are the greatest heat contributor for both high-side and low-side MOSFETs. I^2R losses are distributed between $N_{H\_}$ and $N_{L\_}$ according to duty factor as shown in the equations below. Switching losses affect only the high-side MOSFET, since the low-side MOSFET is a zero-voltage switched device when used in the buck topology.

Calculate MOSFET temperature rise according to package thermal-resistance specifications to ensure that both MOSFETs are within their maximum junction temperature at high ambient temperature. The worst-case dissipation for the high-side MOSFET (P_{NH}) occurs at both extremes of input voltage, and the worst-case dissipation for the low-side MOSFET (P_{NL}) occurs at maximum input voltage.

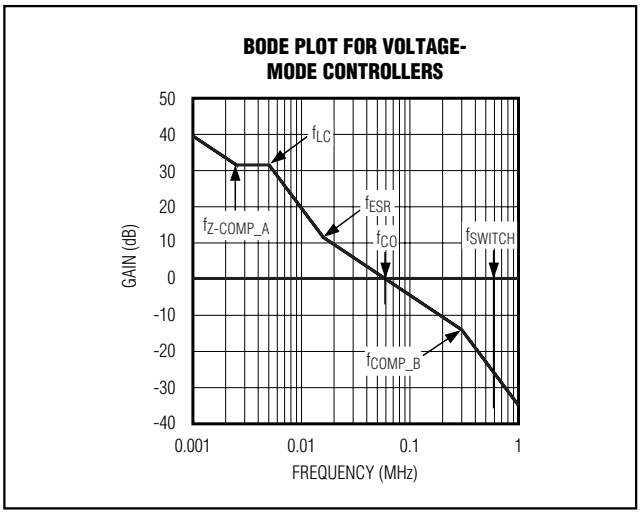


Figure 10. Voltage-Mode Loop Analysis

$$P_{NH(SWITCHING)} = V_{IN} I_{LOAD} f_{SW} \left(\frac{Q_{GS} + Q_{GD}}{I_{GATE}} \right)$$

I_{GATE} is the average DH driver-output current capability determined by:

$$I_{GATE} = \frac{V_L}{2\left(R_{DS(ON)DH} + R_{GATE} + R_{GMOSFET}\right)}$$

where $R_{DS(ON)DH}$ is the high-side MOSFET driver's on-resistance (5Ω max), R_{GATE} is any series resistance between DH and BST (Figure 5), and $R_{GMOSFET}$ is the internal gate resistance of the external MOSFET:

$$P_{NH(CONDUCTION)} = I_{LOAD}{}^2 R_{DS(ON)NH} \left(\frac{V_{OUT}}{V_{IN}} \right)$$

$$P_{NH(TOTAL)} = P_{NH(SWITCHING)} + P_{NH(CONDUCTION)}$$

$$P_{NL} = I_{LOAD}{}^2 R_{DS(ON)NL} \left(1 - \left(\frac{V_{OUT}}{V_{IN}} \right) \right)$$

where $P_{NH(CONDUCTION)}$ is the conduction power loss in the high-side MOSFET, and P_{NL} is the total low-side power loss.

To reduce EMI caused by switching noise, add a 0.1µF ceramic capacitor from the high-side switch drain to the low-side switch source or add resistors in series with DL_ and DH_ to increase the MOSFETs' turn-on and turn-off times.

Dual 180° Out-of-Phase Buck Controllers with Sequencing/Prebias Startup and POR

Applications Information

Dropout Performance

When working with low input voltages, the output-voltage adjustable range for continuous-conduction operation is restricted by the minimum off-time ($t_{OFF(MIN)}$). For best dropout performance, use the lowest (100kHz) switching-frequency setting. Manufacturing tolerances and internal propagation delays introduce an error to the switching frequency and minimum off-time specifications. This error is more significant at higher frequencies. Also, keep in mind that transient response performance of buck regulators operated close to dropout is poor, and bulk output capacitance must often be added (see the V_{SAG} equation in the *Design Procedure* section).

The absolute point of dropout is when the inductor current ramps down during the minimum off-time (ΔI_{DOWN}) as much as it ramps up during the maximum on-time (ΔI_{UP}). The ratio $h = \Delta I_{UP}/\Delta I_{DOWN}$ is an indicator of the ability to slew the inductor current higher in response to increased load, and must always be greater than 1. As h approaches 1, the absolute minimum dropout point, the inductor current cannot increase as much during each switching cycle and V_{SAG} greatly increases unless additional output capacitance is used.

A reasonable minimum value for h is 1.5, but adjusting this up or down allows tradeoffs between V_{SAG}, output capacitance, and minimum operating voltage. For a given value of h, the minimum operating voltage can be calculated as:

$$V_{IN(MIN)} = \left[\frac{V_{OUT} + V_{DROP1}}{1 - hf_{SW}t_{OFF(MIN)}}\right] + V_{DROP2} - V_{DROP1}$$

where V_{DROP1} is the sum of the parasitic voltage drops in the inductor discharge path, including synchronous rectifier, inductor, and PC board resistances; V_{DROP2} is the sum of the resistances in the charging path, including high-side switch, inductor, and PC board resistances; and $t_{OFF(MIN)}$ is from the *Electrical Characteristics*. The absolute minimum input voltage is calculated with h = 1.

If the calculated $V+_{(MIN)}$ is greater than the required minimum input voltage, then reduce the operating frequency or add output capacitance to obtain an acceptable V_{SAG}. If operation near dropout is anticipated, calculate V_{SAG} to be sure of adequate transient response.

Dropout design example:

V_{OUT} = 5V

f_{SW} = 600kHz

$t_{OFF(MIN)}$ = 250ns

$V_{DROP1} = V_{DROP2}$ = 100mV

h = 1.5

$$V_{IN(MIN)} = \left[\frac{5V + 100mV}{1 - 1.5(600kHz)(250ns)}\right] + 100mV - 100mV = 6.58V$$

Calculating again with h = 1 gives the absolute limit of dropout:

$$V_{IN(MIN)} = \left[\frac{5V + 100mV}{1 - (600kHz)(250ns)}\right] + 100mV - 100mV = 6V$$

Therefore, V_{IN} must be greater than 6V, even with very large output capacitance, and a practical input voltage with reasonable output capacitance would be 6.58V.

Improving Noise Immunity

Applications where the MAX1858A/MAX1875A/MAX1876A must operate in noisy environments can typically adjust their controller's compensation to improve the system's noise immunity. In particular, high-frequency noise coupled into the feedback loop causes jittery duty cycles. One solution is to lower the crossover frequency (see the *Compensation* section).

PC Board Layout Guidelines

Careful PC board layout is critical to achieve low switching losses and clean, stable operation. This is especially true for dual converters where one channel can affect the other. Refer to the MAX1858 EV kit or MAX1875 EV kit data sheet for specific layout examples.

If possible, mount all the power components on the top side of the board with their ground terminals flush against one another. Follow these guidelines for good PC board layout:

- Isolate the power components on the top side from the analog components on the bottom side with a ground shield. Use a separate PGND plane under the OUT1 and OUT2 sides (referred to as PGND1 and PGND2). Avoid the introduction of AC currents into the PGND1 and PGND2 ground planes. Run the power plane ground currents on the top side only.

- Use a star-ground connection on the power plane to minimize the crosstalk between OUT1 and OUT2.
- Keep the high-current paths short, especially at the ground terminals. This practice is essential for stable, jitter-free operation.
- Connect GND and PGND together close to the IC. Do not connect them together anywhere else. Carefully follow the grounding instructions under step 4 of the *Layout Procedure* section.
- Keep the power traces and load connections short. This practice is essential for high efficiency. Use thick copper PC boards (2oz vs. 1oz) to enhance full-load efficiency by 1% or more.
- LX_ and PGND connections to the synchronous rectifiers for current limiting must be made using Kelvin-sense connections to guarantee the current-limit accuracy. With 8-pin SO MOSFETs, this is best done by routing power to the MOSFETs from outside using the top copper layer, while connecting PGND and LX_ underneath the 8-pin SO package.
- When trade-offs in trace lengths must be made, allow the inductor-charging path to be made longer than the discharge path. Since the average input current is lower than the average output current in step-down converters, this minimizes the power dissipation and voltage drops caused by board resistance. For example, allow some extra distance between the input capacitors and the high-side MOSFET rather than to allow distance between the inductor and the low-side MOSFET or between the inductor and the output filter capacitor.
- Ensure that the feedback connection to $C_{OUT\_}$ is short and direct.
- Route high-speed switching nodes (BST_, LX_, DH_, and DL_) away from the sensitive analog areas (REF, COMP_, ILIM_, and FB_). Use PGND1 and PGND2 as EMI shields to keep radiated noise away from the IC, feedback dividers, and analog bypass capacitors.
- Make all pin-strap control input connections (ILIM_, SYNC, and EN) to analog ground (GND) rather than power ground (PGND).

Layout Procedure

1) Place the power components first, with ground terminals adjacent ($N_{L\_}$ source, $C_{IN\_}$, and $C_{OUT\_}$). Make all these connections on the top layer with wide, copper-filled areas (2oz copper recommended).
2) Mount the controller IC adjacent to the synchronous-rectifier MOSFETs ($N_{L\_}$), preferably on the back side in order to keep LX_, PGND_, and DL_ traces short and wide. The DL_ gate trace must be short and wide, measuring 50mils to 100mils wide if the low-side MOSFET is 1in from the controller IC.
3) Group the gate-drive components (BST_ diodes and capacitors, and V_L bypass capacitor) together near the controller IC.
4) Make the DC-DC controller ground connections as follows: create a small analog ground plane near the IC. Connect this plane to GND and use this plane for the ground connection for the reference (REF) V+ bypass capacitor, compensation components, feedback dividers, OSC resistor, and ILIM_ resistors (if any). Connect GND and PGND together under the IC (this is the only connection between GND and PGND).
5) On the board's top side (power planes), make a star ground to minimize crosstalk between the two sides.

Chip Information

TRANSISTOR COUNT: 6688

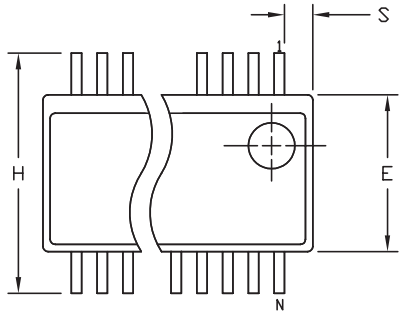
PROCESS: BiCMOS

Dual 180° Out-of-Phase Buck Controllers with Sequencing/Prebias Startup and POR

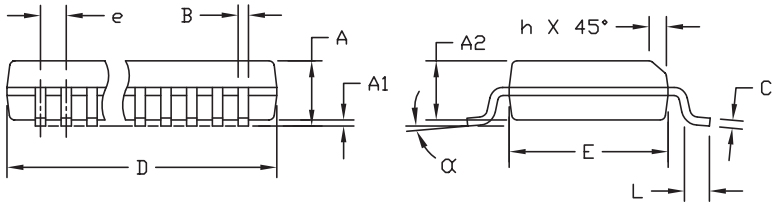
Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

QSOP EPS



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.061	.068	1.55	1.73
A1	.004	.0098	0.102	0.249
A2	.055	.061	1.40	1.55
B	.008	.012	0.20	0.30
C	.0075	.0098	0.191	0.249
D	SEE VARIATIONS			
E	.150	.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
N	SEE VARIATIONS			
α	0°	8°	0°	8°



VARIATIONS:

	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	N	
D	.189	.196	4.80	4.98	16	AB
S	.0020	.0070	0.05	0.18		
D	.337	.344	8.56	8.74	20	AD
S	.0500	.0550	1.270	1.397		
D	.337	.344	8.56	8.74	24	AE
S	.0250	.0300	0.635	0.762		
D	.386	.393	9.80	9.98	28	AF
S	.0250	.0300	0.635	0.762		

NOTES:
1). D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2). MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006" PER SIDE.
3). CONTROLLING DIMENSIONS: INCHES.
4). MEETS JEDEC MO137.

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION

TITLE:
PACKAGE OUTLINE, QSOP .150", .025" LEAD PITCH

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0055	E	1/1