TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74HC595AP, TC74HC595AF, TC74HC595AFN

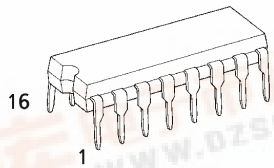
8 – BIT SHIFT REGISTER / LATCH (3 – STATE)

The TC74HC595A is a high speed 8−BIT SHIFT REGISTER / LATCH fabricated with silicon gate C²MOS technology.
It achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
The TC74HC595A contains an 8−bit static shift register which feeds an 8−bit storage register.
Shift operation is accomplished on the positive going transition of the SCK input. The output register is loaded with the contents of the shift register on the positive going transition of the RCK input. Since RCK and SCK signal are independent, parallel outputs can be held stable during the shift operation. And, since the parallel outputs are 3−state, it can be directly connected to 8−bit bus. This register can be used in serial−to−parallel conversion, data receivers, etc.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

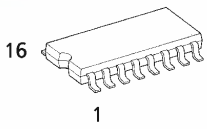
FEATURES :

- High Speed ····· f_{MAX} = 55MHz(typ.) at V_{CC} = 5V
- Low Power Dissipation ····· I_{CC} = 4μA(Max.) at Ta = 25°C
- High Noise Immunity ····· $V_{NIH} = V_{NIL}$ = 28% V_{CC} (Min.)
- Output Drive Capability ····· 15 LSTTL Loads For QA ~ QH
  10 LSTTL Loads For QH'
- Symmetrical Output Impedance ··· $|I_{OH}| = I_{OL}$ = 6mA(Min.) For QA ~ QH
  $|I_{OH}| = I_{OL}$ = 4mA(Min.) For QH'
- Balanced Propagation Delays ····· $t_{pLH} \simeq t_{pHL}$
- Wide Operating Voltage Range ···· V_{CC} (opr.) = 2V ~ 6V
- Pin and Function Compatible with 74LS595

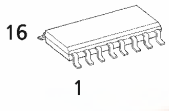
(Note) The JEDEC SOP (FN) is not available in Japan.



P (DIP16-P-300-2.54A)
Weight : 1.00g (Typ.)

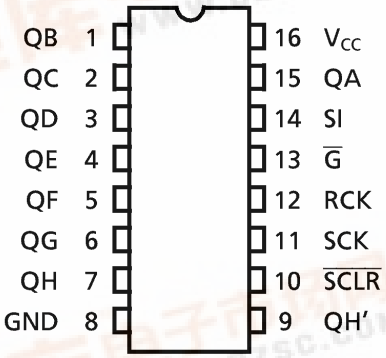


F (SOP16-P-300-1.27)
Weight : 0.18g (Typ.)



FN (SOL16-P-150-1.27)
Weight : 0.13g (Typ.)

PIN ASSIGNMENT



(TOP VIEW)

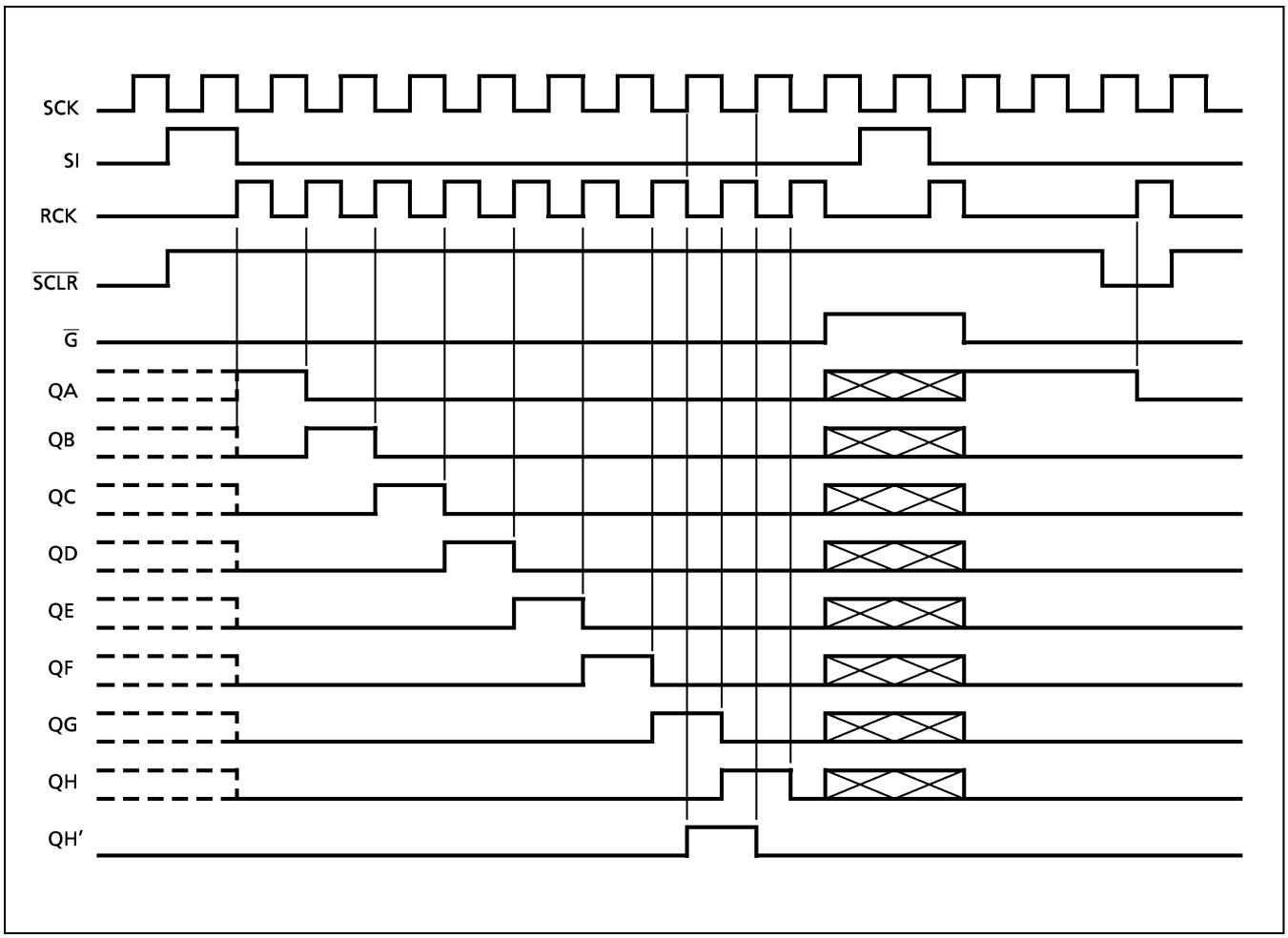
TRUTH TABLE

INPUTS					FUNCTION
SI	SCK	$\overline{SCLR}$	RCK	$\overline{G}$	
X	X	X	X	H	QA thru QH outputs disable
X	X	X	X	L	QA thru QH outputs enable
X	X	L	X	X	Shift register is cleared.
L	↑	H	X	X	First stage of S. R. becomes "L". Other stages store the data of previous stage, respectively.
H	↑	H	X	X	First stage of S. R. becomes "H". Other stages store the data of previous stage, respectively.
X	↓	H	X	X	State of S. R. is not changed.
X	X	X	↑	X	S.R. data is stored into storage register.
X	X	X	↓	X	Storage register stage is not changed.

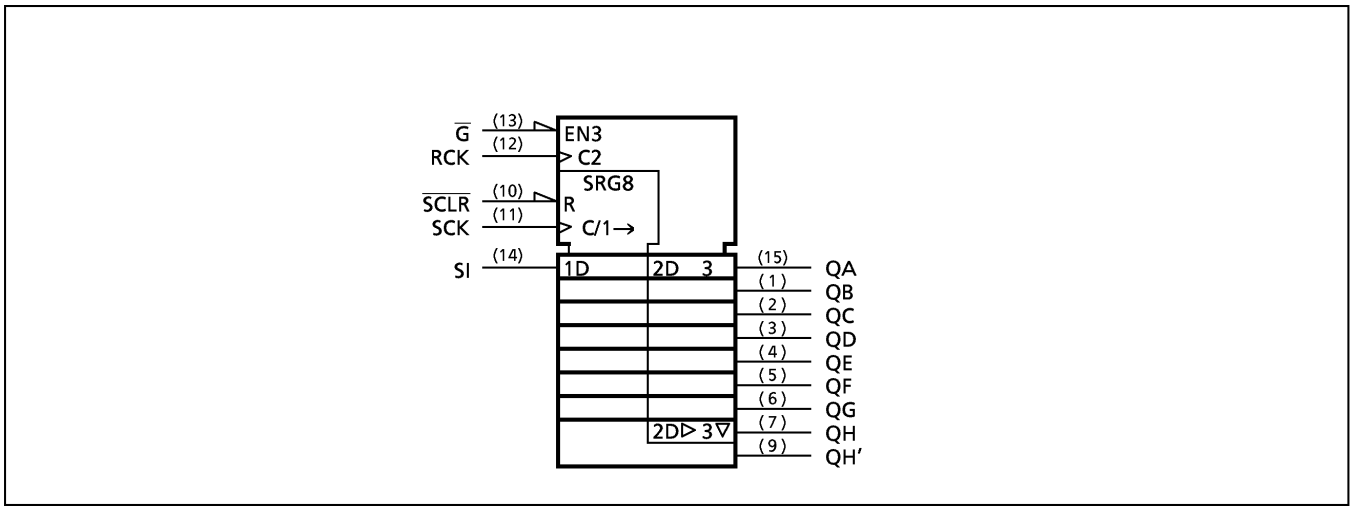
X : Don't Care

961001EBA2

TIMING CHART

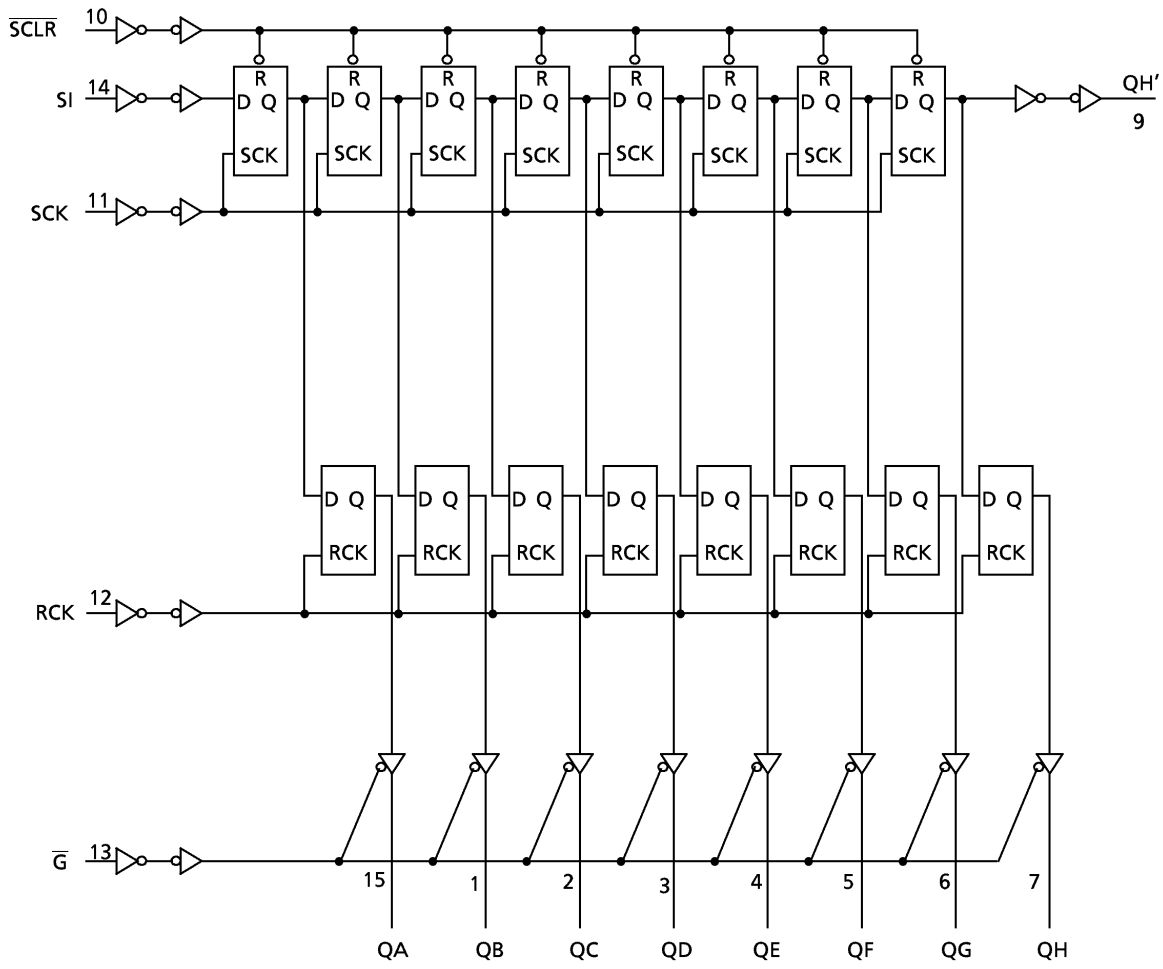


IEC LOGIC SYMBOL



961001EBA2'

SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5~7	V
DC Input Voltage	V_{IN}	−0.5~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current (QH') (QA~QH)	I_{OUT}	±25 ±35	mA
DC V_{CC}/Ground Current	I_{CC}	±75	mA
Power Dissipation	P_D	500 (DIP)* / 180 (SOP)	mW
Storage Temperature	T_{stg}	−65~150	°C

*500mW in the range of Ta= −40°C~65°C. From Ta=65°C to 85 °C a derating factor of −10mW/ °C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2~6	V
Input Voltage	V_{IN}	0~V_{CC}	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	T_{opr}	−40~85	°C
Input Rise and Fall Time	t_r, t_f	0~1000 (V_{CC}=2.0V) 0~ 500 (V_{CC}=4.5V) 0~ 400 (V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC} (V)	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=−40~85°C MIN.	Ta=−40~85°C MAX.	UNIT
High - Level Input Voltage	V_{IH}			2.0 4.5 6.0	1.50 3.15 4.20	— — —	— — —	1.50 3.15 4.20	— — —	V
Low - Level Input Voltage	V_{IL}			2.0 4.5 6.0	— — —	— — —	0.50 1.35 1.80	— — —	0.50 1.35 1.80	V
High - Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=−20μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	— — —	1.9 4.4 5.9	— — —	V
		QH'	I_{OH}=−4 mA I_{OH}=−5.2mA	4.5 6.0	4.18 5.68	4.31 5.80	— —	4.13 5.63	— —	
		QA~QH	I_{OH}=−6 mA I_{OH}=−7.8mA	4.5 6.0	4.18 5.68	4.31 5.80	— —	4.13 5.63	— —	
Low - Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0 4.5 6.0	— — —	0.0 0.0 0.0	0.1 0.1 0.1	— — —	0.1 0.1 0.1	V
		QH'	I_{OL}=4 mA I_{OL}=5.2mA	4.5 6.0	— —	0.17 0.18	0.26 0.26	— —	0.33 0.33	
		QA~QH	I_{OL}=6 mA I_{OL}=7.8mA	4.5 6.0	— —	0.17 0.18	0.26 0.26	— —	0.33 0.33	
3 - State Output Off - State Current	I_{OZ}	V_{IN}=V_{IH} or V_{IL} V_{OUT}=V_{CC} or GND		6.0	—	—	±0.5	—	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	—	—	±0.1	—	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	—	—	4.0	—	40.0	

TIMING REQUIREMENTS (Input $t_r = t_f = 6ns$)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C		Ta = −40~85°C	UNIT
			V_{CC} (V)	TYP.	LIMIT	LIMIT	
Minimum Pulse Width (SCK, RCK)	$t_{W(H)}$ $t_{W(L)}$		2.0 4.5 6.0	— — —	75 15 13	95 19 16	ns
Minimum Pulse Width ($\overline{SCLR}$)	$t_{W(L)}$		2.0 4.5 6.0	— — —	75 15 13	95 19 16	
Minimum Set−up Time (SI−SCK)	t_s		2.0 4.5 6.0	— — —	50 10 9	65 13 11	
Minimum Set−up Time (SCK−RCK)	t_s		2.0 4.5 6.0	— — —	75 15 13	95 19 16	
Minimum Set−up Time ($\overline{SCLR}$−RCK)	t_s		2.0 4.5 6.0	— — —	100 20 17	125 25 21	
Minimum Hold Time	t_h		2.0 4.5 6.0	— — —	0 0 0	0 0 0	
Minimum Removal Time ($\overline{SCLR}$)	t_{rem}		2.0 4.5 6.0	— — —	50 10 9	65 13 11	
Clock Frequency	f		2.0 4.5 6.0	— — —	6 30 35	5 25 28	MHz

AC ELECTRICAL CHARACTERISTICS (C_L = 15pF, V_{CC} = 5V, Ta = 25°C, Input $t_r = t_f$ = 6ns)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time (QH')	t_{TLH} t_{THL}		—	4	8	ns
Propagation Delay Time (SCK − QH')	t_{pLH} t_{pHL}		—	12	21	
Propagation Delay Time ($\overline{SCLR}$ − QH')	t_{pHL}		—	15	30	
Maximum Clock Frequency	f_{MAX}		35	77	—	MHz

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f$ = 6ns)

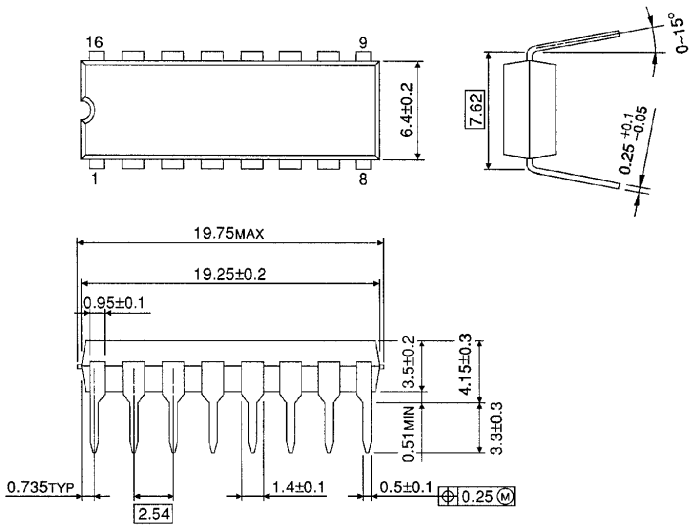
PARAMETER	SYMBOL	TEST CONDITION	CL (pF)	V_{CC} (V)	Ta = 25°C MIN.	Ta = 25°C TYP.	Ta = 25°C MAX.	Ta = −40~85°C MIN.	Ta = −40~85°C MAX.	UNIT
Output Transition Time (Q_n)	t_{TLH} t_{THL}		50	2.0	—	25	60	—	75	ns
				4.5	—	7	12	—	15	
				6.0	—	6	10	—	13	
Output Transition Time (QH')	t_{TLH} t_{THL}		50	2.0	—	30	75	—	95	
				4.5	—	8	15	—	19	
				6.0	—	7	13	—	16	
Propagation Delay Time (SCK − QH')	t_{pLH} t_{pHL}		50	2.0	—	45	125	—	155	
				4.5	—	15	25	—	31	
				6.0	—	13	21	—	26	
Propagation Delay Time ($\overline{SCLR}$ − QH')	t_{pHL}		50	2.0	—	60	175	—	220	
				4.5	—	18	35	—	44	
				6.0	—	15	30	—	37	
Propagation Delay Time (RCK − Q_n)	t_{pLH} t_{pHL}		50	2.0	—	60	150	—	190	
				4.5	—	20	30	—	38	
				6.0	—	17	26	—	32	
			150	2.0	—	75	190	—	240	
				4.5	—	25	38	—	48	
				6.0	—	22	32	—	41	
Output Enable time	t_{pZL} t_{pZH}	R_L = 1kΩ	50	2.0	—	45	135	—	170	
				4.5	—	15	27	—	34	
				6.0	—	13	23	—	29	
			150	2.0	—	60	175	—	220	
				4.5	—	20	35	—	44	
				6.0	—	17	30	—	37	
Output Disable time	t_{pLZ} t_{pHZ}	R_L = 1kΩ	50	2.0	—	30	150	—	190	
				4.5	—	15	30	—	38	
				6.0	—	14	26	—	33	
Maximum Clock Frequency	f_{MAX}		50	2.0	6	17	—	5	—	MHz
				4.5	30	50	—	25	—	
				6.0	35	59	—	28	—	
Input Capacitance	C_{IN}				—	5	10	—	10	pF
Power Dissipation Capacitance	C_{PD}(1)				—	184	—	—	—	

Note(1): C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

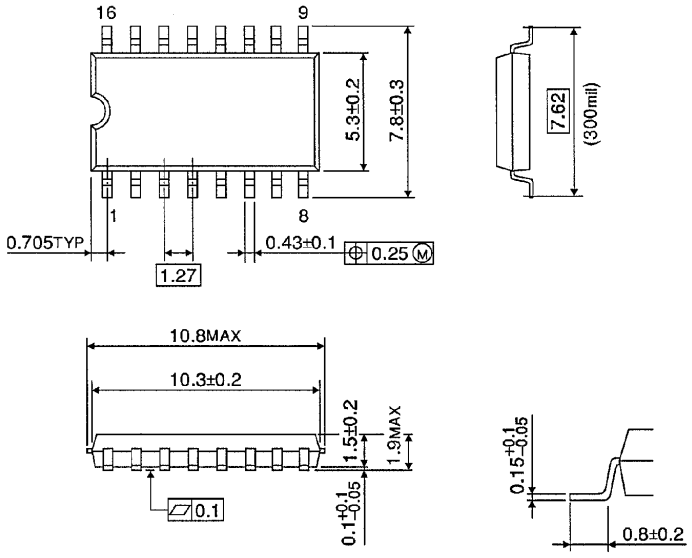
$$I_{CC}\,(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

DIP 16PIN OUTLINE DRAWING (DIP16-P-300-2.54A) Unit in mm



Weight : 1.00g (Typ.)

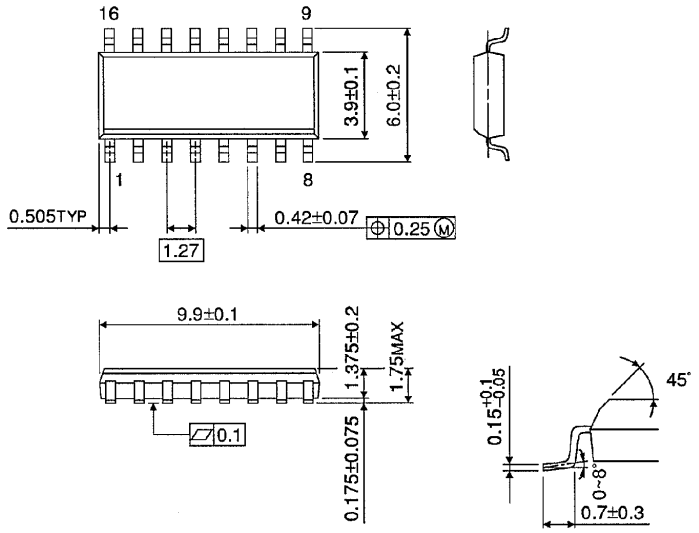
SOP 16PIN (200mil BODY) OUTLINE DRAWING (SOP16-P-300-1.27) Unit in mm



Weight : 0.18g (Typ.)

SOP 16PIN (150mil BODY) OUTLINE DRAWING (SOL16-P-150 -1.27) Unit in mm

(Note) This package is not available in Japan.



Weight : 0.13g (Typ.)