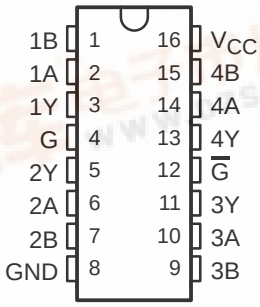
SN75ALS173
QUADRUPLE DIFFERENTIAL LINE RECEIVER

SLLS132C – SEPTEMBER 1991 – REVISED MAY 1995

- **Meets or Exceeds the Requirements of ANSI EIA/TIA-422-B, EIA/TIA-423-B, and RS-485**
- **Meets or Exceeds the Requirements of ITU Recommendations V.10, V.11, X.26, and X.27**
- **Designed for Multipoint Bus Transmission on Long Bus Lines in Noisy Environments**
- **3-State Outputs**
- **Common-Mode Input Voltage Range of –12 V to 12 V**
- **Input Sensitivity . . . ±200 mV**
- **Input Hysteresis . . . 50 mV Typ**
- **High Input Impedance . . . 12 kΩ Min**
- **Operates From Single 5-V Supply**
- **Low Supply-Current Requirement 27 mA Max**

N OR NS† PACKAGE
(TOP VIEW)



† The NS package is only available left-end taped and reeled (order device SN75ALS173 NSLE).

description

The SN75ALS173 is a monolithic quadruple differential line receiver with 3-state outputs. It is designed to meet the requirements of ANSI Standards EIA/TIA-422-B, EIA/TIA-423-B, RS-485, and several ITU recommendations. Advanced low-power Schottky technology provides high speed without the usual power penalty. The four receivers have an ORed pair of enables in common. Either G high or $\overline{G}$ low enables all of the receivers. The device features high input impedance, input hysteresis for increased noise immunity, and input sensitivity of ±200 mV over a common-mode input voltage range of –12 V to 12 V.

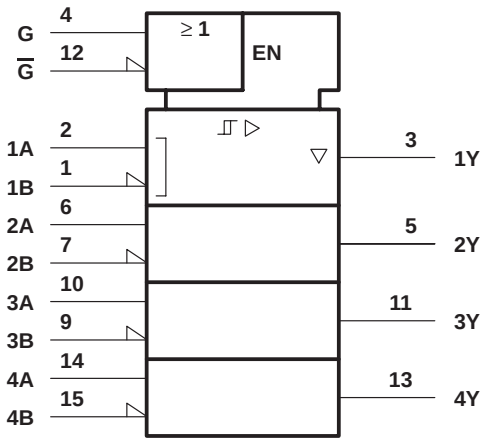
The SN75ALS173 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(each receiver)

DIFFERENTIAL A – B	ENABLES G	ENABLES $\overline{G}$	OUTPUT Y
$V_{ID} \geq 0.2$ V	H	X	H
	X	L	H
$-0.2\text{ V} < V_{ID} < 0.2$ V	H	X	?
	X	L	?
$V_{ID} \leq -0.2$ V	H	X	L
	X	L	L
X	L	H	Z
Open Circuit	H	X	H
	X	L	H

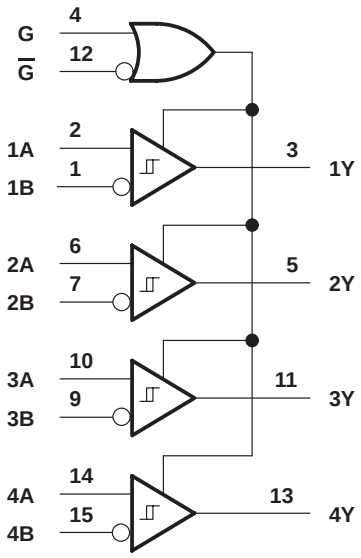
H = high level, L = low level, ? = indeterminate,
X = irrelevant, Z = high impedance (off)

logic symbol†

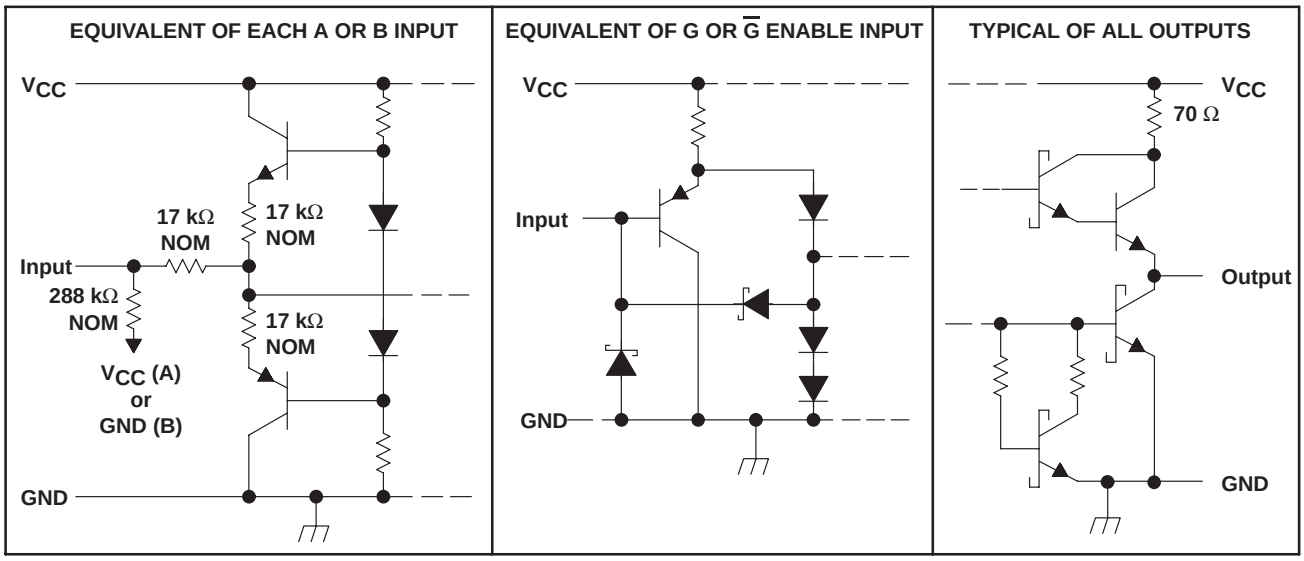


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage, V_I (A or B inputs) . . . . . ±14 V
Differential input voltage, V_{ID} (see Note 2) . . . . . ±14 V
Enable input voltage, V_I . . . . . 7 V
Low-level output current, I_{OL} . . . . . 50 mA
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.
2. Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
N	1150 mW	9.2 mW/°C	736 mW
NS	625 mW	5.0 mW/°C	400 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Common-mode input voltage, V_{IC}				±12	V
Differential input voltage, V_{ID}				±12	V
High-level input voltage, V_{IH}	G, $\overline{G}$	2			V
Low-level input voltage, V_{IL}	G, $\overline{G}$			0.8	V
High-level output current, I_{OH}				–400	µA
Low-level output current, I_{OL}				8	mA
Operating free-air temperature, T_A		0		70	°C

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted) (see Note 3)

PARAMETER			TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage							200	mV
V_{IT-}	Negative-going input threshold voltage					–200‡			mV
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)						50		mV
V_{IK}	Input clamp voltage	G, $\overline{G}$	I_I = –18 mA					–1.5	V
V_{OH}	High-level output voltage		V_{ID} = 200 mV,	I_{OH} = –400 μA,	See Figure 1	2.7			V
V_{OL}	Low-level output voltage		V_{ID} = –200 mV,	I_{OL} = 8 mA,	See Figure 1			0.45	V
I_{OZ}	High-impedance-state output current		V_O = 0.4 V to 2.4 V					±20	μA
I_I	Line input current		Other input at 0 V		V_I = 12 V			1	mA
					V_I = –7 V			–0.8	
I_{IH}	High-level input current	G, $\overline{G}$	V_{IH} = 2.7 V					20	μA
I_{IL}	Low-level input current	G, $\overline{G}$	V_{IL} = 0.4 V					–100	μA
r_i	Input resistance					12			kΩ
I_{OS}	Short-circuit output current		See Note 4			–15		–85	mA
I_{CC}	Supply current (total package)		No load,	Outputs enabled			16	24	mA
			No load,	Outputs disabled			18	27	

† All typical values are at V_{CC} = 5 V and T_A = 25°C.
‡ The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for threshold voltage levels only.

NOTES: 3. Refer to ANSI Standard RS-485 for exact conditions.
4. The duration of the short circuit should not cause the maximum package power dissipation to be exceeded.

switching characteristics, V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high- to low-level output	V_{ID} = –2.5 V to 2.5 V, See Figure 2	9	18	27	ns
t_{PLH}	Propagation delay time, low- to high-level output		9	18	27	ns
t_{PZH}	Output enable time to high level	See Figure 3	4	12	18	ns
t_{PZL}	Output enable time to low level	See Figure 4	6	13	21	ns
t_{PHZ}	Output disable time from high level	See Figure 3	10	21	27	ns
t_{PLZ}	Output disable time from low level	See Figure 4	8	15	25	ns

PARAMETER MEASUREMENT INFORMATION

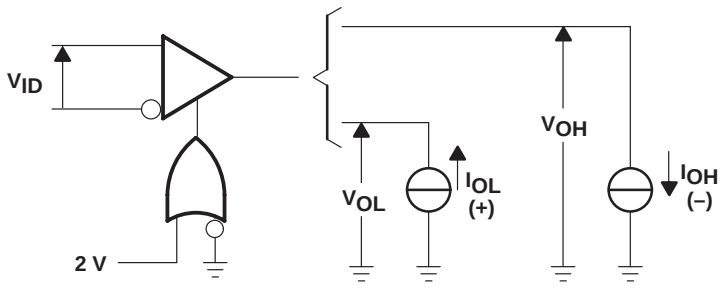


Figure 1. V_{OH}, V_{OL}

PARAMETER MEASUREMENT INFORMATION

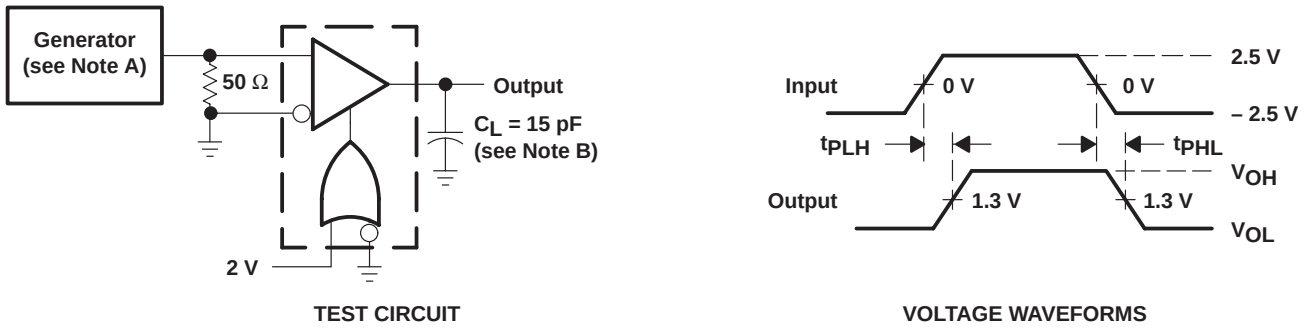


Figure 2. Test Circuit and Voltage Waveforms

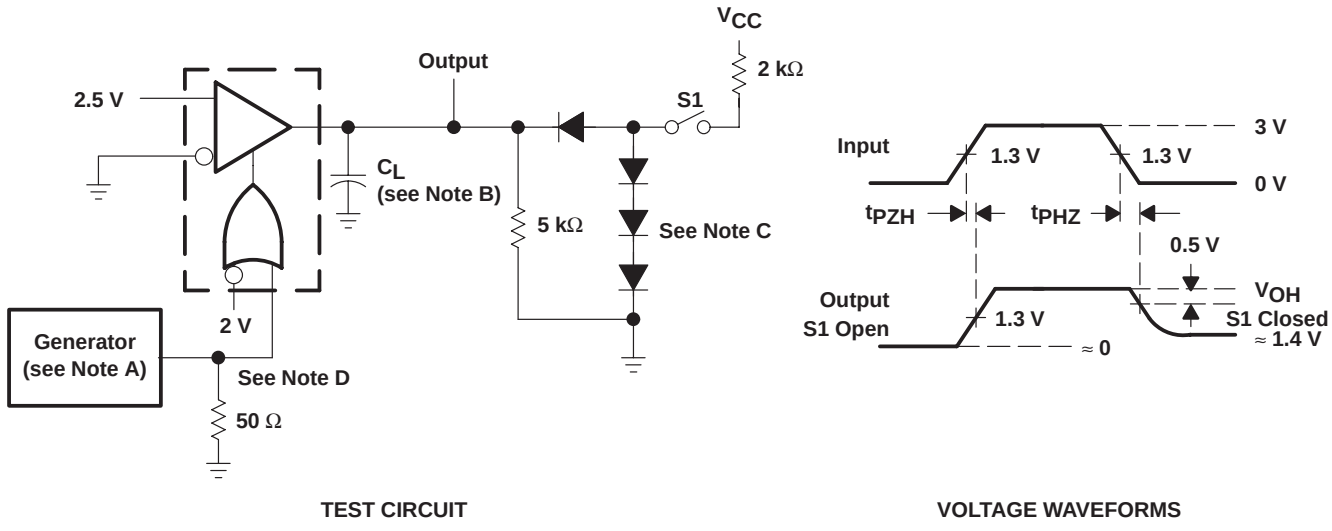
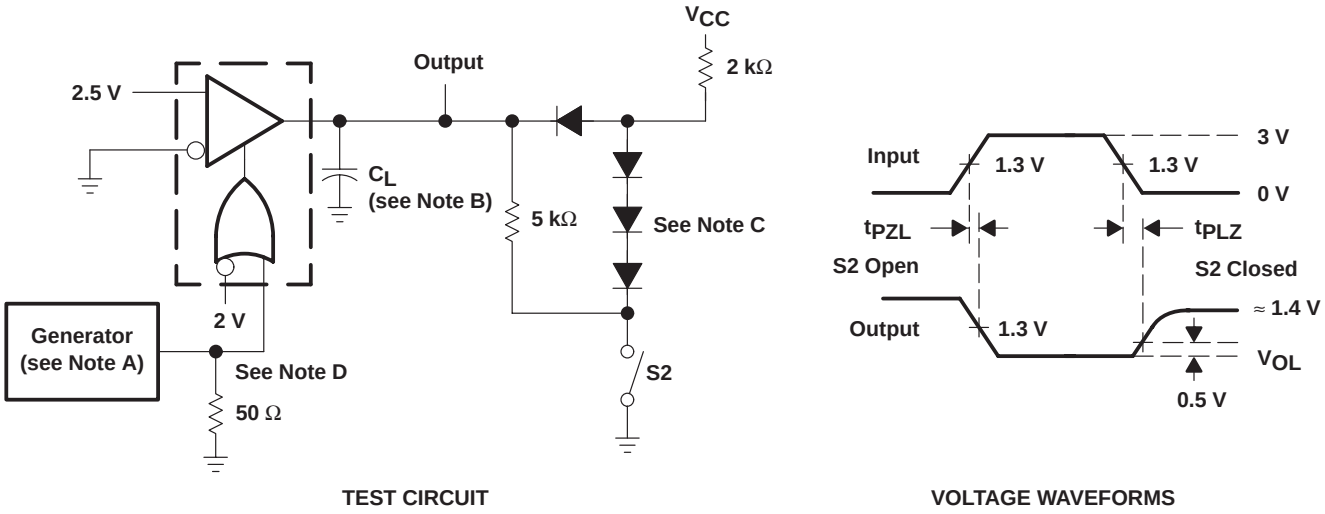


Figure 3. Test Circuit and Voltage Waveforms

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r \le 6$ ns, $t_f \le 6$ ns, $Z_O = 50\ \Omega$.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N916 or equivalent.
D. To test the active-low enable $\overline{G}$, ground G and apply an inverted input waveform to $\overline{G}$.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT **VOLTAGE WAVEFORMS**

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r \le 6$ ns, $t_f \le 6$ ns, $Z_O = 50\ \Omega$.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N916 or equivalent.
D. To test the active-low enable $\overline{G}$, ground G and apply an inverted input waveform to $\overline{G}$.

Figure 4. Test Circuit and Voltage Waveforms

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