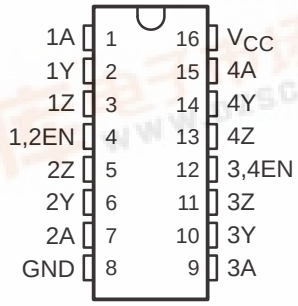
SN75ALS174A
QUADRUPLE DIFFERENTIAL LINE DRIVER

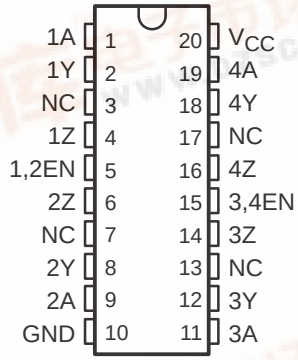
SLLS122E – JULY 1991 – REVISED APRIL 1998

- **Meets or Exceeds the Requirements of ANSI EIA/TIA-422-B and RS-485**
- **High-Speed Advanced Low-Power Schottky Circuitry**
- **Designed for up to 20-Mbit/s Operation in Both Serial and Parallel Applications**
- **Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments**
- **Low Supply Current Requirements 55 mA Max**
- **Wide Positive and Negative Input/Output Bus Voltage Ranges**
- **Driver Output Capacity . . . ±60 mA**
- **Thermal-Shutdown Protection**
- **Driver Positive- and Negative-Current Limiting**
- **Functionally Interchangeable With SN75174**

N PACKAGE
(TOP VIEW)



DW PACKAGE
(TOP VIEW)



NC – No internal connection

description

The SN75ALS174A is a quadruple line driver with 3-state differential outputs. It is designed to meet the requirements of ANSI Standards EIA/TIA-422-B and RS-485. This device is optimized for balanced multipoint bus transmission at rates of up to 20 Mbit/s. Each driver features wide positive and negative common-mode output voltage ranges that make them suitable for party-line applications in noisy environments.

The SN75ALS174A provides positive- and negative-current limiting and thermal shutdown for protection from line fault conditions on the transmission bus line. Shutdown occurs at a junction temperature of approximately 150°C.

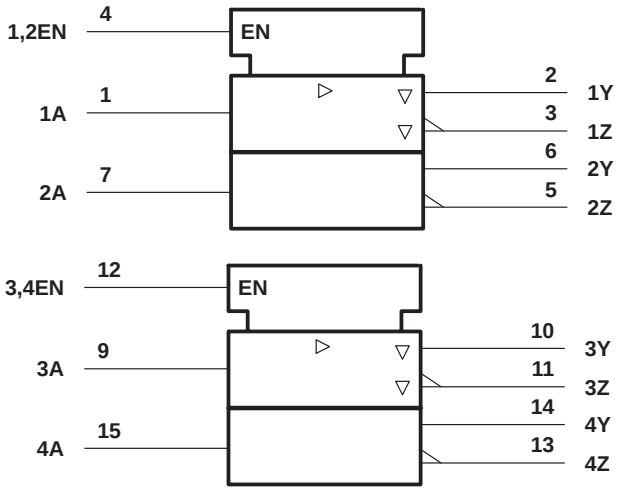
The SN75ALS174A is characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(each driver)

INPUT A	ENABLES	OUTPUTS	
		Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

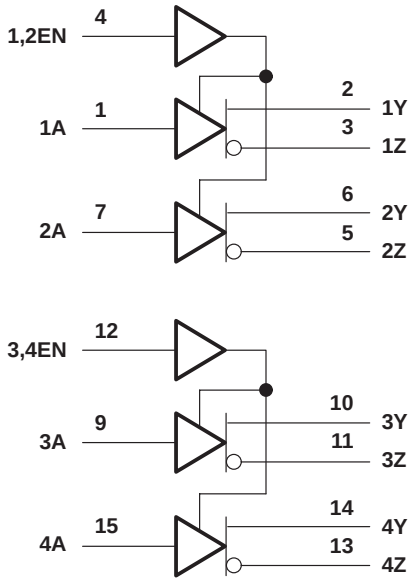
H = high level, L = low level, X = irrelevant,
Z = high impedance (off)

logic symbol†



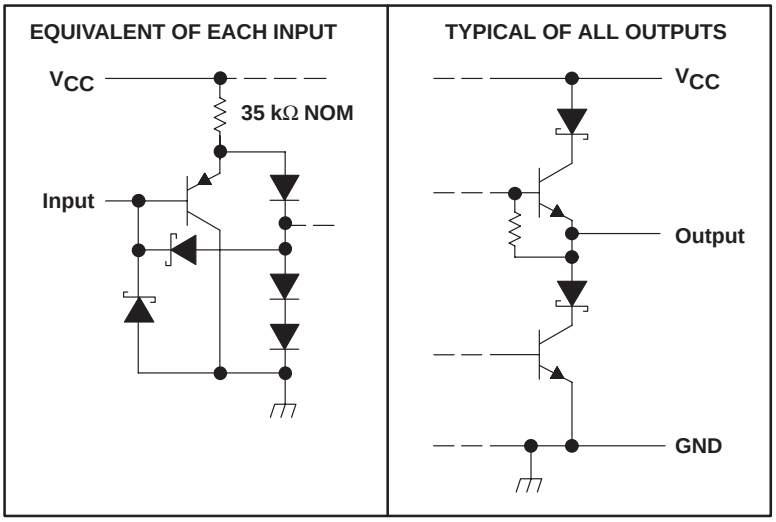
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the N package.

logic diagram (positive logic)



Pin numbers shown are for the N package.

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage, V_I . . . . . 7 V
Output voltage range, V_O . . . . . –9 V to 14 V
Continuous total dissipation . . . . . See Dissipation Rating Table
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to network GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DW	1125 mW	9.0 mW/°C	720 mW	585 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
Common-mode output voltage, V_{OC}			12 –7	V
High-level output current, I_{OH}			–60	mA
Low-level output current, I_{OL}			60	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = –18 mA				–1.5	V
V_O	Output voltage	I_O = 0		0		6	V
$\|V_{OD1}\|$	Differential output voltage	I_O = 0		1.5		6	V
$\|V_{OD2}\|$	Differential output voltage	R_L = 100 Ω	See Figure 1	1/2V_{OD1} or 2‡			V
		R_L = 54 Ω		1.5	2.5	5	
$\|V_{OD3}\|$	Differential output voltage	See Note 2		1.5		5	V
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage§	R_L = 54 Ω or 100 Ω,	See Figure 1			±0.2	V
V_{OC}	Common-mode output voltage¶	R_L = 54 Ω or 100 Ω,	See Figure 1			3 –1	V
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage§	R_L = 54 Ω or 100 Ω,	See Figure 1			±0.2	V
I_O	Output current with power off	V_{CC} = 0,	V_O = –7 V to 12 V			±100	µA
I_{OZ}	High-impedance-state output current	V_O = –7 V to 12 V				±100	µA
I_{IH}	High-level input current	V_I = 2.7 V				20	µA
I_{IL}	Low-level input current	V_I = 0.4 V				–100	µA
I_{OS}	Short-circuit output current	V_O = –7 V to 12 V				±250	mA
I_{CC}	Supply current (all drivers)	No load	Outputs enabled		36	55	mA
			Outputs disabled		16	30	

† All typical values are at V_{CC} = 5 V and T_A = 25°C.
‡ The minimum V_{OD2} with a 100-Ω load is either 1/2 V_{OD1} or 2 V, whichever is greater.
§ $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
¶ In ANSI Standard EIA/TIA-422-B, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.
NOTE 2: See EIA Standard RS-485, Figure 3-5, Test Termination Measurement 2.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
$t_{d(OD)}$	Differential output delay time	R_L = 54 Ω,	See Figure 2	9	15	22	ns
t_{PZH}	Output enable time to high level	R_L = 110 Ω,	See Figure 3	30	45	70	ns
t_{PZL}	Output enable time to low level	R_L = 110 Ω,	See Figure 4	25	40	65	ns
t_{PHZ}	Output disable time from high level	R_L = 110 Ω,	See Figure 3	10	20	35	ns
t_{PLZ}	Output disable time from low level	R_L = 110 Ω,	See Figure 4	10	30	45	ns

† All typical values are at V_{CC} = 5 V and T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

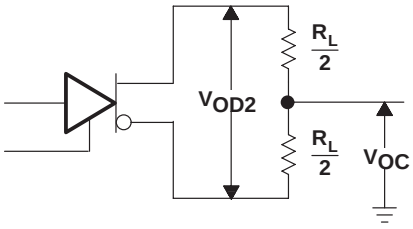
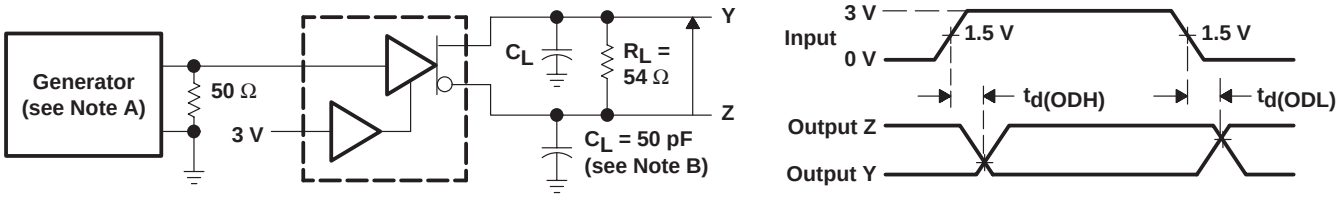
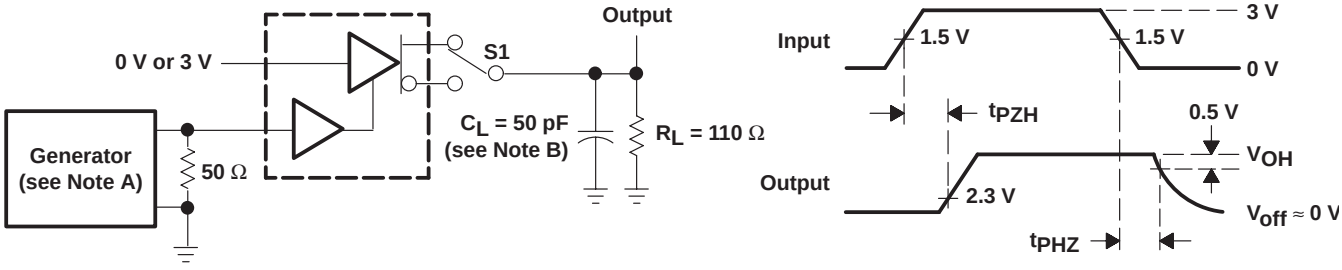


Figure 1. Differential and Common-Mode Output Voltages



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, Z_O = 50 Ω, duty cycle = 50%, $t_f \le 5$ ns, $t_r \le 5$ ns.
B. C_L includes probe and stray capacitance.

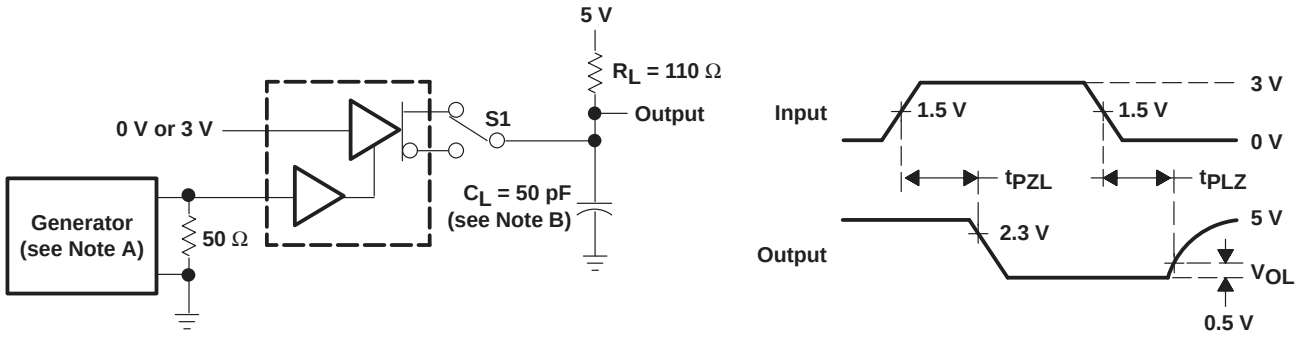
Figure 2. Differential-Output Test Circuit and Delay and Transition Times Voltage Waveforms



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, Z_O = 50 Ω, duty cycle = 50%, $t_f \le 5$ ns, $t_r \le 5$ ns.
B. C_L includes probe and stray capacitance.

Figure 3. Test Circuit and Voltage Waveforms, t_{PZH} and t_{PHZ}

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, Z_O = 50 Ω, duty cycle = 50%, $t_f \le 5$ ns, $t_r \le 5$ ns.
B. C_L includes probe and stray capacitance.

Figure 4. Test Circuit and Voltage Waveforms, t_{PZL} and t_{PLZ}

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.