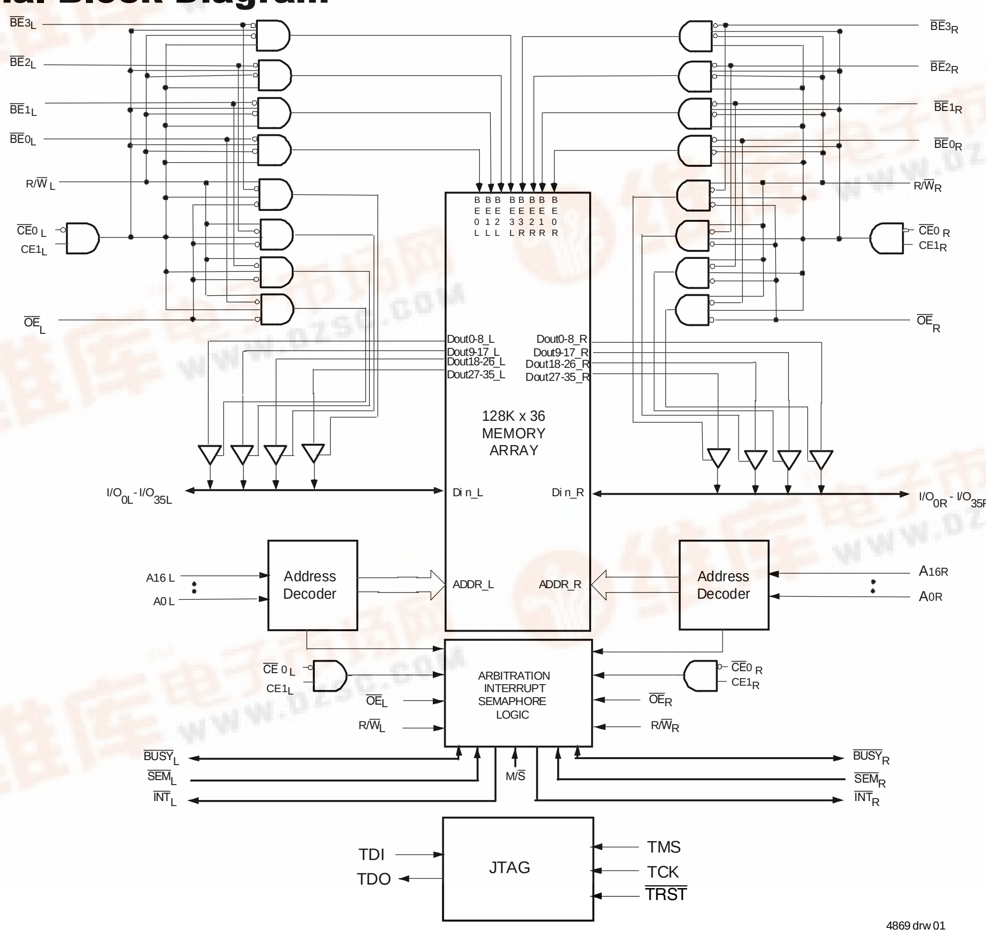
HIGH-SPEED 3.3V 128K x 36 ASYNCHRONOUS DUAL-PORT STATIC RAM

PRELIMINARY
IDT70V659S

Features

- True Dual-Port memory cells which allow simultaneous access of the same memory location
- High-speed access
  - *Commercial: 10/12/15ns (max.)*
  - *Industrial: 12/15ns (max.)*
- Dual chip enables allow for depth expansion without external logic
- IDT70V659 easily expands data bus width to 72 bits or more using the Master/Slave select when cascading more than one device
- M/$\overline{S}$ = VIH for $\overline{BUSY}$ output flag on Master, M/$\overline{S}$ = VIL for $\overline{BUSY}$ input on Slave
- Busy and Interrupt Flags
- On-chip port arbitration logic
- Full on-chip hardware support of semaphore signaling between ports
- Fully asynchronous operation from either port
- Separate byte controls for multiplexed bus and bus matching compatibility
- Supports JTAG features compliant to IEEE 1149.1
- LVTTL-compatible, single 3.3V (±150mV) power supply for core
- LVTTL-compatible, selectable 3.3V (±150mV)/2.5V (±100mV) power supply for I/Os and control signals on each port
- Available in a 208-pin Plastic Quad Flatpack, 208-ball fine pitch Ball Grid Array, and 256-ball Ball Grid Array
- Industrial temperature range (–40°C to +85°C) is available for selected speeds

Functional Block Diagram



NOTES:
1. $\overline{BUSY}$ is an input as a Slave (M/$\overline{S}$=VIL) and an output when it is a Master (M/$\overline{S}$=VIH).
2. $\overline{BUSY}$ and $\overline{INT}$ are non-tri-state totem-pole outputs (push-pull).

JUNE 2001

Description

The IDT70V659 is a high-speed 128K x 36 Asynchronous Dual-Port Static RAM. The IDT70V659 is designed to be used as a stand-alone 4608K-bit Dual-Port RAM or as a combination MASTER/SLAVE Dual-Port RAM for 72-bit-or-more word system. Using the IDT MASTER/SLAVE Dual-Port RAM approach in 72-bit or wider memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

This device provides two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature controlled by the chip enables (either $\overline{CE}_0$ or CE_1) permit the on-chip circuitry of each port to enter a very low standby power mode.

The 70V659 can support an operating voltage of either 3.3V or 2.5V on one or both ports, controlled by the OPT pins. The power supply for the core of the device (V_{DD}) remains at 3.3V.

Pin Configurations(1,2,3,4)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	
A	I/O$_{19L}$	I/O$_{18L}$	V_{SS}	TDO	NC	A_{16L}	A_{12L}	A_{8L}	$\overline{BE}_{1L}$	V_{DD}	$\overline{SEM}_L$	$\overline{INT}_L$	A_{4L}	A_{0L}	OPT$_L$	I/O$_{17L}$	V_{SS}	A
B	I/O$_{20R}$	V_{SS}	I/O$_{18R}$	TDI	NC	A_{13L}	A_{9L}	$\overline{BE}_{2L}$	$\overline{CE}_{0L}$	V_{SS}	$\overline{BUSY}_L$	A_{5L}	A_{1L}	V_{SS}	V_{DDQR}	I/O16L	I/O$_{15R}$	B
C	V_{DDQL}	I/O$_{19R}$	V_{DDQR}	V_{DD}	NC	A_{14L}	A_{10L}	$\overline{BE}_{3L}$	CE_{1L}	V_{SS}	$R/\overline{W}_L$	A_{6L}	A_{2L}	V_{DD}	I/O$_{16R}$	I/O$_{15L}$	V_{SS}	C
D	I/O$_{22L}$	V_{SS}	I/O$_{21L}$	I/O$_{20L}$	A_{15L}	A_{11L}	A_{7L}	$\overline{BE}_{0L}$	V_{DD}	$\overline{OE}_L$	NC	A_{3L}	V_{DD}	I/O$_{17R}$	V_{DDQL}	I/O$_{14L}$	I/O$_{14R}$	D
E	I/O$_{23L}$	I/O$_{22R}$	V_{DDQR}	I/O$_{21R}$										I/O$_{12L}$	I/O$_{13R}$	V_{SS}	I/O$_{13L}$	E
F	V_{DDQL}	I/O$_{23R}$	I/O$_{24L}$	V_{SS}										V_{SS}	I/O$_{12R}$	I/O$_{11L}$	V_{DDQR}	F
G	I/O$_{26L}$	V_{SS}	I/O$_{25L}$	I/O$_{24R}$										I/O$_{9L}$	V_{DDQL}	I/O$_{10L}$	I/O$_{11R}$	G
H	V_{DD}	I/O$_{26R}$	V_{DDQR}	I/O$_{25R}$										V_{DD}	I/O$_{9R}$	V_{SS}	I/O$_{10R}$	H
J	V_{DDQL}	V_{DD}	V_{SS}	V_{SS}										V_{SS}	V_{DD}	V_{SS}	V_{DDQR}	J
K	I/O$_{28R}$	V_{SS}	I/O$_{27R}$	V_{SS}										I/O$_{7R}$	V_{DDQL}	I/O8R	V_{SS}	K
L	I/O$_{29R}$	I/O$_{28L}$	V_{DDQR}	I/O$_{27L}$										I/O$_{6R}$	I/O$_{7L}$	V_{SS}	I/O$_{8L}$	L
M	V_{DDQL}	I/O$_{29L}$	I/O$_{30R}$	V_{SS}										V_{SS}	I/O$_{6L}$	I/O$_{5R}$	V_{DDQR}	M
N	I/O$_{31L}$	V_{SS}	I/O$_{31R}$	I/O$_{30L}$										I/O$_{3R}$	V_{DDQL}	I/O$_{4R}$	I/O$_{5L}$	N
P	I/O$_{32R}$	I/O$_{32L}$	V_{DDQR}	I/O$_{35R}$	$\overline{TRST}$	A_{16R}	A_{12R}	A_{8R}	$\overline{BE}_{1R}$	V_{DD}	$\overline{SEM}_R$	$\overline{INT}_R$	A_{4R}	I/O$_{2L}$	I/O$_{3L}$	V_{SS}	I/O$_{4L}$	P
R	V_{SS}	I/O$_{33L}$	I/O$_{34R}$	TCK	NC	A_{13R}	A_{9R}	$\overline{BE}_{2R}$	$\overline{CE}_{0R}$	V_{SS}	$\overline{BUSY}_R$	A_{5R}	A_{1R}	V_{SS}	V_{DDQL}	I/O$_{1R}$	V_{DDQR}	R
T	I/O$_{33R}$	I/O$_{34L}$	V_{DDQL}	TMS	NC	A_{14R}	A_{10R}	$\overline{BE}_{3R}$	CE_{1R}	V_{SS}	$R/\overline{W}_R$	A_{6R}	A_{2R}	V_{SS}	I/O$_{0R}$	V_{SS}	I/O$_{2R}$	T
U	V_{SS}	I/O$_{35L}$	V_{DD}	NC	A_{15R}	A_{11R}	A_{7R}	$\overline{BE}_{0R}$	V_{DD}	$\overline{OE}_R$	$M/\overline{S}$	A_{3R}	A_{0R}	V_{DD}	OPT$_R$	I/O$_{0L}$	I/O$_{1L}$	U

70V659BF
BF-208(5)

208-Ball BGA
Top View(6)

4869 tbl 02b

NOTES:

1. All V_{DD} pins must be connected to 3.3V power supply.
2. All V_{DDQ} pins must be connected to appropriate power supply: 3.3V if OPT pin for that port is set to V_{IH} (3.3V) and 2.5V if OPT pin for that port is set to V_{IL} (0V).
3. All V_{SS} pins must be connected to ground.
4. Package body is approximately 15mm x 15mm x 1.4mm with 0.8mm ball pitch.
5. This package code is used to reference the package diagram.
6. This text does not indicate orientation of the actual part-marking.

Pin Configurations[1,2,3,4] (con't.)

NOTES:

1. All V_{DD} pins must be connected to 3.3V power supply.
2. All V_{DDQ} pins must be connected to appropriate power supply: 3.3V if OPT pin for that port is set to V_{IH} (3.3V) and 2.5V if OPT pin for that port is set to V_{IL} (0V).
3. All V_{SS} pins must be connected to ground.
4. Package body is approximately 28mm x 28mm x 3.5mm.
5. This package code is used to reference the package diagram.
6. This text does not indicate orientation of the actual part-marking.

Pin Configuration(1,2,3,4) (con't.)

70V659BC
BC-256(5)

256-Pin BGA
Top View(6)

A1: NC	A2: TDI	A3: NC	A4: NC	A5: A_{14L}	A6: A_{11L}	A7: A_{8L}	A8: $\overline{BE}_{2L}$	A9: CE_{1L}	A10: $\overline{OE}_{L}$	A11: $\overline{INT}_{L}$	A12: A_{5L}	A13: A_{2L}	A14: A_{0L}	A15: NC	A16: NC
B1: I/O_{18L}	B2: NC	B3: TDO	B4: NC	B5: A_{15L}	B6: A_{12L}	B7: A_{9L}	B8: $\overline{BE}_{3L}$	B9: $\overline{CE}_{0L}$	B10: $R/\overline{W}_{L}$	B11: NC	B12: A_{4L}	B13: A_{1L}	B14: NC	B15: I/O_{17L}	B16: NC
C1: I/O_{18R}	C2: I/O_{19L}	C3: V_{SS}	C4: A_{16L}	C5: A_{13L}	C6: A_{10L}	C7: A_{7L}	C8: $\overline{BE}_{1L}$	C9: $\overline{BE}_{0L}$	C10: $\overline{SEM}_{L}$	C11: $\overline{BUSY}_{L}$	C12: A_{6L}	C13: A_{3L}	C14: OPT_{L}	C15: I/O_{17R}	C16: I/O_{16L}
D1: I/O_{20R}	D2: I/O_{19R}	D3: I/O_{20L}	D4: V_{DD}	D5: V_{DDQL}	D6: V_{DDQL}	D7: V_{DDQR}	D8: V_{DDQR}	D9: V_{DDQL}	D10: V_{DDQL}	D11: V_{DDQR}	D12: V_{DDQR}	D13: V_{DD}	D14: I/O_{15R}	D15: I/O_{15L}	D16: I/O_{16R}
E1: I/O_{21R}	E2: I/O_{21L}	E3: I/O_{22L}	E4: V_{DDQL}	E5: V_{DD}	E6: V_{DD}	E7: V_{SS}	E8: V_{SS}	E9: V_{SS}	E10: V_{SS}	E11: V_{DD}	E12: V_{DD}	E13: V_{DDQR}	E14: I/O_{13L}	E15: I/O_{14L}	E16: I/O_{14R}
F1: I/O_{23L}	F2: I/O_{22R}	F3: I/O_{23R}	F4: V_{DDQL}	F5: V_{DD}	F6: V_{SS}	F7: V_{SS}	F8: V_{SS}	F9: V_{SS}	F10: V_{SS}	F11: V_{SS}	F12: V_{DD}	F13: V_{DDQR}	F14: I/O_{12R}	F15: I/O_{13R}	F16: I/O_{12L}
G1: I/O_{24R}	G2: I/O_{24L}	G3: I/O_{25L}	G4: V_{DDQR}	G5: V_{SS}	G6: V_{SS}	G7: V_{SS}	G8: V_{SS}	G9: V_{SS}	G10: V_{SS}	G11: V_{SS}	G12: V_{SS}	G13: V_{DDQL}	G14: I/O_{10L}	G15: I/O_{11L}	G16: I/O_{11R}
H1: I/O_{26L}	H2: I/O_{25R}	H3: I/O_{26R}	H4: V_{DDQR}	H5: V_{SS}	H6: V_{SS}	H7: V_{SS}	H8: V_{SS}	H9: V_{SS}	H10: V_{SS}	H11: V_{SS}	H12: V_{SS}	H13: V_{DDQL}	H14: I/O_{9R}	H15: IO_{9L}	H16: I/O_{10R}
J1: I/O_{27L}	J2: I/O_{28R}	J3: I/O_{27R}	J4: V_{DDQL}	J5: V_{SS}	J6: V_{SS}	J7: V_{SS}	J8: V_{SS}	J9: V_{SS}	J10: V_{SS}	J11: V_{SS}	J12: V_{SS}	J13: V_{DDQR}	J14: I/O_{8R}	J15: I/O_{7R}	J16: I/O_{8L}
K1: I/O_{29R}	K2: I/O_{29L}	K3: I/O_{28L}	K4: V_{DDQL}	K5: V_{SS}	K6: V_{SS}	K7: V_{SS}	K8: V_{SS}	K9: V_{SS}	K10: V_{SS}	K11: V_{SS}	K12: V_{SS}	K13: V_{DDQR}	K14: I/O_{6R}	K15: I/O_{6L}	K16: I/O_{7L}
L1: I/O_{30L}	L2: I/O_{31R}	L3: I/O_{30R}	L4: V_{DDQR}	L5: V_{DD}	L6: V_{SS}	L7: V_{SS}	L8: V_{SS}	L9: V_{SS}	L10: V_{SS}	L11: V_{SS}	L12: V_{DD}	L13: V_{DDQL}	L14: I/O_{5L}	L15: I/O_{4R}	L16: I/O_{5R}
M1: I/O_{32R}	M2: I/O_{32L}	M3: I/O_{31L}	M4: V_{DDQR}	M5: V_{DD}	M6: V_{DD}	M7: V_{SS}	M8: V_{SS}	M9: V_{SS}	M10: V_{SS}	M11: V_{DD}	M12: V_{DD}	M13: V_{DDQL}	M14: I/O_{3R}	M15: I/O_{3L}	M16: I/O_{4L}
N1: I/O_{33L}	N2: I/O_{34R}	N3: I/O_{33R}	N4: V_{DD}	N5: V_{DDQR}	N6: V_{DDQR}	N7: V_{DDQL}	N8: V_{DDQL}	N9: V_{DDQR}	N10: V_{DDQR}	N11: V_{DDQL}	N12: V_{DDQL}	N13: V_{DD}	N14: I/O_{2L}	N15: I/O_{1R}	N16: I/O_{2R}
P1: I/O_{35R}	P2: I/O_{34L}	P3: TMS	P4: A_{16R}	P5: A_{13R}	P6: A_{10R}	P7: A_{7R}	P8: $\overline{BE}_{1R}$	P9: $\overline{BE}_{0R}$	P10: $\overline{SEM}_{R}$	P11: $\overline{BUSY}_{R}$	P12: A_{6R}	P13: A_{3R}	P14: I/O_{0L}	P15: I/O_{0R}	P16: I/O_{1L}
R1: I/O_{35L}	R2: NC	R3: $\overline{TRST}$	R4: NC	R5: A_{15R}	R6: A_{12R}	R7: A_{9R}	R8: $\overline{BE}_{3R}$	R9: $\overline{CE}_{0R}$	R10: $R/\overline{W}_{R}$	R11: $M/\overline{S}$	R12: A_{4R}	R13: A_{1R}	R14: OPT_{R}	R15: NC	R16: NC
T1: NC	T2: TCK	T3: NC	T4: NC	T5: A_{14R}	T6: A_{11R}	T7: A_{8R}	T8: $\overline{BE}_{2R}$	T9: CE_{1R}	T10: $\overline{OE}_{R}$	T11: $\overline{INT}_{R}$	T12: A_{5R}	T13: A_{2R}	T14: A_{0R}	T15: NC	T16: NC

4869 drw 02c

NOTES:
1. All V_{DD} pins must be connected to 3.3V power supply.
2. All V_{DDQ} pins must be connected to appropriate power supply: 3.3V if OPT pin for that port is set to V_{IH} (3.3V), and 2.5V if OPT pin for that port is set to V_{IL} (0V).
3. All V_{SS} pins must be connected to ground supply.
4. Package body is approximately 17mm x 17mm x 1.4mm, with 1.0mm ball-pitch.
5. This package code is used to reference the package diagram.
6. This text does not indicate orientation of the actual part-marking.

Pin Names

Left Port	Right Port	Names
$\overline{CE}_{0L}$, CE_{1L}	$\overline{CE}_{0R}$, CE_{1R}	Chip Enables
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
A_{0L} - A_{16L}	A_{0R} - A_{16R}	Address
I/O_{0L} - I/O_{35L}	I/O_{0R} - I/O_{35R}	Data Input/Output
$\overline{SEM}_L$	$\overline{SEM}_R$	Semaphore Enable
$\overline{INT}_L$	$\overline{INT}_R$	Interrupt Flag
$\overline{BUSY}_L$	$\overline{BUSY}_R$	Busy Flag
$\overline{BE}_{0L}$ - $\overline{BE}_{3L}$	$\overline{BE}_{0R}$ - $\overline{BE}_{3R}$	Byte Enables (9-bit bytes)
V_{DDQL}	V_{DDQR}	Power (I/O Bus) (3.3V or 2.5V)(1)
OPT_L	OPT_R	Option for selecting V_{DDQX}(1,2)
$M/\overline{S}$		Master or Slave Select
V_{DD}		Power (3.3V)(1)
V_{SS}		Ground (0V)
TDI		Test Data Input
TDO		Test Data Output
TCK		Test Logic Clock (10MHz)
TMS		Test Mode Select
$\overline{TRST}$		Reset (Initialize TAP Controller)

4869 tbl 01

NOTES:
1. V_{DD}, OPT_X, and V_{DDQX} must be set to appropriate operating levels prior to applying inputs on I/O_X.
2. OPT_X selects the operating voltage levels for the I/Os and controls on that port. If OPT_X is set to V_{IH} (3.3V), then that port's I/Os and controls will operate at 3.3V levels and V_{DDQX} must be supplied at 3.3V. If OPT_X is set to V_{IL} (0V), then that port's I/Os and controls will operate at 2.5V levels and V_{DDQX} must be supplied at 2.5V. The OPT pins are independent of one another—both ports can operate at 3.3V levels, both can operate at 2.5V levels, or either can operate at 3.3V with the other at 2.5V.

Truth Table I—Read/Write and Enable Control(1,2)

$\overline{OE}$	$\overline{SEM}$	$\overline{CE}_0$	CE_1	$\overline{BE}_3$	$\overline{BE}_2$	$\overline{BE}_1$	$\overline{BE}_0$	$R/\overline{W}$	Byte 3 I/O_{27-35}	Byte 2 I/O_{18-26}	Byte 1 I/O_{9-17}	Byte 0 I/O_{0-8}	MODE
X	H	H	X	X	X	X	X	X	High-Z	High-Z	High-Z	High-Z	Deselected–Power Down
X	H	X	L	X	X	X	X	X	High-Z	High-Z	High-Z	High-Z	Deselected–Power Down
X	H	L	H	H	H	H	H	X	High-Z	High-Z	High-Z	High-Z	All Bytes Deselected
X	H	L	H	H	H	H	L	L	High-Z	High-Z	High-Z	D_{IN}	Write to Byte 0 Only
X	H	L	H	H	H	L	H	L	High-Z	High-Z	D_{IN}	High-Z	Write to Byte 1 Only
X	H	L	H	H	L	H	H	L	High-Z	D_{IN}	High-Z	High-Z	Write to Byte 2 Only
X	H	L	H	L	H	H	H	L	D_{IN}	High-Z	High-Z	High-Z	Write to Byte 3 Only
X	H	L	H	H	H	L	L	L	High-Z	High-Z	D_{IN}	D_{IN}	Write to Lower 2 Bytes Only
X	H	L	H	L	L	H	H	L	D_{IN}	D_{IN}	High-Z	High-Z	Write to Upper 2 bytes Only
X	H	L	H	L	L	L	L	L	D_{IN}	D_{IN}	D_{IN}	D_{IN}	Write to All Bytes
L	H	L	H	H	H	H	L	H	High-Z	High-Z	High-Z	D_{OUT}	Read Byte 0 Only
L	H	L	H	H	H	L	H	H	High-Z	High-Z	D_{OUT}	High-Z	Read Byte 1 Only
L	H	L	H	H	L	H	H	H	High-Z	D_{OUT}	High-Z	High-Z	Read Byte 2 Only
L	H	L	H	L	H	H	H	H	D_{OUT}	High-Z	High-Z	High-Z	Read Byte 3 Only
L	H	L	H	H	H	L	L	H	High-Z	High-Z	D_{OUT}	D_{OUT}	Read Lower 2 Bytes Only
L	H	L	H	L	L	H	H	H	D_{OUT}	D_{OUT}	High-Z	High-Z	Read Upper 2 Bytes Only
L	H	L	H	L	L	L	L	H	D_{OUT}	D_{OUT}	D_{OUT}	D_{OUT}	Read All Bytes
H	H	L	H	L	L	L	L	X	High-Z	High-Z	High-Z	High-Z	Outputs Disabled

4869 tbl 02

NOTES:
1. "H" = V_{IH}, "L" = V_{IL}, "X" = Don't Care.
2. It is possible to read or write any combination of bytes during a given access. A few representative samples have been illustrated here.

Truth Table II – Semaphore Read/Write Control(1)

Inputs(1)								Outputs		
$\overline{CE}$(2)	$R/\overline{W}$	$\overline{OE}$	$\overline{BE}_3$	$\overline{BE}_2$	$\overline{BE}_1$	$\overline{BE}_0$	$\overline{SEM}$	I/O_{1-35}	I/O_0	Mode
H	H	L	L	L	L	L	L	$DATA_{OUT}$	$DATA_{OUT}$	Read Data in Semaphore Flag(3)
H	↑	X	X	X	X	L	L	X	$DATA_{IN}$	Write I/O_0 into Semaphore Flag
L	X	X	X	X	X	X	L	——	——	Not Allowed

486 tbl 03

NOTES:
1. There are eight semaphore flags written to I/O_0 and read from all the I/Os (I/O_0-I/O_{35}). These eight semaphore flags are addressed by A_0-A_2.
2. $\overline{CE}$ = L occurs when $\overline{CE}_0$ = V_{IL} and CE_1 = V_{IH}.
3. Each byte is controlled by the respective $\overline{BE}n$. To read data $\overline{BE}n$ = V_{IL}.

Maximum Operating Temperature and Supply Voltage(1)

Grade	Ambient Temperature	GND	VDD
Commercial	0°C to +70°C	0V	3.3V ± 150mV
Industrial	-40°C to +85°C	0V	3.3V ± 150mV

4869 tbl 04

NOTE:
1. This is the parameter TA. This is the "instant on" case temperature.

Absolute Maximum Ratings(1)

Symbol	Rating	Commercial & Industrial	Unit
VTERM(2)	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
TBIAS	Temperature Under Bias	-55 to +125	°C
TSTG	Storage Temperature	-65 to +150	°C
IOUT	DC Output Current	50	mA

4869 tbl 05

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. VTERM must not exceed VDD + 150mV for more than 25% of the cycle time or 4ns maximum, and is limited to ≤ 20mA for the period of VTERM ≥ VDD + 150mV.

Capacitance(1)

(TA = +25°C, F = 1.0MHz) PQFP ONLY

Symbol	Parameter	Conditions(2)	Max.	Unit
CIN	Input Capacitance	VIN = 3dV	8	pF
COUT(3)	Output Capacitance	VOUT = 3dV	10.5	pF

4869 tbl 08

NOTES:
1. These parameters are determined by device characterization, but are not production tested.
2. 3dV references the interpolated capacitance when the input and output switch from 0V to 3V or from 3V to 0V.
3. COUT also references CI/O.

Recommended DC Operating Conditions with VDDQ at 2.5V

Symbol	Parameter	Min.	Typ.	Max.	Unit
VDD	Core Supply Voltage	3.15	3.3	3.45	V
VDDQ	I/O Supply Voltage(3)	2.4	2.5	2.6	V
VSS	Ground	0	0	0	V
VIH	Input High Voltage(3) (Address & Control Inputs)	1.7	—	VDDQ + 100mV(2)	V
VIH	Input High Voltage - I/O(3)	1.7	—	VDDQ + 100mV(2)	V
VIL	Input Low Voltage	-0.5(1)	—	0.7	V

4869 tbl 06

NOTES:
1. VIL ≥ -1.5V for pulse width less than 10 ns.
2. VTERM must not exceed VDDQ + 100mV.
3. To select operation at 2.5V levels on the I/Os and controls of a given port, the OPT pin for that port must be set to VIL (0V), and VDDQX for that port must be supplied as indicated above.

Recommended DC Operating Conditions with VDDQ at 3.3V

Symbol	Parameter	Min.	Typ.	Max.	Unit
VDD	Core Supply Voltage	3.15	3.3	3.45	V
VDDQ	I/O Supply Voltage(3)	3.15	3.3	3.45	V
VSS	Ground	0	0	0	V
VIH	Input High Voltage (Address & Control Inputs)(3)	2.0	—	VDDQ + 150mV(2)	V
VIH	Input High Voltage - I/O(3)	2.0	—	VDDQ + 150mV(2)	V
VIL	Input Low Voltage	-0.3(1)	—	0.8	V

4869 tbl 07

NOTES:
1. VIL ≥ -1.5V for pulse width less than 10 ns.
2. VTERM must not exceed VDDQ + 150mV.
3. To select operation at 3.3V levels on the I/Os and controls of a given port, the OPT pin for that port must be set to VIH (3.3V), and VDDQX for that port must be supplied as indicated above.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (V_{DD} = 3.3V ± 150mV)

Symbol	Parameter	Test Conditions	70V659S Min.	70V659S Max.	Unit
$\|I_{LI}\|$	Input Leakage Current(1)	V_{DDQ} = Max., V_{IN} = 0V to V_{DDQ}	—	10	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}_0$ = V_{IH} or CE_1 = V_{IL}, V_{OUT} = 0V to V_{DDQ}	—	10	µA
V_{OL} (3.3V)	Output Low Voltage(2)	I_{OL} = +4mA, V_{DDQ} = Min.	—	0.4	V
V_{OH} (3.3V)	Output High Voltage(2)	I_{OH} = -4mA, V_{DDQ} = Min.	2.4	—	V
V_{OL} (2.5V)	Output Low Voltage(2)	I_{OL} = +2mA, V_{DDQ} = Min.	—	0.4	V
V_{OH} (2.5V)	Output High Voltage(2)	I_{OH} = -2mA, V_{DDQ} = Min.	2.0	—	V

4869 tbl 09

NOTE:
1. At V_{DD} ≤ - 2.0V input leakages are undefined.
2. V_{DDQ} is selectable (3.3V/2.5V) via OPT pins. Refer to p.5 for details.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range(3) (V_{DD} = 3.3V ± 150mV)

Symbol	Parameter	Test Condition	Version		70V659S10 Com'l Only		70V659S12 Com'l & Ind		70V659S15 Com'l & Ind		Unit
					Typ.(4)	Max.	Typ.(4)	Max.	Typ.(4)	Max.	
I_{DD}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}_L$ and $\overline{CE}_R$= V_{IL}, Outputs Disabled f = f_{MAX}(1)	COM'L	S	340	500	315	465	300	440	mA
			IND	S	—	—	365	515	350	490	
I_{SB1}	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_L$ = $\overline{CE}_R$ = V_{IH} f = f_{MAX}(1)	COM'L	S	115	165	90	125	75	100	mA
			IND	S	—	—	115	150	100	125	
I_{SB2}	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}$"A" = V_{IL} and $\overline{CE}$"B" = V_{IH}(5) Active Port Outputs Disabled, f=f_{MAX}(1)	COM'L	S	225	340	200	325	175	315	mA
			IND	S	—	—	225	365	200	350	
I_{SB3}	Full Standby Current (Both Ports - CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{DD} - 0.2V, V_{IN} ≥ V_{DD} - 0.2V or V_{IN} ≤ 0.2V, f = 0(2)	COM'L	S	3	15	3	15	3	15	mA
			IND	S	—	—	6	15	6	15	
I_{SB4}	Full Standby Current (One Port - CMOS Level Inputs)	$\overline{CE}$"A" ≤ 0.2V and $\overline{CE}$"B" ≥ V_{DD} - 0.2V(5) V_{IN} ≥ V_{DD} - 0.2V or V_{IN} ≤ 0.2V, Active Port, Outputs Disabled, f = f_{MAX}(1)	COM'L	S	220	335	195	320	170	310	mA
			IND	S	—	—	220	360	195	345	

4869 tbl 10

NOTES:
1. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/t_{RC}, using "AC TEST CONDITIONS" at input levels of GND to 3V.
2. f = 0 means no address or control lines change. Applies only to input at CMOS level standby.
3. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
4. V_{DD} = 3.3V, T_A = 25°C for Typ, and are not production tested. $I_{DD\,DC}$(f=0) = 120mA (Typ).
5. $\overline{CE}_X$ = V_{IL} means $\overline{CE}_{0X}$ = V_{IL} and CE_{1X} = V_{IH}
   $\overline{CE}_X$ = V_{IH} means $\overline{CE}_{0X}$ = V_{IH} or CE_{1X} = V_{IL}
   $\overline{CE}_X$ ≤ 0.2V means $\overline{CE}_{0X}$ ≤ 0.2V and CE_{1X} ≥ V_{CC} - 0.2V
   $\overline{CE}_X$ ≥ V_{CC} - 0.2V means $\overline{CE}_{0X}$ ≥ V_{CC} - 0.2V or CE_{1X} - 0.2V
   "X" represents "L" for left port or "R" for right port.

AC Test Conditions (V_{DDQ} - 3.3V/2.5V)

Input Pulse Levels	GND to 3.0V / GND to 2.5V
Input Rise/Fall Times	2ns Max.
Input Timing Reference Levels	1.5V/1.25V
Output Reference Levels	1.5V/1.25V
Output Load	Figures 1 and 2

4869 tbl 11

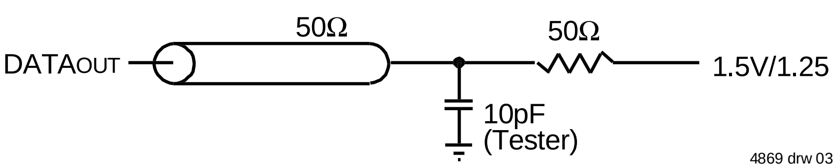


Figure 1. AC Output Test load.

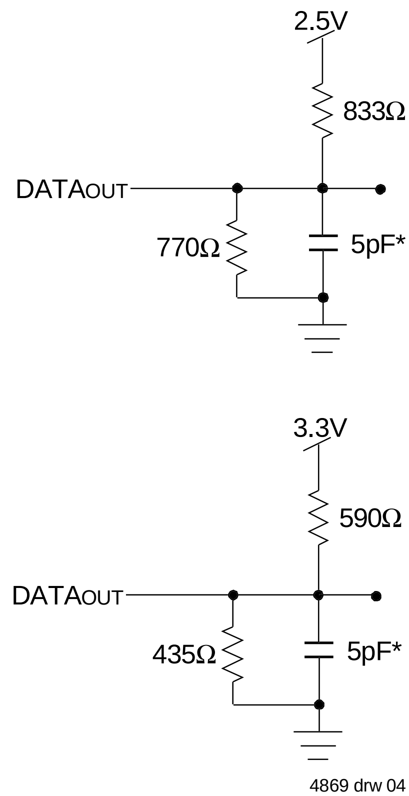


Figure 2. Output Test Load
(For t_{CKLZ}, t_{CKHZ}, t_{OLZ}, and t_{OHZ}).
*Including scope and jig.

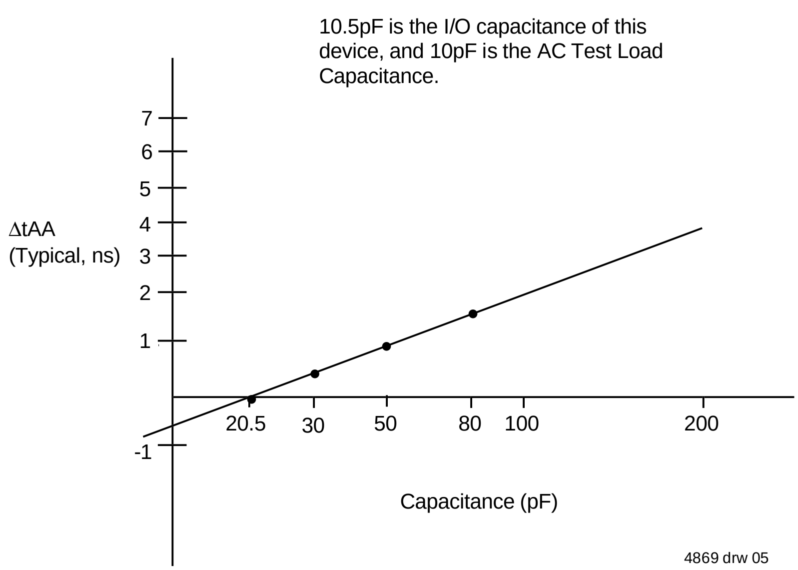


Figure 3. Typical Output Derating (Lumped Capacitive Load).

AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range[5]

Symbol	Parameter	70V659S10 Com'l Only		70V659S12 Com'l & Ind		70V659S15 Com'l & Ind		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	10	—	12	—	15	—	ns
t_{AA}	Address Access Time	—	10	—	12	—	15	ns
t_{ACE}	Chip Enable Access Time[3]	—	10	—	12	—	15	ns
t_{ABE}	Byte Enable Access Time[3]	—	5	—	6	—	7	ns
t_{AOE}	Output Enable Access Time	—	5	—	6	—	7	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	ns
t_{LZ}	Output Low-Z Time[1,2]	0	—	0	—	0	—	ns
t_{HZ}	Output High-Z Time[1,2]	0	4	0	6	0	8	ns
t_{PU}	Chip Enable to Power Up Time[2]	0	—	0	—	0	—	ns
t_{PD}	Chip Disable to Power Down Time[2]	—	10	—	10	—	15	ns
t_{SOP}	Semaphore Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	—	4	—	6	—	8	ns
t_{SAA}	Semaphore Address Access Time	3	10	3	12	3	20	ns

4869 tbl 12

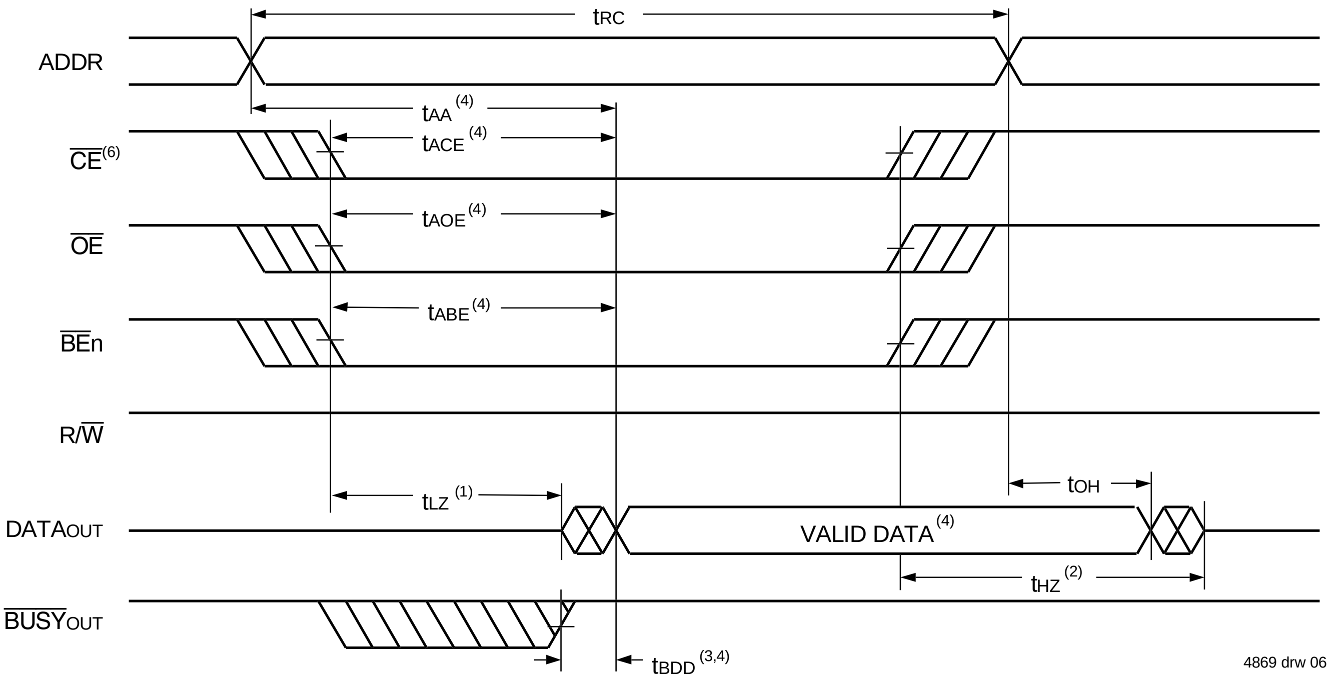
AC Electrical Characteristics Over the Operating Temperature and Supply Voltage[5]

Symbol	Parameter	70V659S10 Com'l Only		70V659S12 Com'l & Ind		70V659S15 Com'l & Ind		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE								
t_{WC}	Write Cycle Time	10	—	12	—	15	—	ns
t_{EW}	Chip Enable to End-of-Write[3]	8	—	10	—	12	—	ns
t_{AW}	Address Valid to End-of-Write	8	—	10	—	12	—	ns
t_{AS}	Address Set-up Time[3]	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	8	—	10	—	12	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End-of-Write	6	—	8	—	10	—	ns
t_{DH}	Data Hold Time[4]	0	—	0	—	0	—	ns
t_{WZ}	Write Enable to Output in High-Z[1,2]	—	4	—	4	—	4	ns
t_{OW}	Output Active from End-of-Write[1,2,4]	0	—	0	—	0	—	ns
t_{SWRD}	$\overline{SEM}$ Flag Write to Read Time	5	—	5	—	5	—	ns
t_{SPS}	$\overline{SEM}$ Flag Contention Window	5	—	5	—	5	—	ns

4869 tbl 13

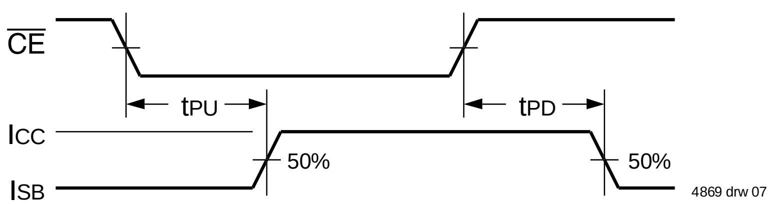
NOTES:
1. Transition is measured 0mV from Low or High-impedance voltage with Output Test Load (Figure 2).
2. This parameter is guaranted by device characterization, but is not production tested.
3. To access RAM, $\overline{CE}$= V_{IL} and $\overline{SEM}$ = V_{IH}. To access semaphore, $\overline{CE}$ = V_{IH} and $\overline{SEM}$ = V_{IL}. Either condition must be valid for the entire t_{EW} time.
4. The specification for t_{DH} must be met by the device supplying write data to the RAM under all operating conditions. Although t_{DH} and t_{OW} values will vary over voltage and temperature, the actual t_{DH} will always be smaller than the actual t_{OW}.
5. These values are valid regardless of the power supply level selected for I/O and control signals (3.3V/2.5V). See page 5 for details.

Waveform of Read Cycles(5)

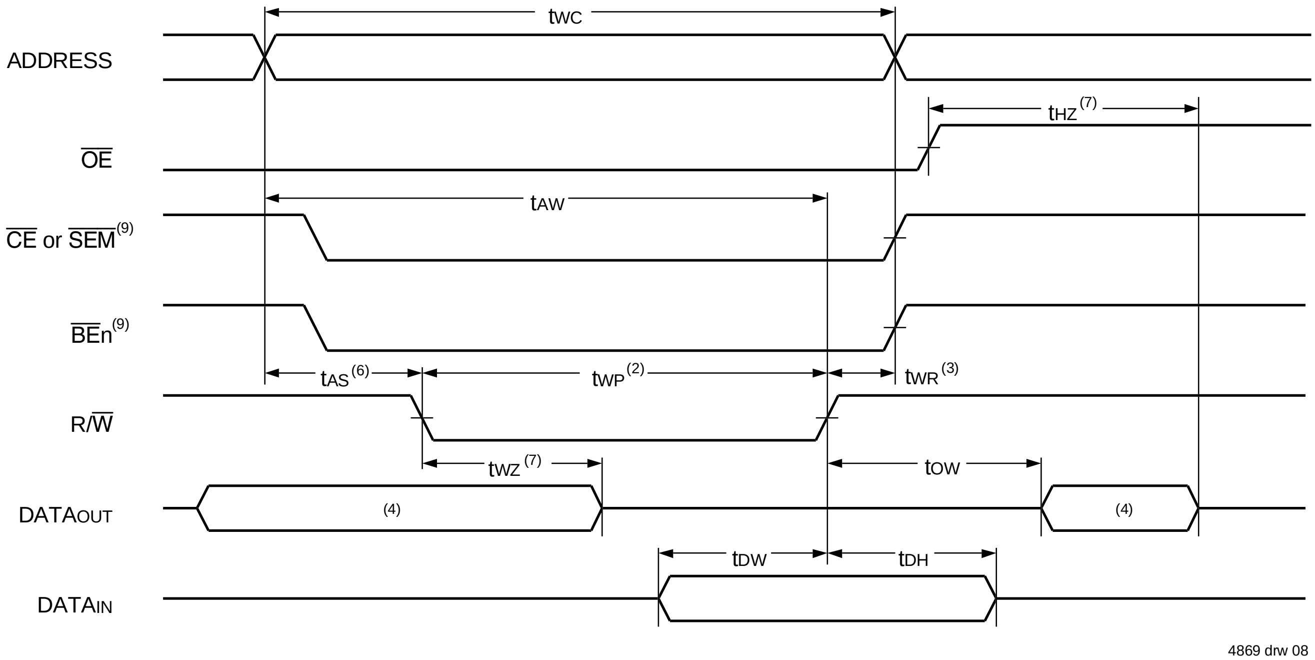


NOTES:
1. Timing depends on which signal is asserted last, OE, CE or BEn.
2. Timing depends on which signal is de-asserted first CE, OE or BEn.
3. t_{BDD} delay is required only in cases where the opposite port is completing a write operation to the same address location. For simultaneous read operations BUSY has no relation to valid output data.
4. Start of valid data depends on which timing becomes effective last t_{AOE}, t_{ACE}, t_{AA} or t_{BDD}.
5. SEM = V_{IH}.

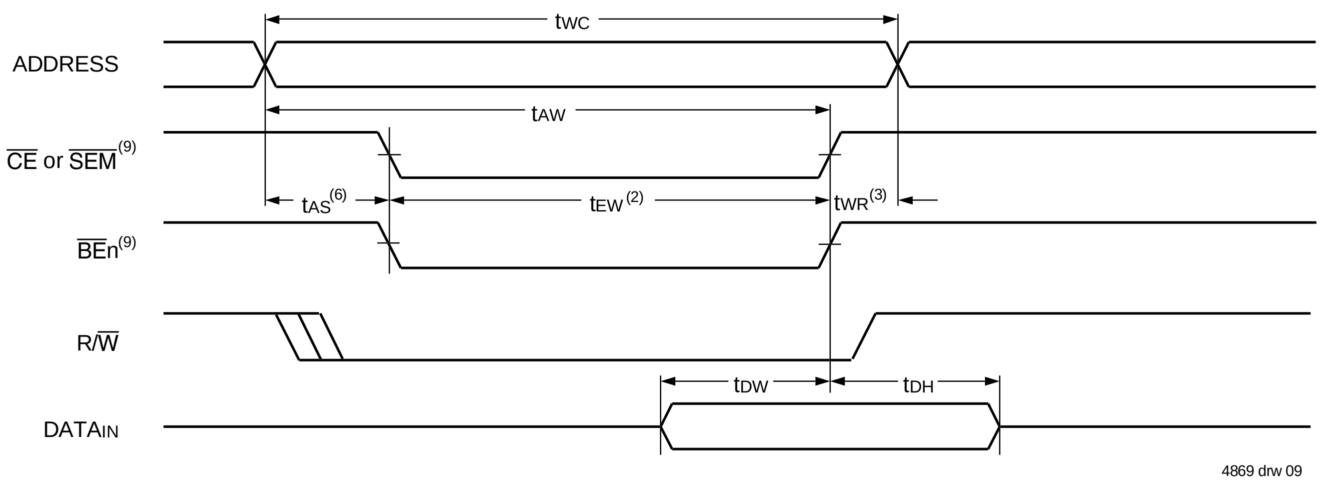
Timing of Power-Up Power-Down



Timing Waveform of Write Cycle No. 1, R/$\overline{W}$ Controlled Timing(1,5,8)

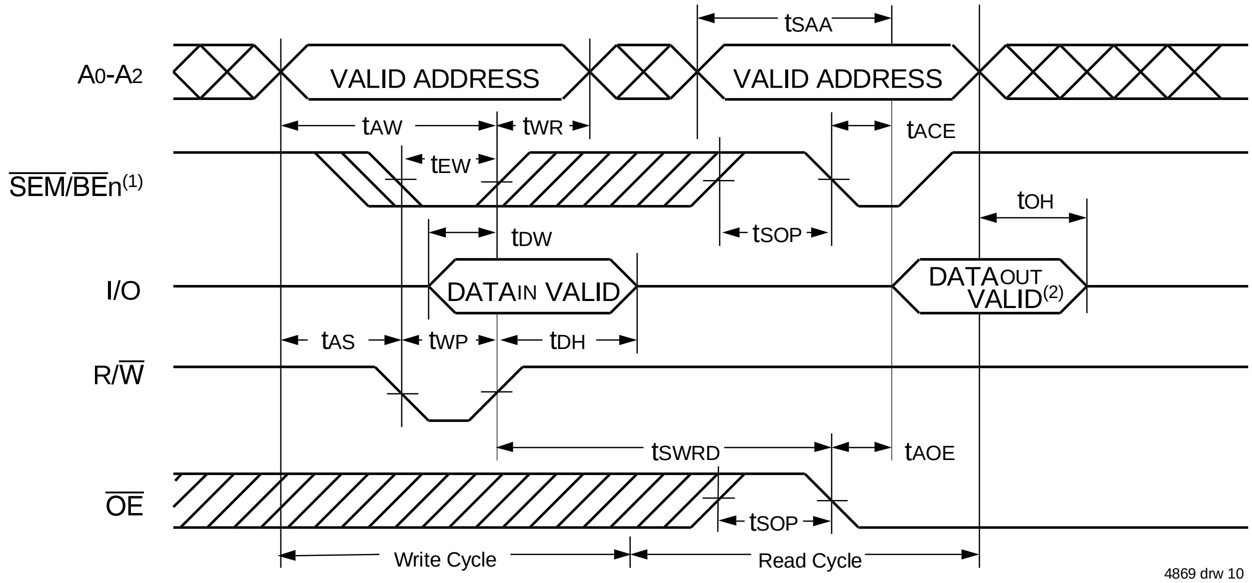


Timing Waveform of Write Cycle No. 2, $\overline{CE}$ Controlled Timing(1,5)



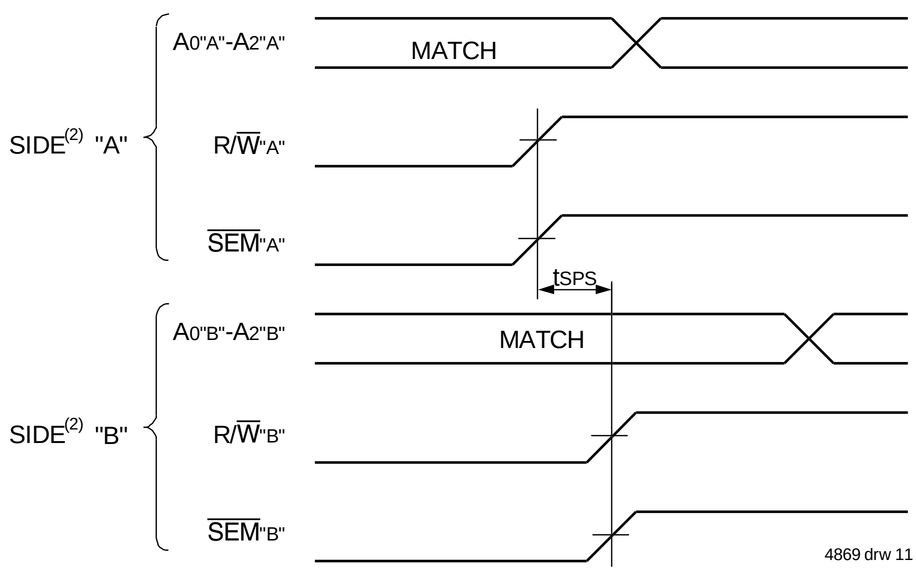
NOTES:
1. R/$\overline{W}$ or $\overline{CE}$ or $\overline{BE}$n = V_{IH} during all address transitions.
2. A write occurs during the overlap (t_{EW} or t_{WP}) of a $\overline{CE}$ = V_{IL} and a R/$\overline{W}$ = V_{IL} for memory array writing cycle.
3. t_{WR} is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ (or $\overline{SEM}$ or R/$\overline{W}$) going HIGH to the end of write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CE}$ or $\overline{SEM}$ = V_{IL} transition occurs simultaneously with or after the R/$\overline{W}$ = V_{IL} transition, the outputs remain in the High-impedance state.
6. Timing depends on which enable signal is asserted last, $\overline{CE}$ or R/$\overline{W}$.
7. This parameter is guaranteed by device characterization, but is not production tested. Transition is measured 0mV from steady state with the Output Test Load (Figure 2).
8. If $\overline{OE}$ = V_{IL} during R/W controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ = V_{IH} during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.
9. To access RAM, $\overline{CE}$ = V_{IL} and $\overline{SEM}$ = V_{IH}. To access semaphore, $\overline{CE}$ = V_{IH} and $\overline{SEM}$ = V_{IL}. t_{EW} must be met for either condition.

Timing Waveform of Semaphore Read after Write Timing, Either Side(1)



NOTES:
1. CE = VIH for the duration of the above timing (both write and read cycle) (Refer to Chip Enable Truth Table). Refer also to Truth Table II for appropriate BE controls.
2. "DATAOUT VALID" represents all I/O's (I/O0 - I/O35) equal to the semaphore value.

Timing Waveform of Semaphore Write Contention(1,3,4)



NOTES:
1. DOR = DOL = VIL, CEL = CER = VIH. Refer to Truth Table II for appropriate BE controls.
2. All timing is the same for left and right ports. Port "A" may be either left or right port. "B" is the opposite from port "A".
3. This parameter is measured from R/W"A" or SEM"A" going HIGH to R/W"B" or SEM"B" going HIGH.
4. If tSPS is not satisfied,the semaphore will fall positively to one side or the other, but there is no guarantee which side will be granted the semaphore flag.

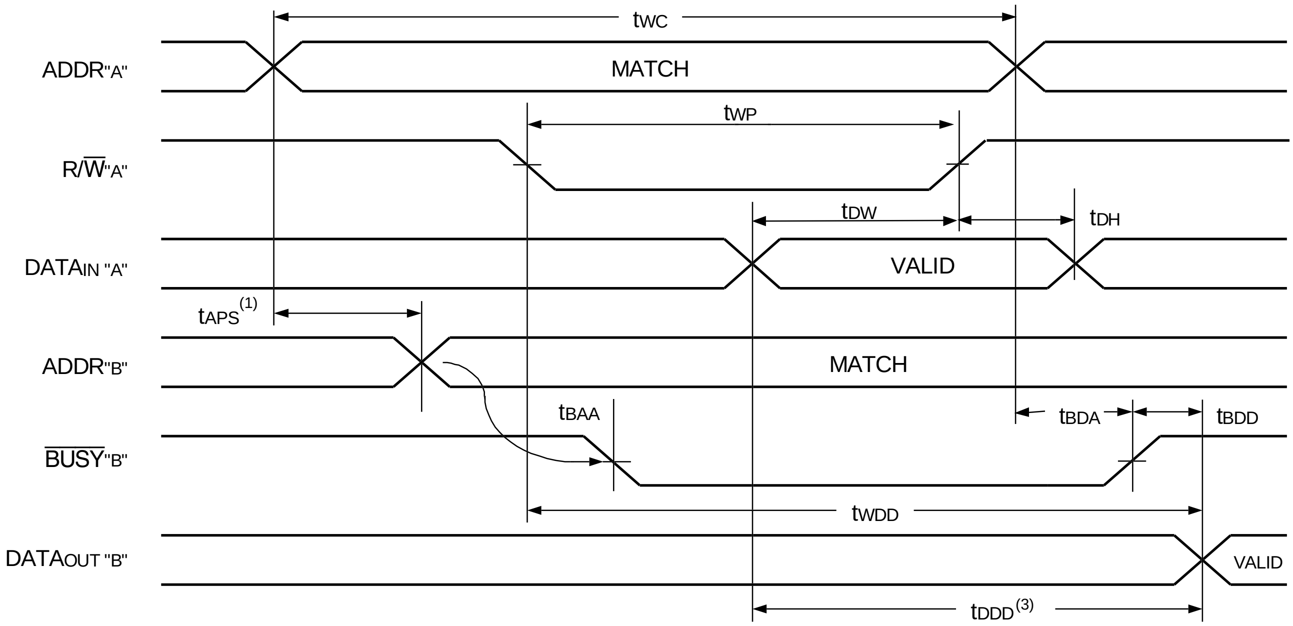
AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range

Symbol	Parameter	70V659S10 Com'l Only		70V659S12 Com'l & Ind		70V659S15 Com'l & Ind		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
$\overline{BUSY}$ TIMING (M/$\overline{S}$=V_{IH})								
t_{BAA}	$\overline{BUSY}$ Access Time from Address Match	—	10	—	12	—	15	ns
t_{BDA}	$\overline{BUSY}$ Disable Time from Address Not Matched	—	10	—	12	—	15	ns
t_{BAC}	$\overline{BUSY}$ Access Time from Chip Enable Low	—	10	—	12	—	15	ns
t_{BDC}	$\overline{BUSY}$ Disable Time from Chip Enable High	—	10	—	12	—	15	ns
t_{APS}	Arbitration Priority Set-up Time[2]	5	—	5	—	5	—	ns
t_{BDD}	$\overline{BUSY}$ Disable to Valid Data[3]	—	10	—	12	—	15	ns
t_{WH}	Write Hold After $\overline{BUSY}$[5]	8	—	10	—	12	—	ns
$\overline{BUSY}$ TIMING (M/$\overline{S}$=V_{IL})								
t_{WB}	$\overline{BUSY}$ Input to Write[4]	0	—	0	—	0	—	ns
t_{WH}	Write Hold After $\overline{BUSY}$[5]	8	—	10	—	12	—	ns
PORT-TO-PORT DELAY TIMING								
t_{WDD}	Write Pulse to Data Delay[1]	—	22	—	25	—	30	ns
t_{DDD}	Write Data Valid to Read Data Delay[1]	—	20	—	22	—	25	ns

4869 tbl 14

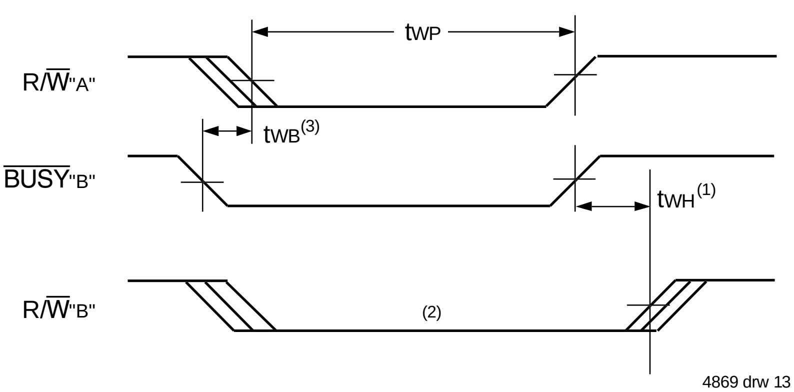
NOTES:
1. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Write with Port-to-Port Read and $\overline{BUSY}$ (M/$\overline{S}$ = V_{IH})".
2. To ensure that the earlier of the two ports wins.
3. t_{BDD} is a calculated parameter and is the greater of the Max. spec, t_{WDD} – t_{WP} (actual), or t_{DDD} – t_{DW} (actual).
4. To ensure that the write cycle is inhibited on port "B" during contention on port "A".
5. To ensure that a write cycle is completed on port "B" after contention on port "A".

Timing Waveform of Write with Port-to-Port Read and $\overline{BUSY}$ (M/$\overline{S}$ = V_{IH})(2,4,5)



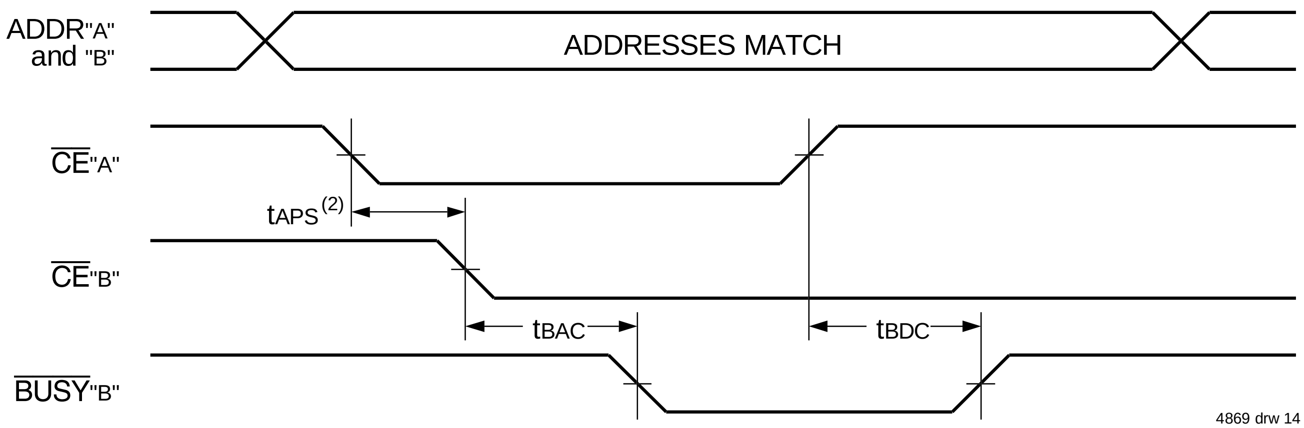
NOTES:
1. To ensure that the earlier of the two ports wins. t_{APS} is ignored for M/$\overline{S}$ = V_{IL} (SLAVE).
2. $\overline{CE}_L$ = $\overline{CE}_R$ = V_{IL}.
3. $\overline{OE}$ = V_{IL} for the reading port.
4. If M/$\overline{S}$ = V_{IL} (slave), $\overline{BUSY}$ is an input. Then for this example $\overline{BUSY}$"A" = V_{IH} and $\overline{BUSY}$"B" input is shown above.
5. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from port "A".

Timing Waveform of Write with $\overline{BUSY}$ (M/$\overline{S}$ = V_{IL})

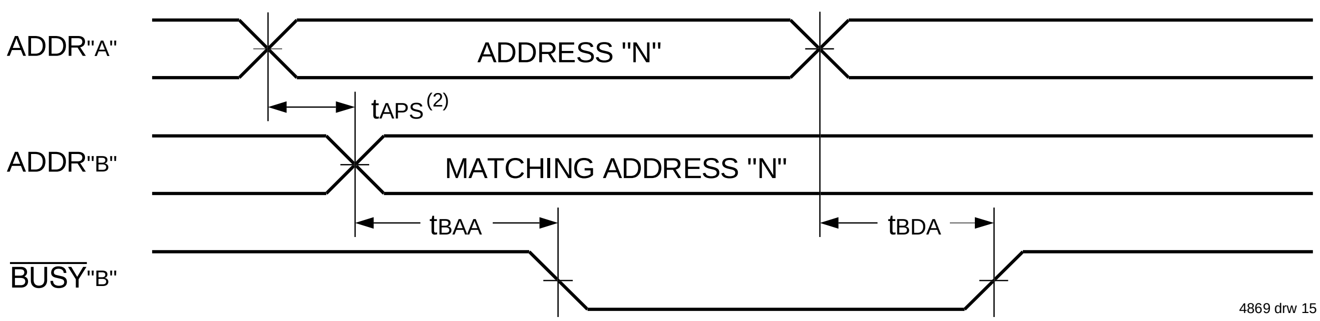


NOTES:
1. t_{WH} must be met for both $\overline{BUSY}$ input (SLAVE) and output (MASTER).
2. $\overline{BUSY}$ is asserted on port "B" blocking R/$\overline{W}$"B", until $\overline{BUSY}$"B" goes HIGH.
3. t_{WB} is only for the 'slave' version.

Waveform of BUSY Arbitration Controlled by CE Timing (M/S = VIH)(1)



Waveform of BUSY Arbitration Cycle Controlled by Address Match Timing (M/S = VIH)(1)



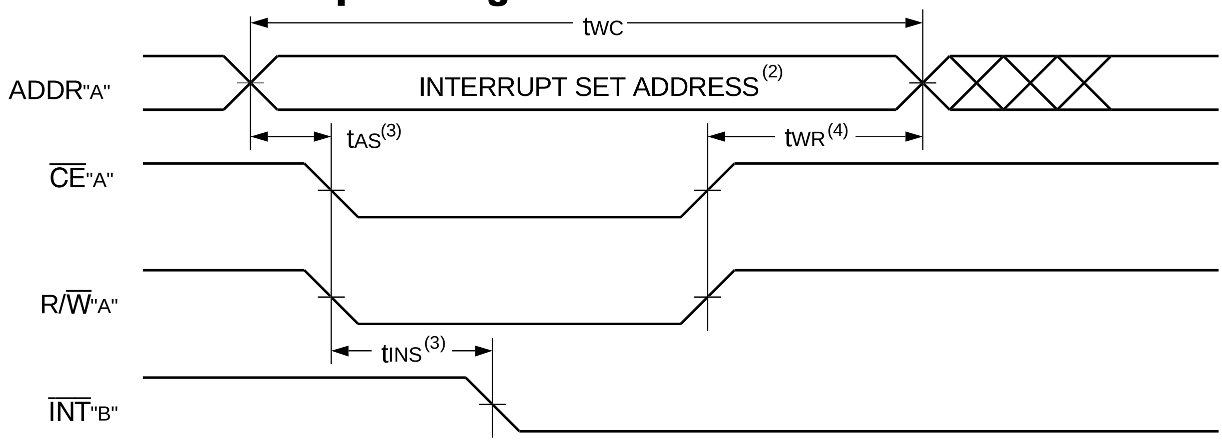
NOTES:
1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from port "A".
2. If tAPS is not satisfied, the BUSY signal will be asserted on one side or another but there is no guarantee on which side BUSY will be asserted.

AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range

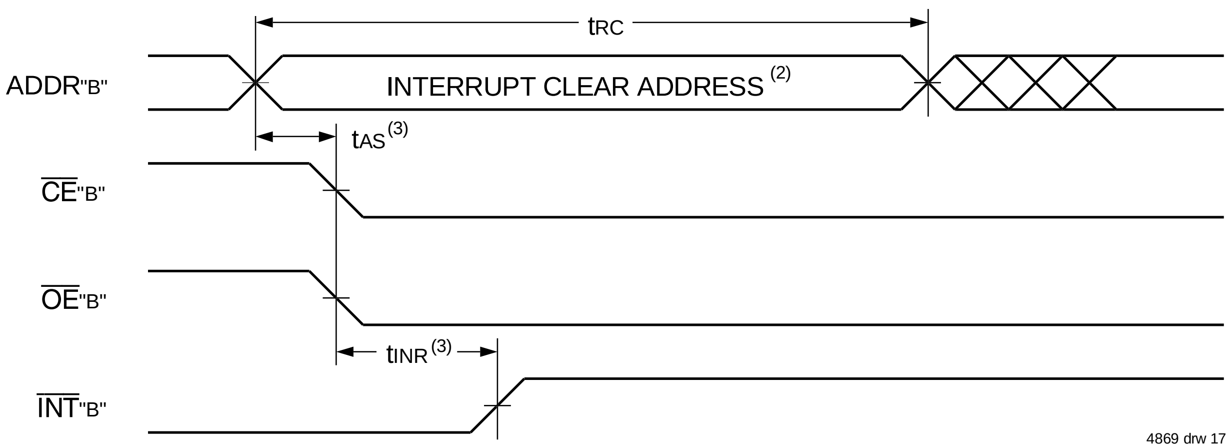
		70V659S10 Com'l Only		70V659S12 Com'l & Ind		70V659S15 Com'l & Ind		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
INTERRUPT TIMING								
tAS	Address Set-up Time	0	—	0	—	0	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tINS	Interrupt Set Time	—	10	—	12	—	15	ns
tINR	Interrupt Reset Time	—	10	—	12	—	15	ns

4869 tbl 15

Waveform of Interrupt Timing(1)



4869 drw 16



4869 drw 17

NOTES:

1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from port "A".
2. Refer to Interrupt Truth Table.
3. Timing depends on which enable signal ($\overline{CE}$ or R/$\overline{W}$) is asserted last.
4. Timing depends on which enable signal ($\overline{CE}$ or R/$\overline{W}$) is de-asserted first.

Truth Table III — Interrupt Flag(1,4)

Left Port					Right Port					Function
R/$\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	A_{16L}-A_{0L}	$\overline{INT}_L$	R/$\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	A_{16R}-A_{0R}	$\overline{INT}_R$	
L	L	X	1FFFF	X	X	X	X	X	L(2)	Set Right $\overline{INT}_R$ Flag
X	X	X	X	X	X	L	L	1FFFF	H(3)	Reset Right $\overline{INT}_R$ Flag
X	X	X	X	L(3)	L	L	X	1FFFE	X	Set Left $\overline{INT}_L$ Flag
X	L	L	1FFFE	H(2)	X	X	X	X	X	Reset Left $\overline{INT}_L$ Flag

4869 tbl 16

NOTES:

1. Assumes $\overline{BUSY}_L$ = $\overline{BUSY}_R$ =V_{IH}.
2. If $\overline{BUSY}_L$ = V_{IL}, then no change.
3. If $\overline{BUSY}_R$ = V_{IL}, then no change.
4. $\overline{INT}_L$ and $\overline{INT}_R$ must be initialized at power-up.

Truth Table IV — Address $\overline{BUSY}$ Arbitration

Inputs			Outputs		Function
$\overline{CE}_L$	$\overline{CE}_R$	A_{0L}-A_{16L} A_{0R}-A_{16R}	$\overline{BUSY}_L$(1)	$\overline{BUSY}_R$(1)	
X	X	NO MATCH	H	H	Normal
H	X	MATCH	H	H	Normal
X	H	MATCH	H	H	Normal
L	L	MATCH	(2)	(2)	Write Inhibit(3)

4869 tbl 17

NOTES:
1. Pins $\overline{BUSY}_L$ and $\overline{BUSY}_R$ are both outputs when the part is configured as a master. Both are inputs when configured as a slave. $\overline{BUSY}$ outputs on the IDT70V659 are push-pull, not open drain outputs. On slaves the $\overline{BUSY}$ input internally inhibits writes.
2. "L" if the inputs to the opposite port were stable prior to the address and enable inputs of this port. "H" if the inputs to the opposite port became stable after the address and enable inputs of this port. If t_{APS} is not met, either $\overline{BUSY}_L$ or $\overline{BUSY}_R$ = LOW will result. $\overline{BUSY}_L$ and $\overline{BUSY}_R$ outputs can not be LOW simultaneously.
3. Writes to the left port are internally ignored when $\overline{BUSY}_L$ outputs are driving LOW regardless of actual logic level on the pin. Writes to the right port are internally ignored when $\overline{BUSY}_R$ outputs are driving LOW regardless of actual logic level on the pin.

Truth Table V — Example of Semaphore Procurement Sequence(1,2,3)

Functions	D_0 - D_{35} Left	D_0 - D_{35} Right	Status
No Action	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Right Port Writes "0" to Semaphore	0	1	No change. Right side has no write access to semaphore
Left Port Writes "1" to Semaphore	1	0	Right port obtains semaphore token
Left Port Writes "0" to Semaphore	1	0	No change. Left port has no write access to semaphore
Right Port Writes "1" to Semaphore	0	1	Left port obtains semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free
Right Port Writes "0" to Semaphore	1	0	Right port has semaphore token
Right Port Writes "1" to Semaphore	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free

4869 tbl 18

NOTES:
1. This table denotes a sequence of events for only one of the eight semaphores on the IDT70V659.
2. There are eight semaphore flags written to via I/O_0 and read from all I/O's (I/O_0-I/O_{35}). These eight semaphores are addressed by A_0 - A_2.
3. $\overline{CE}$ = V_{IH}, $\overline{SEM}$ = V_{IL} to access the semaphores. Refer to the Semaphore Read/Write Control Truth Table.

Functional Description

The IDT70V659 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. The IDT70V659 has an automatic power down feature controlled by $\overline{CE}$. The $\overline{CE}_0$ and CE_1 control the on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ = HIGH). When a port is enabled, access to the entire memory array is permitted.

Interrupts

If the user chooses the interrupt function, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag ($\overline{INT}_L$) is asserted when the right port writes to memory location 1FFFE (HEX), where a write is defined as $\overline{CE}_R$ = R/$\overline{W}_R$ = V_{IL} per the Truth Table. The left port clears the interrupt through access of address location 1FFFE when $\overline{CE}_L$ = $\overline{OE}_L$ = V_{IL}, R/$\overline{W}$ is a "don't care". Likewise, the right port interrupt flag ($\overline{INT}_R$) is asserted when the left port writes to memory location 1FFFF (HEX) and to clear the interrupt flag ($\overline{INT}_R$), the right port must read the memory location 1FFFF. The message (36 bits) at 1FFFE or 1FFFF is user-defined since it is an addressable SRAM location. If the interrupt function is not used, address locations 1FFFE and 1FFFF are not used as mail boxes, but as part of the random access memory. Refer to Truth Table III for the interrupt operation.

Busy Logic

Busy Logic provides a hardware indication that both ports of the RAM have accessed the same location at the same time. It also allows one of the two accesses to proceed and signals the other side that the RAM is "Busy". The $\overline{BUSY}$ pin can then be used to stall the access until the operation on the other side is completed. If a write operation has been attempted from the side that receives a $\overline{BUSY}$ indication, the write signal is gated internally to prevent the write from proceeding.

The use of $\overline{BUSY}$ logic is not required or desirable for all applications. In some cases it may be useful to logically OR the $\overline{BUSY}$ outputs together and use any $\overline{BUSY}$ indication as an interrupt source to flag the event of an illegal or illogical operation. If the write inhibit function of $\overline{BUSY}$ logic is not desirable, the $\overline{BUSY}$ logic can be disabled by placing the part in slave mode with the M/$\overline{S}$ pin. Once in slave mode the $\overline{BUSY}$ pin operates solely as a write inhibit input pin. Normal operation can be programmed by tying the $\overline{BUSY}$ pins HIGH. If desired, unintended write operations can be prevented to a port by tying the $\overline{BUSY}$ pin for that port LOW.

The $\overline{BUSY}$ outputs on the IDT70V659 RAM in master mode, are push-pull type outputs and do not require pull up resistors to operate. If these RAMs are being expanded in depth, then the $\overline{BUSY}$ indication for the resulting array requires the use of an external AND gate.

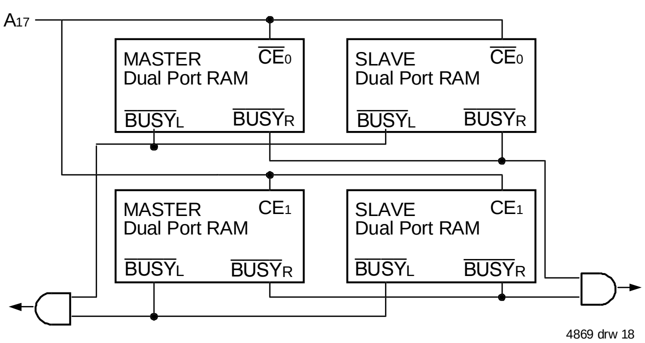


Figure 3. Busy and chip enable routing for both width and depth expansion with IDT70V659 RAMs.

Width Expansion with Busy Logic Master/Slave Arrays

When expanding an IDT70V659 RAM array in width while using $\overline{BUSY}$ logic, one master part is used to decide which side of the RAMs array will receive a $\overline{BUSY}$ indication, and to output that indication. Any number of slaves to be addressed in the same address range as the master use the $\overline{BUSY}$ signal as a write inhibit signal. Thus on the IDT70V659 RAM the $\overline{BUSY}$ pin is an output if the part is used as a master (M/$\overline{S}$ pin = V_{IH}), and the $\overline{BUSY}$ pin is an input if the part used as a slave (M/$\overline{S}$ pin = V_{IL}) as shown in Figure 3.

If two or more master parts were used when expanding in width, a split decision could result with one master indicating $\overline{BUSY}$ on one side of the array and another master indicating $\overline{BUSY}$ on one other side of the array. This would inhibit the write operations from one port for part of a word and inhibit the write operations from the other port for the other part of the word.

The $\overline{BUSY}$ arbitration on a master is based on the chip enable and address signals only. It ignores whether an access is a read or write. In a master/slave array, both address and chip enable must be valid long enough for a $\overline{BUSY}$ flag to be output from the master before the actual write pulse can be initiated with the R/$\overline{W}$ signal. Failure to observe this timing can result in a glitched internal write inhibit signal and corrupted data in the slave.

Semaphores

The IDT70V659 is an extremely fast Dual-Port 128K x 36 CMOS Static RAM with an additional 8 address locations dedicated to binary semaphore flags. These flags allow either processor on the left or right side of the Dual-Port RAM to claim a privilege over the other processor for functions defined by the system designer's software. As an example, the semaphore can be used by one processor to inhibit the other from accessing a portion of the Dual-Port RAM or any other shared resource.

The Dual-Port RAM features a fast access time, with both ports being completely independent of each other. This means that the activity on the left port in no way slows the access time of the right port. Both ports are identical in function to standard CMOS Static RAM and can be read from or written to at the same time with the only possible conflict arising from the simultaneous writing of, or a simultaneous READ/WRITE of, a non-semaphore location. Semaphores are protected against such ambiguous situations and may be used by the system program to avoid any conflicts in the non-semaphore portion of the Dual-Port RAM. These devices have an automatic power-down feature controlled by $\overline{CE}$, the Dual-Port RAM enable, and $\overline{SEM}$, the semaphore enable. The $\overline{CE}$ and $\overline{SEM}$ pins control on-chip power down circuitry that permits the respective port to go into standby mode when not selected.

Systems which can best use the IDT70V659 contain multiple processors or controllers and are typically very high-speed systems which are software controlled or software intensive. These systems can benefit from a performance increase offered by the IDT70V659s hardware semaphores, which provide a lockout mechanism without requiring complex programming.

Software handshaking between processors offers the maximum in system flexibility by permitting shared resources to be allocated in varying configurations. The IDT70V659 does not use its semaphore flags to control any resources through hardware, thus allowing the system designer total flexibility in system architecture.

An advantage of using semaphores rather than the more common methods of hardware arbitration is that wait states are never incurred in either processor. This can prove to be a major advantage in very high-speed systems.

How the Semaphore Flags Work

The semaphore logic is a set of eight latches which are independent of the Dual-Port RAM. These latches can be used to pass a flag, or token, from one port to the other to indicate that a shared resource is in use. The semaphores provide a hardware assist for a use assignment method called "Token Passing Allocation." In this method, the state of a semaphore latch is used as a token indicating that a shared resource is in use. If the left processor wants to use this resource, it requests the token by setting the latch. This processor then verifies its success in setting the latch by reading it. If it was successful, it proceeds to assume control over the shared resource. If it was not successful in setting the latch, it determines that the right side processor has set the latch first, has the token and is using the shared resource. The left processor can then either repeatedly request that semaphore's status or remove its request for that semaphore to perform another task and occasionally attempt again to gain control of the token via the set and test sequence. Once the right side has relinquished the token, the left side should succeed in gaining control.

The semaphore flags are active LOW. A token is requested by writing a zero into a semaphore latch and is released when the same side writes a one to that latch.

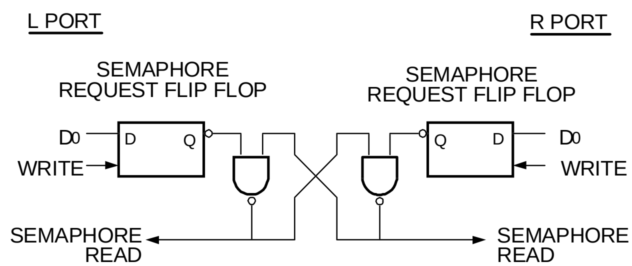
The eight semaphore flags reside within the IDT70V659 in a separate memory space from the Dual-Port RAM. This address space is accessed by placing a low input on the $\overline{SEM}$ pin (which acts as a chip select for the semaphore flags) and using the other control pins (Address, $\overline{CE}$, R/$\overline{W}$ and $\overline{BE}_0$) as they would be used in accessing a standard Static RAM. Each of the flags has a unique address which can be accessed by either side through address pins A_0 – A_2. When accessing the semaphores, none of the other address pins has any effect.

When writing to a semaphore, only data pin D_0 is used. If a low level is written into an unused semaphore location, that flag will be set to a zero on that side and a one on the other side (see Truth Table V). That semaphore can now only be modified by the side showing the zero. When a one is written into the same location from the same side, the flag will be set to a one for both sides (unless a semaphore request from the other side is pending) and then can be written to by both sides. The fact that the side which is able to write a zero into a semaphore subsequently locks out writes from the other side is what makes semaphore flags useful in interprocessor communications. (A thorough discussion on the use of this feature follows shortly.) A zero written into the same location from the other side will be stored in the semaphore request latch for that side until the semaphore is freed by the first side.

When a semaphore flag is read, its value is spread into all data bits so that a flag that is a one reads as a one in all data bits and a flag containing a zero reads as all zeros. The read value is latched into one side's output register when that side's semaphore select ($\overline{SEM}$, $\overline{BE}_n$) and output enable ($\overline{OE}$) signals go active. This serves to disallow the semaphore from changing state in the middle of a read cycle due to a write cycle from the other side. Because of this latch, a repeated read of a semaphore in a test loop must cause either signal ($\overline{SEM}$ or $\overline{OE}$) to go inactive or the output will never change. However, during reads $\overline{BE}_n$ functions only as an output for semaphore. It does not have any influence on the semaphore control logic.

A sequence WRITE/READ must be used by the semaphore in order to guarantee that no system level contention will occur. A processor requests access to shared resources by attempting to write a zero into a semaphore location. If the semaphore is already in use, the semaphore request latch will contain a zero, yet the semaphore flag will appear as one, a fact which the processor will verify by the subsequent read (see Table V). As an example, assume a processor writes a zero to the left port at a free semaphore location. On a subsequent read, the processor will verify that it has written successfully to that location and will assume control over the resource in question. Meanwhile, if a processor on the right side attempts to write a zero to the same semaphore flag it will fail, as will be verified by the fact that a one will be read from that semaphore on the right side during subsequent read. Had a sequence of READ/WRITE been used instead, system contention problems could have occurred during the gap between the read and write cycles.

It is important to note that a failed semaphore request must be followed by either repeated reads or by writing a one into the same location. The reason for this is easily understood by looking at the simple logic diagram of the semaphore flag in Figure 4. Two semaphore request latches feed into a semaphore flag. Whichever latch is first to present a zero to the semaphore flag will force its side of the semaphore flag LOW and the other side HIGH. This condition will



4869 drw 19

Figure 4. IDT70V659 Semaphore Logic

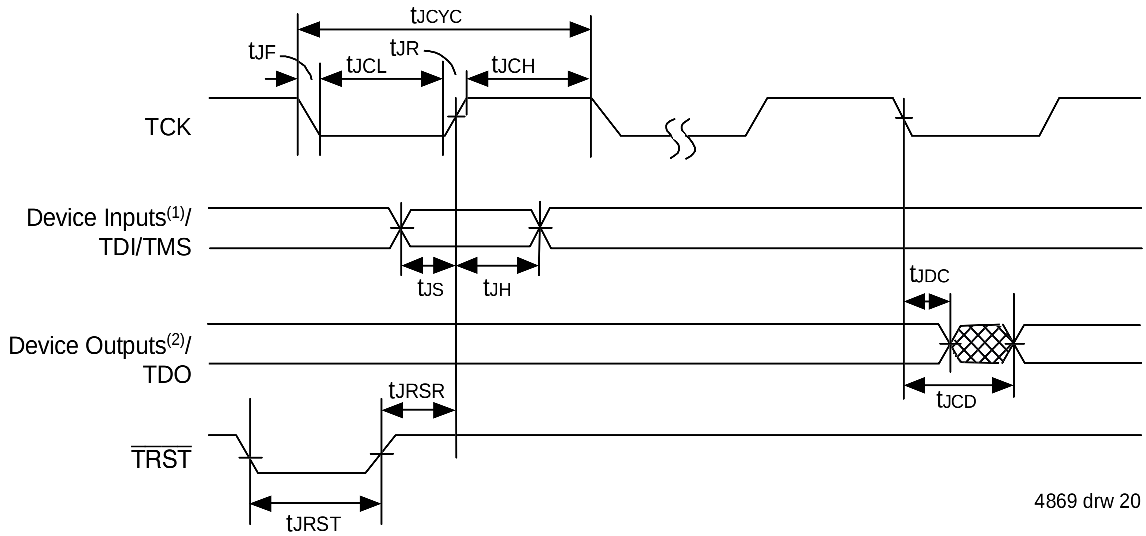
continue until a one is written to the same semaphore request latch. Should the other side's semaphore request latch have been written to a zero in the meantime, the semaphore flag will flip over to the other side as soon as a one is written into the first side's request latch. The second side's flag will now stay LOW until its semaphore request latch is written to a one. From this it is easy to understand that, if a semaphore is requested and the processor which requested it no longer needs the resource, the entire system can hang up until a one is written into that semaphore request latch.

The critical case of semaphore timing is when both sides request a single token by attempting to write a zero into it at the same time. The semaphore logic is specially designed to resolve this problem. If simultaneous requests are made, the logic guarantees that only one side receives the token. If one side is earlier than the other in making the request, the first side to make the request will receive the token. If both requests arrive at the same time, the assignment will be arbitrarily made to one port or the other.

One caution that should be noted when using semaphores is that semaphores alone do not guarantee that access to a resource is secure. As with any powerful programming technique, if semaphores are misused or misinterpreted, a software error can easily happen.

Initialization of the semaphores is not automatic and must be handled via the initialization program at power-up. Since any semaphore request flag which contains a zero must be reset to a one, all semaphores on both sides should have a one written into them at initialization from both sides to assure that they will be free when needed.

JTAG Timing Specifications



NOTES:
1. Device inputs = All device inputs except TDI, TMS, and TRST.
2. Device outputs = All device outputs except TDO.

JTAG AC Electrical Characteristics(1,2,3,4)

Symbol	Parameter	Min.	Max.	Units
t_{JCYC}	JTAG Clock Input Period	100	—	ns
t_{JCH}	JTAG Clock HIGH	40	—	ns
t_{JCL}	JTAG Clock Low	40	—	ns
t_{JR}	JTAG Clock Rise Time	—	3(1)	ns
t_{JF}	JTAG Clock Fall Time	—	3(1)	ns
t_{JRST}	JTAG Reset	50	—	ns
t_{JRSR}	JTAG Reset Recovery	50	—	ns
t_{JCD}	JTAG Data Output	—	25	ns
t_{JDC}	JTAG Data Output Hold	0	—	ns
t_{JS}	JTAG Setup	15	—	ns
t_{JH}	JTAG Hold	15	—	ns

4869 tbl 19

NOTES:
1. Guaranteed by design.
2. 30pF loading on external output signals.
3. Refer to AC Electrical Test Conditions stated earlier in this document.
4. JTAG operations occur at one speed (10MHz). The base device may run at any speed specified in this datasheet.

Identification Register Definitions

Instruction Field	Value	Description
Revision Number (31:28)	0x0	Reserved for version number
IDT Device ID (27:12)	0x303	Defines IDT part number
IDT JEDEC ID (11:1)	0x33	Allows unique identification of device vendor as IDT
ID Register Indicator Bit (Bit 0)	1	Indicates the presence of an ID register

4869 tbl 20

Scan Register Sizes

Register Name	Bit Size
Instruction (IR)	4
Bypass (BYR)	1
Identification (IDR)	32
Boundary Scan (BSR)	Note (3)

4869 tbl 21

System Interface Parameters

Instruction	Code	Description
EXTEST	0000	Forces contents of the boundary scan cells onto the device outputs(1). Places the boundary scan register (BSR) between TDI and TDO.
BYPASS	1111	Places the bypass register (BYR) between TDI and TDO.
IDCODE	0010	Loads the ID register (IDR) with the vendor ID code and places the register between TDI and TDO.
HIGHZ	0100	Places the bypass register (BYR) between TDI and TDO. Forces all device output drivers to a High-Z state.
CLAMP	0011	Uses BYR. Forces contents of the boundary scan cells onto the device outputs. Places the bypass register (BYR) between TDI and TDO.
SAMPLE/PRELOAD	0001	Places the boundary scan register (BSR) between TDI and TDO. SAMPLE allows data from device inputs(2) and outputs(1) to be captured in the boundary scan cells and shifted serially through TDO. PRELOAD allows data to be input serially into the boundary scan cells via the TDI.
RESERVED	All other codes	Several combinations are reserved. Do not use codes other than those identified above.

4869 tbl 22

NOTES:
1. Device outputs = All device outputs except TDO.
2. Device inputs = All device inputs except TDI, TMS, and $\overline{TRST}$.
3. The Boundary Scan Descriptive Language (BSDL) file for this device is available on the IDT website (www.idt.com), or by contacting your local IDT sales representative.

Ordering Information

IDT XXXXX A 999 A A

Device Type — Power — Speed — Package — Process/Temperature Range

Process/Temperature Range:
- Blank: Commercial (0°C to +70°C)
- I: Industrial (-40°C to +85°C)

Package:
- BF: 208-ball fpBGA (BF-208)
- DR: 208-pin PQFP (DR-208)
- BC: 256-ball BGA (BC-256)

Speed (Speed in nanoseconds):
- 10: Commercial Only
- 12: Commercial & Industrial
- 15: Commercial & Industrial

Power:
- S: Standard Power

Device Type:
- 70V659: 4608K (128K x 36) Asynchronous Dual-Port RAM

4869 drw 21

Preliminary Datasheet: Definition

"PRELIMINARY' datasheets contain descriptions for products that are in early release.

Datasheet Document History:

6/2/00: Initial Public Offering.
8/11/00: Inserted additional $\overline{BE}$n information on pages 6,13,20.
6/20/01: Increased $\overline{BUSY}$ TIMING parameters t_{BDA}, t_{BAC}, t_{BDC} and t_{BDD} for all speeds on page 14.
Changed maximum value for JTAG AC Electrical Characteristics for t_{JCD} from 20ns to 25ns on page 21.

CORPORATE HEADQUARTERS
2975 Stender Way
Santa Clara, CA 95054

for SALES:
800-345-7015 or 408-727-6116
fax: 408-492-8674
www.idt.com

for Tech Support:
831-754-4613
DualPortHelp@idt.com