CAT35C204
4K BIT SERIAL E²PROM

1MHz OPERATION

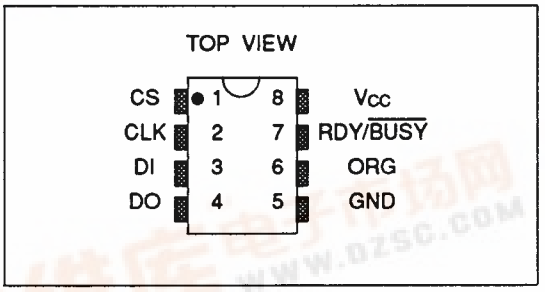
DESCRIPTION

The CAT35C204 is a 4K bit Serial E²PROM memory device organized in 256 registers of 16 bits (ORG pin at Vcc) or 512 registers of 8 bits each (ORG pin at GND). Each register can be written (or read) serially by using the DI (or DO) pin. The CAT35C204 is manufactured using Catalyst's advanced CMOS E²PROM floating gate technology. It is designed to endure 10,000 erase/write cycles and has a data retention of 10 years. Packaged in an 8-pin DIP and Small Outline packages. Also to be available in a 3V version (CAT33C204).

FEATURES

- Compatible with General Instruments ER5912
- Single 5V supply
- 256x16 or 512x8 user selectable serial memory
- 10ms programming cycle
- Self timed programming cycle with Autoerase
- Highly reliable CMOS floating gate technology
- Word and chip erasable
- Operating range 0°C to +70°C [Industrial temp. range available]
- 10,000 erase/write cycles
- 10 year data retention
- Power-up inadvertent write protection

PIN CONFIGURATION

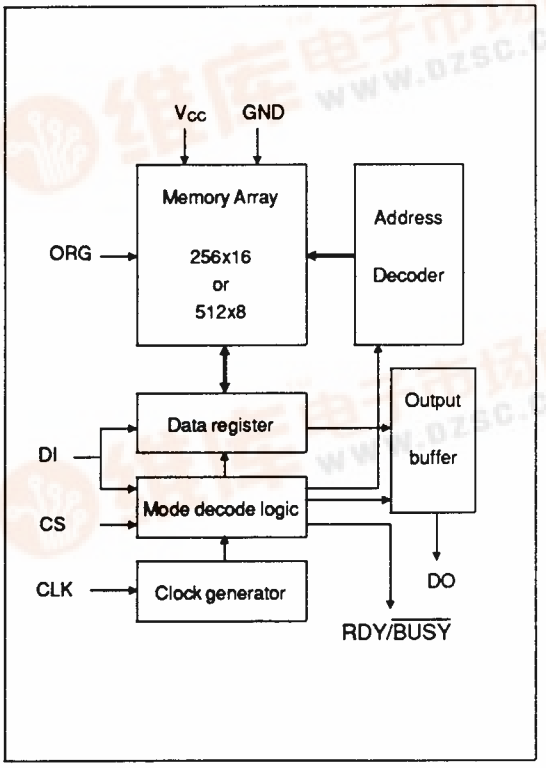


PIN FUNCTIONS

CS	Chip select
CLK	Clock input
DI	Serial data input
DO	Serial data output
Vcc	+5V power supply
RDY/BUSY	Status output
GND	Ground
ORG	Memory organization

Note: When the ORG pin is connected to Vcc, the 256x16 organization is selected. When it is connected to ground, the 512x8 organization is selected. If the ORG pin is left unconnected, then an internal pullup device will select the 256x16 organization.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Storage temperature . . . . . -65°C to +150°C
Power supply (V_{CC}) . . . . . +7V
Voltage on any input pin . . . . . -0.3 to +7V
Voltage on any output pin . . . . . -0.3V to V_{CC} +0.3V

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

(V_{CC} = +5V ±10%, T_A = 0°C to +70°C)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
I_{CC1}	Current consumption (operating)	DI=0.0V, SK=5.0V V_{CC} =5.0V, CS = 5.0V DO unloaded			3	mA
I_{CC2}	Current consumption (stand-by)	V_{CC} = 5.5V, CS = 0 DI = 0, SK = 0			100	µA
I_{LI}	Input leakage current	V_{IN} = 5.5V			10	µA
I_{LO}	Output leakage current	V_{OUT} = 5.5V, CS = 0			10	µA
V_{IH}	High level input voltage		2.0		V_{CC} +1	V
V_{IL}	Low level input voltage		-0.1		0.8	V
V_{OH}	High level output voltage	I_{OH} = -400µA	2.4			V
V_{OL}	Low level output voltage	I_{OL} = 2.1mA			0.4	V

INSTRUCTION SET

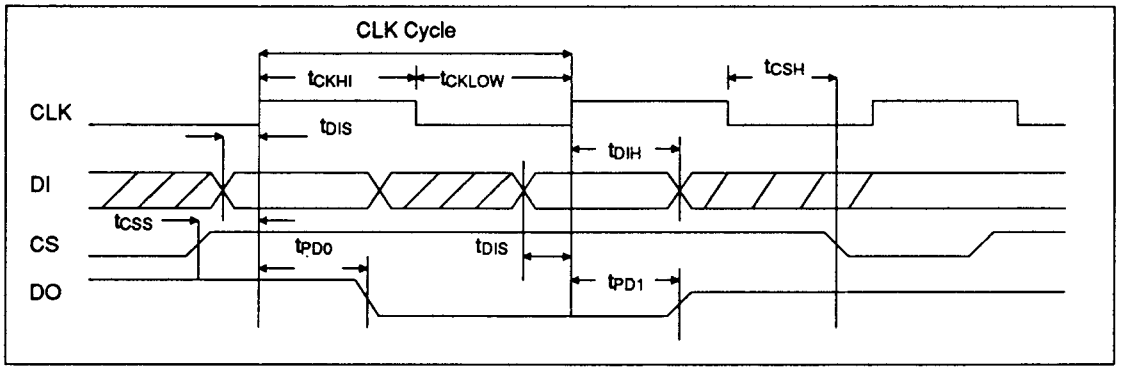
Instruction	Start Bit	Opcode	Address		Data		Comments
			512 x 8	256 x 16	512 x 8	256 x 16	
READ	1	1000	A8 - A0	A7 - A0			Read address AN - A0
PROGRAM	1	X100	A8 - A0	A7 - A0	D7 - D0	D15 - D0	Program address AN - A0
PEN	1	0011	000000000	00000000			Program enable
PDS	1	0000	000000000	00000000			Program disable
ERAL	1	0010	000000000	00000000			Erase all addresses
WRAL	1	0001	000000000	00000000	D7 - D0	D15 - D0	Write all addresses

AC CHARACTERISTICS

(V_{CC} = +5V ±10%, T_A = 0°C to +70°C)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
t_{CSS}	CS setup time		50			ns
t_{CSH}	CS hold time	C_L = 100pF V_{OL} = 0.8V, V_{OH} = 2.0V V_{IL} = 0.45V, V_{IH} = 2.4V	100			ns
t_{DIS}	DI setup time		100			ns
t_{DIH}	DI hold time		100			ns
t_{PD1}	Output delay to 1				500	ns
t_{PD0}	Output delay to 0				500	ns
t_{EW}	Erase/Write pulse width				10	ms
t_{SKHI}	Minimum SK high time		250			ns
t_{SKLOW}	Minimum SK low time		250			ns
CK_{MAX}	Maximum clock frequency		DC		1	MHz

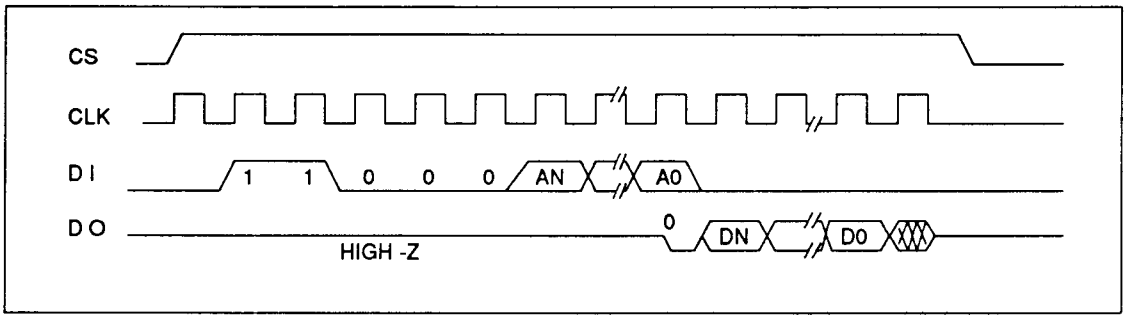
SYNCHRONOUS TIMINGS



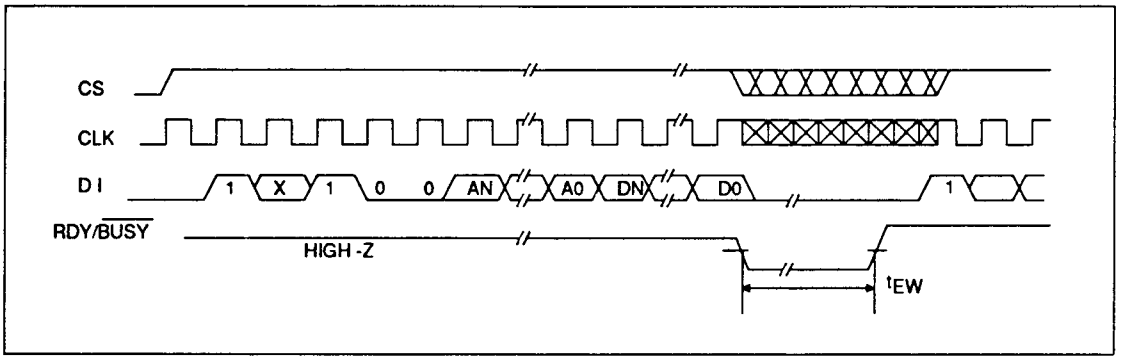
INSTRUCTION TIMING <ORGANIZATION>

Organization	A_N (or AN)	D_N (or DN)
512 x 8	A_8	D_7
256 x 16	A_7	D_{15}

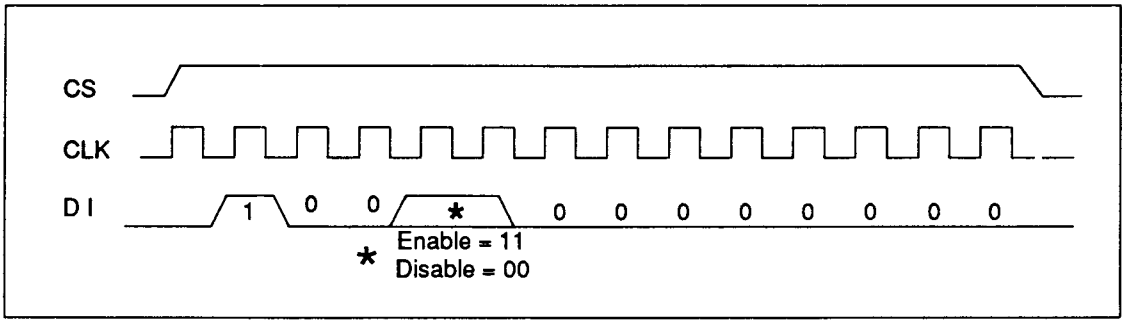
INSTRUCTION TIMING <READ>



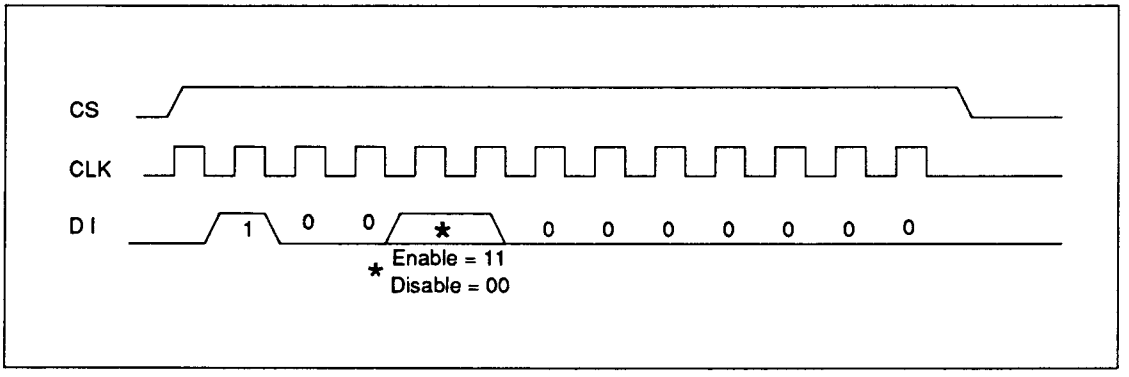
INSTRUCTION TIMING <PROGRAM>



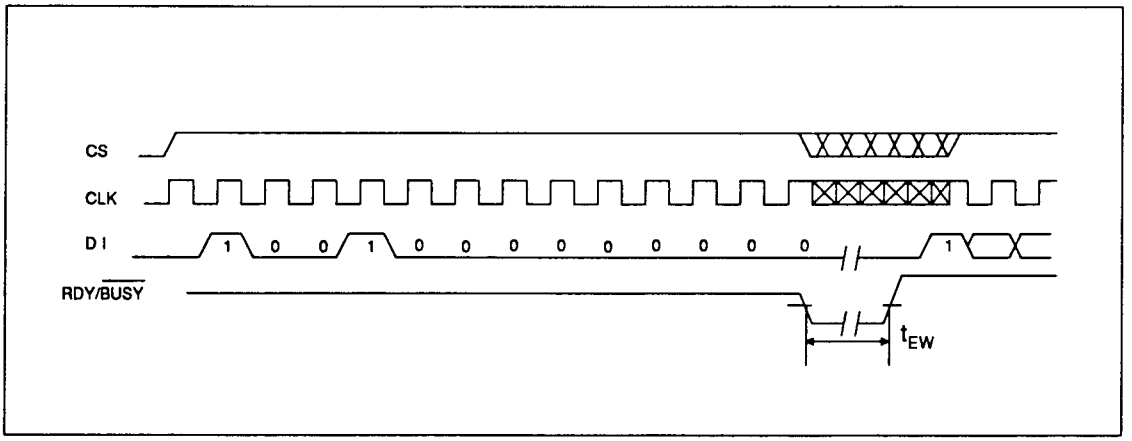
INSTRUCTION TIMING <PEN, PDS 512 x 8 organization>



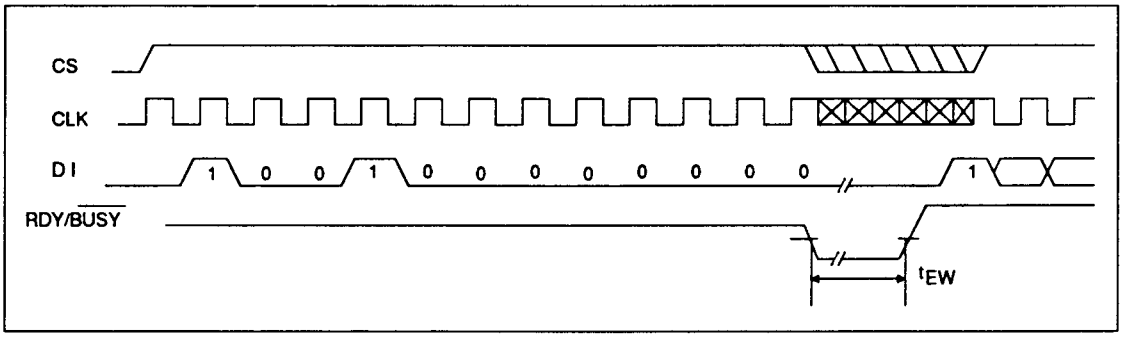
INSTRUCTION TIMING <PEN, PDS 256 x 16 organization>



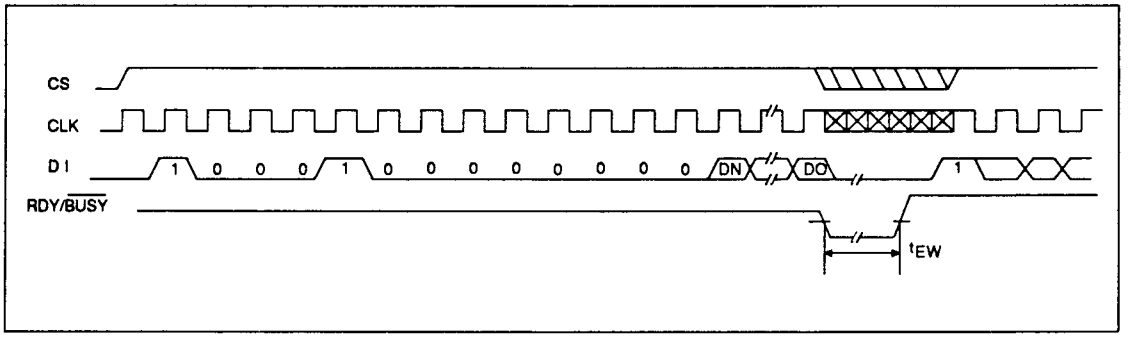
INSTRUCTION TIMING <ERAL 512 x 8 organization>



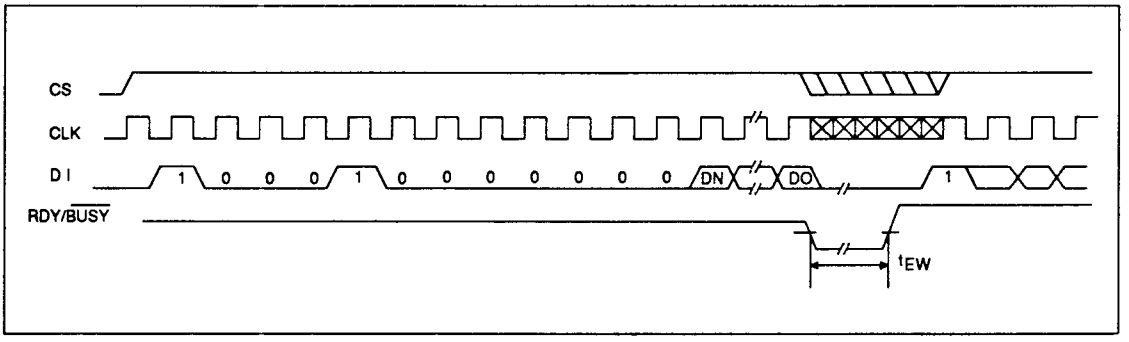
INSTRUCTION TIMING <ERAL 256 x 16 organization>



INSTRUCTION TIMING <WRAL 512 x 8 organization>



INSTRUCTION TIMING <WRAL 256 x 16 organization>



DEVICE OPERATION

The CAT35C204H is a high endurance 4096 bit nonvolatile memory intended for use with all standard controllers. The CAT35C204H can be organized as either 256 registers by 16 bits, or as 512 registers by 8 bits. Six 13 bit instructions (14 bit instruction in 512 by 8 organization) control the reading, writing, and erase operations of the device. The CAT35C204H operates on a single 5V supply and will generate on chip the high voltage required during any programming operations. Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (CLK). The DO pin is normal in a high impedance state except when reading data from the device. The ready/busy status can be determined after a programming operation by polling the RDY/$\overline{\text{BUSY}}$ pin.

The format for all instructions sent to the CAT35C204H is one logical "1" start bit, a 4 bit op code, an 8 bit address (9 bit address when organized as 512 X 8), and for write operations a 16 bit data field (8 bit data field when organized as 512 X 8).

READ

Upon receiving a READ command and address (clocked into the DI pin), the DO pin of the CAT35C204H will come out of the high impedance state. After sending 1 dummy zero bit the 16 bits (or 8 bits) of data located at the address location specified in the instruction will be shifted out. The data bit being shifted out will toggle on the rising edge of the CLK and becomes stable after the specified time delay (t_{PD1} and t_{PD0}).

ERASE/WRITE ENABLE AND DISABLE

The CAT35C204H powers up in the programming disable state. Any programming after power-up or after a PDS (programming disable) instruction must first be preceded by the PEN (programming enable) instruction. Once programming is enabled, it will remain enabled until power to the device is removed or the PDS instruction is sent. The PDS instruction can be used to disable all the CAT35C204H's program and erase functions, and will prevent any accidental programming or erasing of the device. Data can be read normally from the CAT35C204H regardless of the programming enable/disable status.

PROGRAM

After receiving a PROGRAM command, address, and the data, the RDY/$\overline{\text{BUSY}}$ pin goes low and the self clocking erase and data store cycle begins. The clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT35C204H can be determined by polling the RDY/$\overline{\text{BUSY}}$ pin.

ERASE ALL

Upon receiving an ERAL command, the RDY/$\overline{\text{BUSY}}$ pin goes low and the self clocking erase sequence starts. The clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT35C204H can be determined by polling the RDY/$\overline{\text{BUSY}}$ pin. Once erased, all memory bits return to logical "1" state.

WRITE ALL

Upon receiving a WRAL command and data, the RDY/$\overline{\text{BUSY}}$ pin goes low and the self clocking data store cycle starts. The clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT35C204H can be determined by polling the RDY/$\overline{\text{BUSY}}$ pin. It **IS NOT** necessary for all memory locations to be erased before the WRAL command is executed.